Received 28 December 2021; revised 12 February 2022; accepted 12 March 2022. Date of publication 21 March 2022; date of current version 28 March 2022.
The review of this article was arranged by Editor N. Collaert.

Digital Object Identifier 10.1109/JEDS.2022.3160881

Significance of Overdrive Voltage in the Analysis of Short-Channel Behaviors of n-FinFET Devices

YI-CHUEN ENG [1] (Member, IEEE), LUKE HU [1] (Member, IEEE), TZU-FENG CHANG [1], CHIH-YI WANG [1], STEVEN HSU [1], OSBERT CHENG [2] (Member, IEEE), CHIEN-TING LIN [1], YU-SHIANG LIN [1], ZEN-JAY TSAI [1], CHIH-WEI YANG [1], JIM LU [1], AND STEVE YI-WEN CHEN [1]

1 Technology Development Division, United Microelectronics Corporation, Tainan 744, Taiwan
2 Device Technology Development & Design Division, United Microelectronics Corporation, Tainan 744, Taiwan

CORRESPONDING AUTHOR: Y.-C. ENG (e-mail: yi_chuen_eng@umc.com; eyc03m@yahoo.com)

ABSTRACT The short–channel behaviors of n–channel (electron–conducting) fin field–effect transistors (n–FinFETs) set at different threshold voltages were analyzed at different power supply voltages. Interesting observations were made by considering the on and off voltage states of the overdrive voltage instead of the gate–source voltage. Intrinsic transistor characteristics were revealed, enabling the comparison of short–channel characteristics between devices designed for different threshold voltages. Drain–induced barrier lowering (DIBL), subthreshold swing (SS), on/off current ratio, I_{on}/I_{off}, and other parameters of the devices were considered. In addition, the novel figure of merit introduced in our previous work for the evaluation of short–channel effects, which accounts for the DIBL, SS, and I_{on}/I_{off} of the devices, was also analyzed under this context. It was shown that the off–state current does not increase significantly with the increase in the supply voltage, indicating good gate control.

INDEX TERMS $\Delta V_{DIBLSS}/(I_{on}/I_{off})$, V_{SCE}, FinFETs, intrinsic voltage gain, multiple devices, overdrive voltage, performance metrics, transistor intrinsic delay.

I. INTRODUCTION

With the shrinking of gate length, the circuit speed has improved with increasing on–state current, I_{on} [1]. At zero gate–source voltage, V_{gs}, an ideal metal–oxide–semiconductor field–effect transistor (MOSFET) is in the off state. This means that the transistor channel conducts an exceedingly small off–state current, I_{off}. In reality, short–channel effects (SCE) arise because the channel potential barrier height is no longer controlled entirely by V_{gs} [1]. The drain–source voltage, V_{ds}, also contributes to the lowering of the barrier height, which reduces the threshold voltage, V_t [1]. This inevitable phenomenon in short–channel devices is usually addressed with a variety of process optimizations.

Another short–channel phenomenon related to the off–state leakage current is the significant degradation in the subthreshold swing (SS). In order to achieve a high I_{on} and a low I_{off}, SS should be as small as possible. In order to achieve a small SS, a high level of control of the gate over the channel carriers is essential. If SCE cannot be effectively suppressed, the on/off current ratio, I_{on}/I_{off}, would decrease as device dimensions continue to scale down [1]–[4].

In theory, comparisons between the I_{on}/I_{off} and the SCE of devices with the same V_t are useful in revealing their relative performance and robustness. However, V_t is different for every device, rendering the direct comparison of different devices meaningless. To resolve this issue of comparison, we have found that by considering the on and off voltage states of the overdrive voltage, V_{ov} ($= V_{gs} - V_t$), the intrinsic I_{on}/I_{off} can be extracted. Since the intrinsic I_{on}/I_{off} is independent of the V_t, this value can be useful in quickly comparing the performance between several devices.

In this work, different types of devices are analyzed by comparing their short–channel behaviors and their intrinsic performance. In addition, the effects of different power supply voltages on the performance of transistors will be demonstrated. Section II covers the concept of intrinsic performance of core devices and the role of the novel figure of merit (FoM) introduced in our previous work [5]–[7].

Section III introduces the fabrication process of FinFET devices and defines several parameters we will use throughout this work. Section IV displays and discusses the actual data of the FinFET devices. Finally, Section V concludes this material.

II. INTRINSIC PERFORMANCE AND THE NOVEL FIGURE OF MERIT

A. INTRINSIC PERFORMANCE OF CORE DEVICES

Four types of devices are presented, differentiated by the level of V_t: standard–V_t (SVT), low–V_t (LVT), extreme–low–V_t (ELVT), and ultra–low–V_t (ULVT). These devices are categorized as core devices. V_t is one of the most important parameters in a MOSFET as it governs the I_{on}/I_{off}. I_{off}, in particular, dominates the difference in I_{on}/I_{off} for different threshold voltages. SVT devices, by definition, exhibit the highest I_{on}/I_{off} as compared to other core devices. However, aside from V_t (due to process tuning), other factors can also significantly affect the I_{off} of a MOSFET, including short–channel characteristics such as drain–induced barrier lowering (DIBL) and SS.

In order to evaluate and compare the intrinsic performances between different types of devices, a method is needed in order to disregard the effect of different saturation threshold voltages on the I_{on}/I_{off}. This can be accomplished by investigating the intrinsic I_{on}/I_{off} by considering the on and off voltage states of the overdrive voltage, V_{ov} ($= V_{gs} - V_t$), instead of just V_{gs}.

B. THE NOVEL FOM: $\Delta V_{DIBLSS}/(I_{ON}/I_{OFF})$

References [5]–[7] focused on the electrical characterization of SVT and LVT devices and introduced the FoM, $\Delta V_{DIBLSS}/(I_{on}/I_{off})$, to make comparisons between the overall behaviors of FinFETs. ΔV_{DIBLSS} was introduced in [5] and accounts for the DIBL and SS of the transistors (see Table 1). I_{on}/I_{off} is the on/off current ratio of the transistors. We define the SCE voltage, V_{SCE}, to be equivalent to $\Delta V_{DIBLSS}/(I_{on}/I_{off})$. This value indicates how well a transistor performs in the short–channel regime. Based on the results obtained from [5]–[7], we can see that the smaller the ΔV_{DIBLSS}, the higher the I_{on}/I_{off}. Hence, smaller V_{SCE} is indicative of a device with better short–channel performance. The relationships between V_{SCE} and both ΔV_{DIBLSS} and I_{on}/I_{off} (or V_t) are presented.

III. EXPERIMENT

A. DEVICE FABRICATION

n–channel (electron–conducting) fin field–effect transistors (n–FinFETs) with gate lengths between 16 nm and 20 nm were fabricated on P–type silicon (Si) substrates. (In P–type Si, the abundant holes make up the majority carriers, and the minority carriers, electrons, are almost inexistent.) Major steps in the fabrication process of n–FinFETs are as follows (see Fig. 1). The Si wafers were implanted with boron monofluoride (BF) ions to form p–well (2.5×10^{19} cm^{-3} to 5×10^{19} cm^{-3}). The Fin height ranges from 43 nm to 44.5 nm and the Fin width ranges from 11.4 nm to 12.1 nm. Polycrystalline Si (Poly–Si) was deposited over the Si surface. Next, lithography and plasma etching were used to define the gate. In–situ growth of phosphorus–doped Si was performed to create source/drain structures. All four types of core devices have similar hafnium oxide thicknesses from 1.82 nm to 2.03 nm that serve as the high–k dielectric. Different work function metals were used for different types of devices. Finally, the contacts and the metal interconnects were fabricated to complete the process. The ranges of the parameters mentioned earlier (gate length, Fin height, Fin width, etc.) are due to the manufacturing process variations.

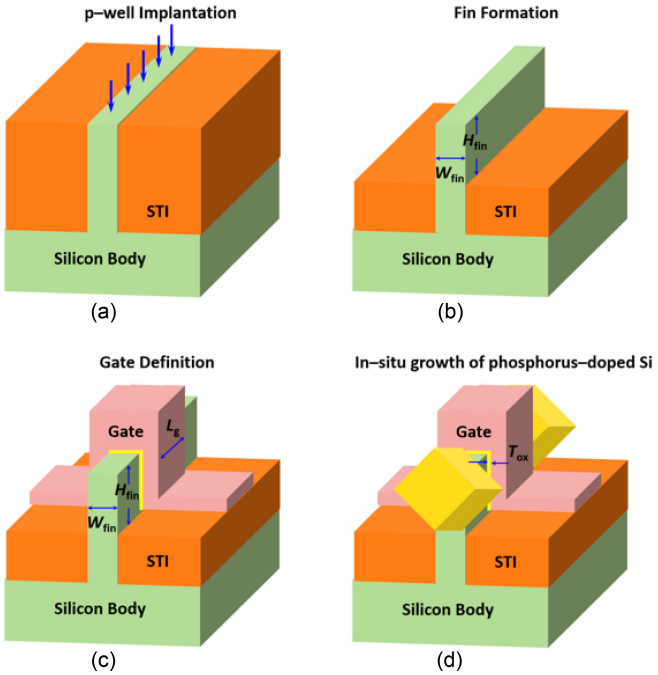


FIGURE 1. Key fabrication steps of the n–channel FinFET. (a) p–well implantation, (b) Fin formation, (c) Gate definition, and (d) In–situ growth of phosphorus–doped Si. STI: Shallow trench isolation. H_{fin}: Fin height. W_{fin}: Fin width. L_g: Gate length. T_{ox}: Gate oxide thickness.

B. ELECTRICAL PARAMETERS OF FINFETS

The measured FinFET data (at $V_{dd} = 0.4$ and 0.8 V) were obtained from the wafer acceptance test carried out at the end of the process. Table 1 shows the electrical parameters of FinFETs. The constant–current (CC) method [14] is used to extract the threshold voltage, V_t, from the $I_{ds}-V_{gs}$ plot (where I_{ds} is the drain–to–source current and V_{gs} is the gate–source voltage). In this work, we have selected 1×10^{-8} A as the CC from [16]. Linear threshold voltage, $V_{t,lin}$, is measured at a very low drain–source voltage, V_{ds}, of 50 mV (or $V_{ds,low}$). Saturation threshold voltage, $V_{t,sat}$, is measured at the power supply voltage, V_{dd} (0.4 V and 0.8 V). The drain–induced barrier lowering (DIBL) is then calculated as $(V_{t,lin} - V_{t,sat})/(V_{dd} - V_{ds,low})$ (or DIBL $= \Delta V_{DIBL}/(V_{dd} - V_{ds,low})$). The subthreshold swing (SS) is defined as $dV_{gs}/d(\log I_{ds}) \approx \Delta V_{gs}/\Delta I_{ds} =$

TABLE 1. Electrical parameters of FinFETs.

Parameters	Description	Remark
V_b, V_s, V_d, V_g	Terminal voltages: body (B), source (S), drain (D), and gate (G)	V_b = GND (= V_s) GND: Ground
V_{gs}	Gate–source voltage	V_{gs}: G
V_{ds}	Drain–source voltage	V_{ds}: D
$V_{ds,low}$	Low drain–source voltage	$V_{ds,low}$ = 50 mV (D = 50 mV)
V_{ov}	Overdrive voltage	$V_{ov} = V_{gs} - V_{t,sat}$
V_{dd}	Power supply voltage	0.4 V and 0.8 V
I_{ds}	Drain–to–source current	-
Device characteristics	**Description**	**Remark**
V_t (mV)	Threshold voltage	$V_t = V_{gs}$ @ $I_{ds} = I_0 \times$ W/L [5], [14] I_0: I_{ds} (= 1×10^{-8} A) [16] at which we define the V_t where W is the Fin width and L is the gate length
$V_{t,lin}$ (mV)	Linear threshold voltage	$V_{t,lin} = V_t$ @ $V_{ds} = V_{ds,low}$
$V_{t,sat}$ (mV)	Saturation threshold voltage	$V_{t,sat} = V_t$ @ $V_{ds} = V_{dd}$ (0.4 V and 0.8 V)
DIBL (mV/V)	Drain–induced barrier lowering	DIBL = $(V_{t,lin} - V_{t,sat})/(V_{dd} - V_{ds,low}) = \Delta V_{DIBL}/(V_{dd} - V_{ds,low})$
SS (mV/dec)	Subthreshold swing	SS = $dV_{gs}/d(\log I_{ds}) \approx \Delta V_{gs}/\Delta I_{ds} = \Delta V_{SS}/\Delta I_{ds}$ [5]
ΔV_{DIBLSS} (mV)	Gate controllability over the channel	$\Delta V_{DIBLSS} = \Delta V_{DIBL} + \Delta V_{SS}$
I_{on} (μA/μm)	On–state current	$I_{on} = I_{ds}$ @ $V_{gs} = V_{ds} = V_{dd}$ (normal "on" state) $I_{on} = I_{ds}$ @ $V_{ov} = V_{ds} = V_{dd}$ (intrinsic "on" state)
I_{off} (μA/μm)	Off–state current	$I_{off} = I_{ds}$ @ $V_{gs} = 0$ V & $V_{ds} = V_{dd}$ (normal "off" state) $I_{off} = I_{ds}$ @ $V_{ov} = 0$ V & $V_{ds} = V_{dd}$ (intrinsic "off" state)
I_{on}/I_{off}	On/off current ratio	-
V_{SCE} (mV)	Short–channel effects (SCE) voltage	$V_{SCE} = \Delta V_{DIBLSS}/(I_{on}/I_{off})$
$C_{g,total}$ (F/μm)	Total gate capacitance in inversion	-
τ (ps)	Intrinsic MOSFET delay	$\tau = C_{g,total}V_{dd}/I_{on} = CV/I$
g_m (μS/μm)	Transconductance	$g_m = dI_{ds}/dV_{gs}$
r_o (kΩ-μm)	Output resistance	$r_o = (dI_{ds}/dV_{ds})^{-1}$
$g_m r_o$	Intrinsic voltage gain	-

$\Delta V_{SS}/\Delta I_{ds}$ [5]. (Here, ΔV_{SS} is defined to be equal to ΔV_{gs}.) For ΔV_{SS}, we have selected a value which results in a ten-fold increase of ΔI_{ds} from 1×10^{-10} A to 1×10^{-9} A in [16]. In [5], $\Delta V_{DIBLSS} = \Delta V_{DIBL} + \Delta V_{SS}$ represents the gate controllability over the channel.

On–state current, I_{on}, is the I_{ds} when $V_{gs} = V_{ds} = V_{dd}$ (normal on–state). And off–state current, I_{off}, is the I_{ds} when $V_{gs} = 0$ V and $V_{ds} = V_{dd}$ (normal off–state). The ratio of I_{on} to I_{off} is called the on/off current ratio of the devices. We define the FoM [6], [7] known as the SCE voltage, V_{SCE}, as $\Delta V_{DIBLSS}/(I_{on}/I_{off})$, which indicates how well devices will perform in the short–channel regime. For V_{SCE}, we utilize the relationship between DIBL, SS, and I_{on}/I_{off} to derive at a value, which the smaller the better. In order to properly benchmark different transistor devices based on the intrinsic performance, the overdrive voltage, V_{ov} (= $V_{gs} - V_{t,sat}$), is considered in place of V_{gs} [8]. This rids the dependence of I_{on}/I_{off} on different $V_{t,sat}$ values. Therefore, I_{on} is taken when $V_{ov} = V_{ds} = V_{dd}$ (intrinsic on–state) and I_{off} is taken when $V_{ov} = 0$ V and $V_{ds} = V_{dd}$ (intrinsic off–state). Since I_{on}/I_{off} has an intrinsic state, V_{SCE} also has an intrinsic state.

The total gate capacitance in inversion, $C_{g,total}$, is measured at $V_{ov} = V_{ds} = V_{dd}$. Therefore, the intrinsic MOSFET delay, τ, is calculated from $C_{g,total}V_{dd}/I_{on}$ (or CV/I). Transconductance, g_m, is defined as dI_{ds}/dV_{gs}. Output resistance, r_o, is defined as $(dI_{ds}/dV_{ds})^{-1}$, which is the reciprocal value of the slope of the $I_{ds}-V_{ds}$ curves (output conductance). The intrinsic voltage gain, $g_m r_o$, is obtained by simply multiplying g_m and r_o. A V_{dd} of 0.8 V (operating voltage) is used in this work. To study the effects of the V_{dd} in the performance of transistors, a lower V_{dd} of 0.4 V (half of 0.8 V), is investigated. The 0.4 V is representative of the low supply voltage (or low V_{cc}). In the next section, ΔV_{DIBLSS}, I_{on}/I_{off}, V_{SCE}, $C_{g,total}$, CV/I, and $g_m r_o$ as functions of $V_{t,sat}$ are analyzed. Furthermore, state–of–the–art electron devices from [9]–[12] are also included in the comparison.

IV. RESULTS AND DISCUSSION

In Table 1, the four terminals: body (B), source (S), drain (D), and gate (G), are assigned four different voltages: V_b, V_s, V_d, and V_g, respectively. Since the V_b is set to ground (and $V_b = V_s$), the body effect is eliminated in this work. For simplicity, we use D and G to represent the V_{ds} and V_{gs}, respectively.

First, ΔV_{DIBLSS} as a function of $V_{t,sat}$ is examined (Fig. 2). For the four types of devices, $V_{t,sat}$ ranges from roughly 50 mV to 280 mV, but ΔV_{DIBLSS} remains similar. This indicates that these four devices have similar short–channel characteristics. In addition, ΔV_{DIBLSS} measured at $V_{dd} = 0.8$ V is only about 15 mV larger than ΔV_{DIBLSS} measured at $V_{dd} = 0.4$ V, indicating that the control of the channel potential barrier height remains dominated by the gate in comparison to the drain even with twice the supply voltage. It was mentioned in [6], [7] that a ΔV_{DIBLSS} value of equal to or smaller than 100 mV constitutes strong gate control over the channel [15]. For the devices mentioned in this work, ΔV_{DIBLSS} (measured at $V_{dd} = 0.8$ V) of about 100 mV indicates good short–channel behaviors. In addition, the ΔV_{DIBLSS} variations (about 40 mV) are due to the process variations in gate length, Fin height, Fin width, etc.

In normal on–state, I_{on} is equal to I_{ds} when $V_{gs} = V_{ds} = V_{dd}$, and in normal off–state, I_{off} is equal

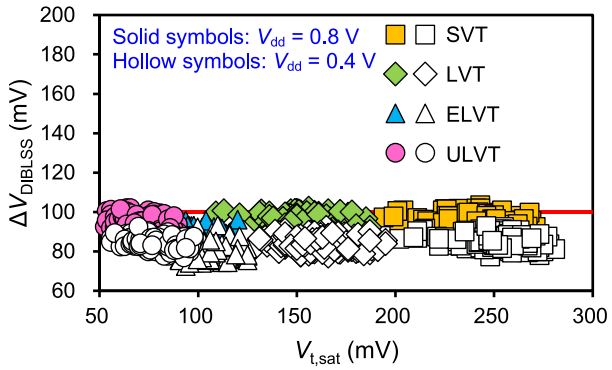
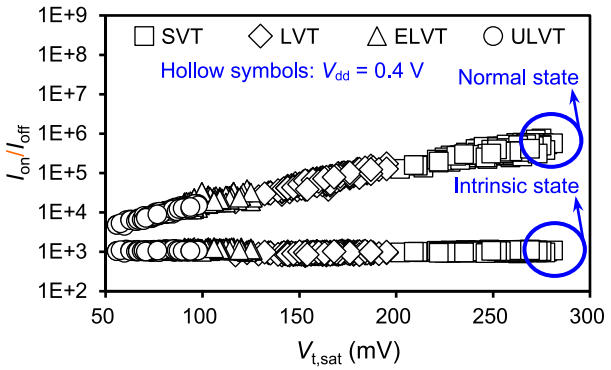
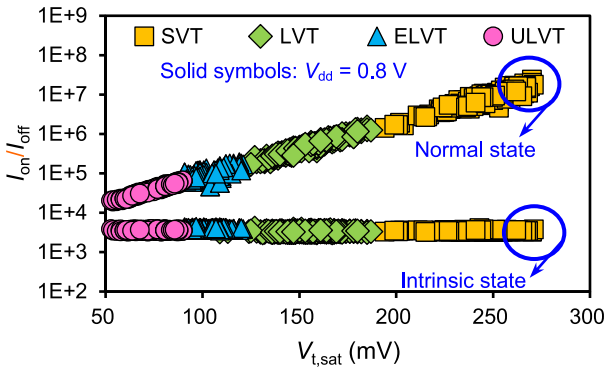


FIGURE 2. ΔV_{DIBLSS} versus $V_{t,sat}$. Hollow symbols: V_{dd} = 0.4 V. Solid symbols: V_{dd} = 0.8 V. L_g ranges from 16 to 20 nm. H_{fin} ranges from 43 to 44.5 nm. W_{fin} ranges from 11.4 to 12.1 nm. T_{ox} ranges from 1.82 to 2.03 nm. ΔV_{DIBLSS} remains almost unchanged due to strong gate control. A larger V_{dd} does not increase ΔV_{DIBLSS} significantly.



(a) V_{dd} = 0.4 V



(b) V_{dd} = 0.8 V

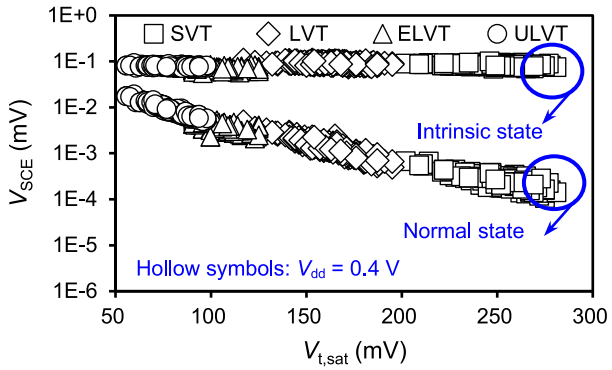
FIGURE 3. I_{on}/I_{off} versus $V_{t,sat}$. (a) Hollow symbols: V_{dd} = 0.4 V. (b) Solid symbols: V_{dd} = 0.8 V. L_g ranges from 16 to 20 nm. H_{fin} ranges from 43 to 44.5 nm. W_{fin} ranges from 11.4 to 12.1 nm. T_{ox} ranges from 1.82 to 2.03 nm. In normal state, on–state is when $I_{on} = I_{ds}$ and $V_{gs} = V_{ds} = V_{dd}$, and off–state is when $I_{off} = I_{ds}$, V_{gs} = 0 V, and $V_{ds} = V_{dd}$. In intrinsic state, on–state is when $I_{on} = I_{ds}$ and $V_{ov} = V_{ds} = V_{dd}$, and off–state is when $I_{off} = I_{ds}$, V_{ov} = 0 V, and $V_{ds} = V_{dd}$. As $V_{t,sat}$ increases, I_{on}/I_{off} increases. A larger V_{dd} results in a larger I_{on}/I_{off} value than a smaller V_{dd}.

to I_{ds} when $V_{gs} = 0$ V and $V_{ds} = V_{dd}$. In intrinsic on–state, I_{on} is equal to I_{ds} when $V_{ov} = V_{ds} = V_{dd}$, and in intrinsic off–state, I_{off} is equal to I_{ds} when $V_{ov} = 0$ V and $V_{ds} = V_{dd}$. The plots of I_{on}/I_{off} versus $V_{t,sat}$ measured at $V_{dd} = 0.4$ V and $V_{dd} = 0.8$ V are shown in Fig. 3. In this work, the gate–induced drain leakage (GIDL) current can be ignored because the I_{off} is dominated by the subthreshold leakage current. Therefore, the I_{off} of all the core devices is set by electrostatics. It is observed that I_{on}/I_{off} increases as $V_{t,sat}$ increases. Since both I_{on} and I_{off} decrease as $V_{t,sat}$ increases, it can be deducted at this point that the change in I_{on}/I_{off} due to $V_{t,sat}$ is dominated by the I_{off} term. When $V_{t,sat}$ is set very low, I_{off} becomes very large, and vice versa. Out of the four devices, ULVT devices provide the highest values of both I_{on} and I_{off}, and SVT devices provide the lowest values of both I_{on} and I_{off}. As a result of the dominating I_{off}, the highest I_{on}/I_{off} is observed for SVT devices, and the lowest I_{on}/I_{off} is observed for ULVT devices. This results in data clusters to have an obvious slope, indicating its dependence on $V_{t,sat}$ (normal state).

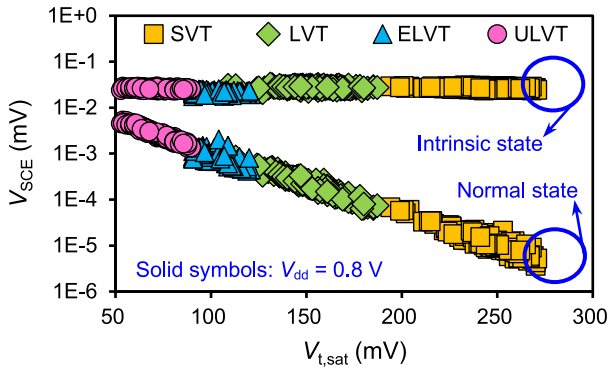
It can be noted that the devices have higher I_{on}/I_{off} at $V_{dd} = 0.8$ V (Fig. 3(b)) than at $V_{dd} = 0.4$ V (Fig. 3(a)). This reflects the increase of I_{on} with the increase of V_{dd}, which does not significantly increase the DIBL effect because of strong gate control. However, it is expected that at even higher level of V_{dd}, the DIBL effect will dominate, causing I_{on}/I_{off} to decrease [1], [2].

So far, the performances (I_{on}/I_{off}) of the devices have been observed to be largely dependent on $V_{t,sat}$. This is because V_{dd} and 0 V are simply applied to the gate terminal during the on state and off state, respectively. Based on the well–known expression of the saturation drive current, I_{on} [1], [2], it is inversely dependent on $V_{t,sat}$. For the off–state leakage current, I_{off}, it is also governed by $V_{t,sat}$. In order to eliminate the dependence of the I_{on}/I_{off} on $V_{t,sat}$, the intrinsic performance needs to be considered [8]. This can be extracted by varying the V_{ov}, rather than just the V_{gs} for both on and off states. For on state, V_{ov} is set to V_{dd}, and for off state, V_{ov} is set to 0 V. The result is also plotted in Fig. 3, where the data clusters are labeled with intrinsic state. The data for intrinsic I_{on}/I_{off} appear to be much less dependent on $V_{t,sat}$ (the slope is near zero), so devices with different supply voltages can be benchmarked regardless of $V_{t,sat}$. Thus, data points across different devices (categorized by different levels of $V_{t,sat}$) converge into a similar I_{on}/I_{off} level. This indicates that these devices have similar short–channel characteristics (ΔV_{DIBLSS}) shown in Fig. 2.

Since $V_{SCE} = \Delta V_{DIBLSS}/(I_{on}/I_{off})$, and there is a normal state and an intrinsic state for I_{on}/I_{off}, it is natural that there is a normal state and an intrinsic state for V_{SCE} as well (shown in Fig. 4). Note that each type of FinFET devices has different ΔV_{DIBLSS} and I_{on}/I_{off} (and thus different V_{SCE} values) depending on the $V_{t,sat}$. Since the I_{on}/I_{off} exists in the denominator of the equation for V_{SCE}, the slope that represents the normal state is flipped in Fig. 4 when compared to the slope in Fig. 3. The results for supply voltages of both 0.4 V and 0.8 V are shown.



(a) $V_{dd} = 0.4$ V



(b) $V_{dd} = 0.8$ V

FIGURE 4. V_{SCE} versus $V_{t,sat}$. (a) Hollow symbols: $V_{dd} = 0.4$ V. (b) Solid symbols: $V_{dd} = 0.8$ V. L_g ranges from 16 to 20 nm. H_{fin} ranges from 43 to 44.5 nm. W_{fin} ranges from 11.4 to 12.1 nm. T_{ox} ranges from 1.82 to 2.03 nm. Since there exists a normal state and an intrinsic state for I_{on}/I_{off}, there also exists a normal state and an intrinsic state for V_{SCE}, which is proportional to $1/(I_{on}/I_{off})$. In the normal state, the V_{SCE} is dependent of $V_{t,sat}$. In the intrinsic state, the V_{SCE} is independent of the $V_{t,sat}$.

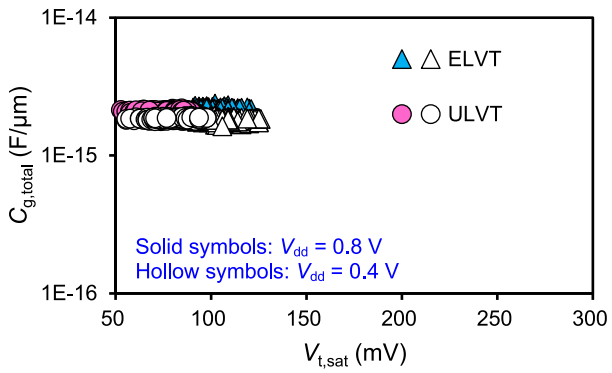


FIGURE 5. $C_{g,total}$ versus $V_{t,sat}$. Hollow symbols: $V_{dd} = 0.4$ V. Solid symbols: $V_{dd} = 0.8$ V. L_g ranges from 16 to 20 nm. H_{fin} ranges from 43 to 44.5 nm. W_{fin} ranges from 11.4 to 12.1 nm. T_{ox} ranges from 1.82 to 2.03 nm. Both devices have similar values of $C_{g,total}$.

When V_{ov} is considered (intrinsic state), the V_{SCE} for four different devices converge into the same order, much like the case of I_{on}/I_{off}. This is expected as the short–channel characteristics and the intrinsic I_{on}/I_{off} of all four devices

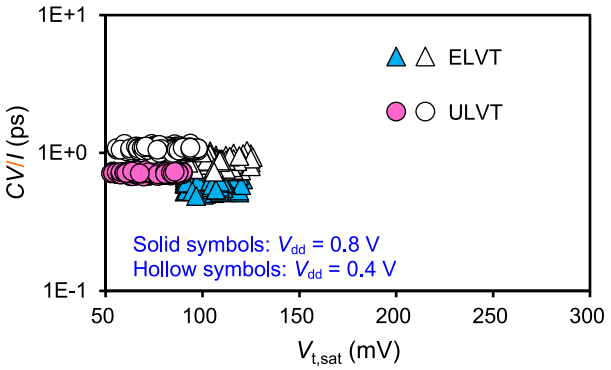


FIGURE 6. CV/I versus $V_{t,sat}$. Hollow symbols: $V_{dd} = 0.4$ V. Solid symbols: $V_{dd} = 0.8$ V. L_g ranges from 16 to 20 nm. H_{fin} ranges from 43 to 44.5 nm. W_{fin} ranges from 11.4 to 12.1 nm. T_{ox} ranges from 1.82 to 2.03 nm. A larger V_{dd} results in a lower CV/I because of the domination of the I_{on} value in the denominator. ELVT devices have a smaller CV/I than ULVT devices due to their smaller ΔV_{DIBLSS} values.

are supposed to be similar due to being fabricated with the same processes (see Figs. 2 and 3). Since the intrinsic state is independent of $V_{t,sat}$ and the slope is almost zero, both I_{on}/I_{off} (Fig. 3) and V_{SCE} (Fig. 4) appear flat.

The numerator of V_{SCE} is the ΔV_{DIBLSS}, which quantifies the short–channel behaviors, and the denominator is I_{on}/I_{off}, which quantifies the transistor performance. Thus, having a relatively small V_{SCE} indicates that gate control over the channel is not significantly affected by the change in V_{dd}. Transistors with V_{SCE} of smaller than 0.1 mV when V_{ov} is considered, as shown in the data in Fig. 4, indicate good short–channel behavior.

Since the capacitor test structure is laid out in the ELVT and ULVT devices, only these two devices will be compared. Fig. 5 shows a plot of $C_{g,total}$ versus $V_{t,sat}$. It is observed that the consideration of V_{ov} renders the $C_{g,total}$ values of the two devices almost equal in magnitude. Like for V_{SCE}, this indicates that devices with different $V_{t,sat}$ intrinsically have similar $C_{g,total}$ values. If V_{gs} was considered, $C_{g,total}$ would increase with decreasing $V_{t,sat}$ like V_{SCE} does. This explains why CV/I values converge at similar levels as shown in Fig. 6. In the case of a larger V_{dd} of 0.8 V, even though $C_{g,total}$ is slightly larger than the $V_{dd} = 0.4$ V case, a smaller CV/I is still obtained due to the domination of the increase of the denominator, I_{on}. Furthermore, ELVT devices have a smaller CV/I than ULVT devices because of their smaller ΔV_{DIBLSS} values, as shown in Fig. 2. Although the capacitor test structures of SVT and LVT devices are not included, their $C_{g,total}$ behaviors are expected to be similar to the ELVT and ULVT devices. In other words, the CV/I of SVT and LVT devices will be similar to the ULVT devices due to their similar ΔV_{DIBLSS}.

Fig. 7 shows $g_m r_o$ versus $V_{t,sat}$ measured at $V_{dd} = 0.4$ V and $V_{dd} = 0.8$ V. $g_m r_o$ remains consistent for all devices, independent of $V_{t,sat}$. The similarity in the behaviors between ΔV_{DIBLSS} and $g_m r_o$ is observed as $V_{t,sat}$ varies. Increase in DIBL is related to the reduction of $V_{t,sat}$, so small DIBL

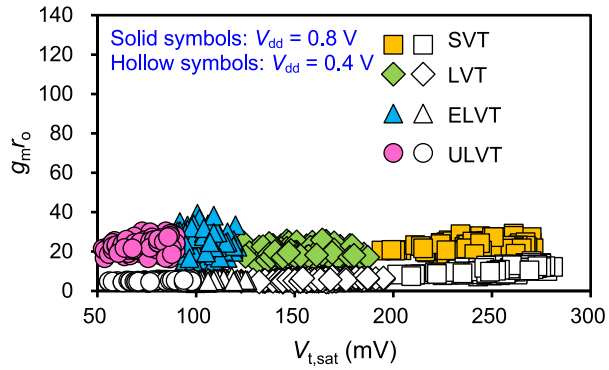


FIGURE 7. $g_m r_o$ versus $V_{t,sat}$. Hollow symbols: V_{dd} = 0.4 V. Solid symbols: V_{dd} = 0.8 V. L_g ranges from 16 to 20 nm. H_{fin} ranges from 43 to 44.5 nm. W_{fin} ranges from 11.4 to 12.1 nm. T_{ox} ranges from 1.82 to 2.03 nm. A larger $g_m r_o$ is observed due to a larger V_{dd}.

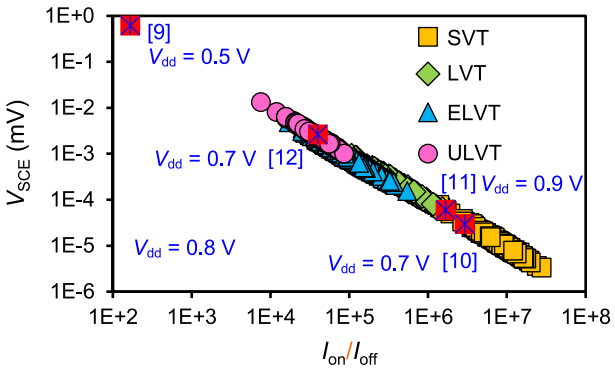


FIGURE 8. V_{SCE} versus I_{on}/I_{off}. V_{dd} = 0.8 V. L_g ranges from 16 to 20 nm. H_{fin} ranges from 43 to 44.5 nm. W_{fin} ranges from 11.4 to 12.1 nm. T_{ox} ranges from 1.82 to 2.03 nm. The slopes for all devices are very similar.

indicates a high r_o [7]. SS is given by the V_{gs} required to increase the I_{ds} by one order of magnitude. g_m is given by the change in I_{ds} divided by the change in V_{gs}. Thus, a small SS and a large g_m are desirable. Since DIBL and SS are related to $g_m r_o$, ΔV_{DIBLSS} (Fig. 2) can be used to predict the trend of $g_m r_o$. Also, it is shown in Fig. 3 and Fig. 4 that V_{ov} can eliminate the dependence of I_{on}/I_{off} on $V_{t,sat}$. The intrinsic performance obtained as a result will follow the same trend as $g_m r_o$ as well. It can be observed in Fig. 7 that increasing V_{dd} also increases $g_m r_o$.

The performances of different state–of–the–art electron devices from [9]–[12] are compared with the four devices mentioned in this work (at $V_{dd} = 0.8$ V) in Fig. 8. The V_{SCE} versus I_{on}/I_{off} plot shows that V_{SCE} decreases as I_{on}/I_{off} increases. Interestingly, the devices presented in [9]–[12] follow the same slope. This is a good indication that the gate control is sufficiently strong for all the devices shown in Fig. 8, where $V_{t,sat}$ strongly dominates I_{on}/I_{off} and thus determines the V_{SCE}. If an advanced transistor has a small ΔV_{DIBLSS} value (about 100 mV), the value of V_{SCE} will be similar as long as the devices have similar V_t values. In addition, V_{SCE} values converge into the same order when V_{ov} is used to minimize the dependence on $V_{t,sat}$.

V. CONCLUSION

The short–channel behaviors of n–FinFETs at $V_{dd} = 0.4$ V and $V_{dd} = 0.8$ V have been demonstrated. ΔV_{DIBLSS} of 100 mV indicates that the gate control is strong. For a transistor with a larger V_{dd}, as long as its ΔV_{DIBLSS} is smaller than (or equal to) 100 mV, its I_{on}/I_{off} will be larger than that of a transistor with a smaller V_{dd}. In this work, the increase of I_{on}/I_{off} with increasing. V_{dd} is observed. With good control for the SCE, I_{on}/I_{off} (and $g_m r_o$) can be increased by using a larger V_{dd}. V_{SCE} and CV/I in turn decrease for larger V_{dd}. The device behaviors of standard–V_t (SVT), low–V_t (LVT), extreme–low–V_t (ELVT), and ultra–low–V_t (ULVT) are presented with consideration of the on and off voltage states of the overdrive voltage, which disregards the effect of the saturation threshold voltage, revealing the intrinsic performance of the FinFETs. With the device intrinsic characteristics revealed, the performances of devices with different threshold voltage values can be directly compared.

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YI-CHUEN ENG (Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from National Sun Yat-sen University, Kaohsiung, Taiwan, in 2005 and 2012, respectively. In 2012, he joined United Microelectronics Corporation, Tainan, Taiwan, where he has been engaged in the field of semiconductor device physics, simulation, and reliability of FinFET, and embedded high–voltage devices.

LUKE HU (Member, IEEE) was born in Tainan, Taiwan, in 1989. He received the B.Eng. and M.Eng. degrees in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 2011 and 2013, respectively, specializing in photonics and semiconductor physics. He is currently with the Research and Development Division, United Microelectronics Corporation, Tainan, where he has been engaged in the development and qualification of the fabrication, device physics, simulation, and reliability of 3-D IC processes.

TZU-FENG CHANG received the M.S. degree in electrical engineering from National Sun Yat-sen University, Kaohsiung, Taiwan, in 2010. From 2011 to 2014, he was a Product Engineer with the Department of Technology Development and Product, Rexchip (Micron), Taichung, Taiwan. He is currently with the Research and Development Division, United Microelectronics Corporation, Tainan, Taiwan. His research interests include semiconductor device physics and SRAM cell operation.

CHIH-YI WANG received the Ph.D. degree in physics from National Taiwan University, Taipei, Taiwan, in 2015. In 2016, he joined United Microelectronics Corporation, Tainan, Taiwan, where he has been engaged in the field of semiconductor device physics and new process improvement.

STEVEN HSU received the M.S. degree in electrical engineering from National Chiao Tung University, Hsinchu, Taiwan. He was with United Microelectronics Corporation (UMC), Hsinchu, for over 21 years, where he has had experience with semiconductor fabrication from the 0.18 μm architecture all the way to the 14 nm architecture. He is currently the Vice President of the Technology Development Division, UMC, where he is in charge of logic and specialty technology platform development.

OSBERT CHENG (Member, IEEE) received the M.S. degree from National Tsing Hua University, Hsinchu, Taiwan, and the Ph.D. degree in electronics engineering from National Chiao Tung University, Hsinchu.

He is currently the Vice President of the Device Technology Development & Design Division, United Microelectronics Corporation, Tainan, Taiwan. He has been involved in developing the foundry platform with over eight technology nodes. He is currently leading the research of advanced devices, SRAM, mixed–signal, reliability, TCAD, and Model in the Research and Development Team. He is currently a member of the Technical Program Committee of IEEE Symposium on VLSI Technology.

CHIEN-TING LIN was born in Kaohsiung, Taiwan, in 1968. He received the Ph.D. degree in electronics engineering from National Cheng Kung University, Tainan, Taiwan, in 2007. He has been with the Central Research and Development Division, United Microelectronics Corporation, Hsinchu, Taiwan, for over 23 years, where he is currently the Director of the Technology Development Division. He leads the FinFET, 3-D IC, embedded high–voltage devices, and magnetic random-access memory process development in the Research and Development Team.

YU-SHIANG LIN received the M.S. degree in chemical engineering from National Taiwan University, Taipei, Taiwan. He was with United Microelectronics Corporation (UMC), Hsinchu, Taiwan, for over 20 years, where he participated in the CMOS process integration development from 0.18 μm to 14 nm architectures. He is currently the Deputy Director of the Technology Development Division, UMC, where he is in charge of the FinFET and embedded high-voltage devices process development.

ZEN-JAY TSAI received the M.S. degree from the Institute of Electro-Optical Science and Engineering, National Cheng Kung University, Tainan, Taiwan. In 2007, she joined United Microelectronics Corporation, Tainan, where she was responsible for the development process of high-κ and metal gate integration and is currently the Deputy Department Manager focusing on the FinFET and embedded high-voltage devices process development.

CHIH-WEI YANG was born in Kaohsiung, Taiwan. He received the B.S. and Ph.D. degrees in electrical engineering from National Cheng Kung University, Tainan, Taiwan. In 2003, he joined United Microelectronics Corporation, Hsinchu, Taiwan, where he was responsible for the development process of high-κ and metal gate integration as well as reliability characterization for the 28 nm process and is currently a Section Manager focusing on the FinFET process development.

JIM LU received the M.S. degree from the Institute of Microelectronics Engineering, National Cheng Kung University, Tainan, Taiwan. In 2013, he joined United Microelectronics Corporation, Tainan, where he was responsible for the development process of high-κ and metal gate integration. He is currently a Section Manager focusing on the FinFET and embedded high-voltage devices process development.

STEVE YI-WEN CHEN received the M.S. and Ph.D. degrees in materials science and engineering from National Tsing Hua University, Hsinchu, Taiwan. He has been in the United Microelectronics Corporation for over 14 years, where he participated in the CMOS process integration development from 28-nm HKMG to 14-nm FinFET process development in the Research and Development Team. He is currently a Section Manager in charge of the embedded high-voltage devices process development.