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Transparent Floating Gate Memory Based on ZnO Thin Film Transistor With Controllable Memory Window

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ABSTRACT The transparent floating gate memory based on zinc oxide (ZnO) thin film transistors (TFTs) was fabricated by using one-step atom layer deposition of aluminia tunneling and ZnO charge-trap layers. Free electrons trapping mechanism of this memory device is proposed after systematical investigation of gate voltage scanning and thickness of the trapping layer. Furthermore, the relationship between the geometrical size of the charge-trapping layer and the memory window is explored. The devices with different memory windows can be controlled simply by designing the area of their trapping layer without any external process, which is much beneficial to the low cost process fabrication of the memory array and driving circuits, since the memory and switch/digital transistors can be fabricated at the same time. Finally, the presented TFT memory exhibits a maximum memory window of 15 V, excellent fatigue and retention properties more than 30,000 s without any charge loss. The transparent floating gate memory with the ZnO charge-trap layer has great potential for application of 3D, transparent or multi-value memory.

INDEX TERMS Zinc oxide, floating gate memory, thin film transistor, charge-trap layer, memory window.

I. INTRODUCTION

Memory is one of the five basic building blocks of computer hardware. Among them, flash memory has broad application due to its non-volatile nature and ease of erasing. So far, silicon- oxygen-nitrogen-oxygen-silicon (SONOS) type structure floating gate memory is the most common choice [1]–[4]. As continuous scaling down of the feature size of transistors, the physical limitation will appear in the last few years. The density of the SONOS type flash memory will touch the ceiling. In the case, developing 3D architecture of novel memory or computing-in-memory are the trends for the future non-volatile memory. Meanwhile, metal-oxide thin film transistors (TFTs) have great potential to be applied into the 3D non-volatile memory due to their low-temperature process compatibility, stable and better electrical performance [5]. Charge trapping memories based on metal-oxide TFTs have gradually been favored and researched [6], [7]. It is most important to choose the appropriate material as the charge-trap layer (CTL). In many works, they prefer to use metal nanoparticles as the charge-trap layer of the non-volatile memory [8]–[10], such as Ag, Ni and Pt nanocrystals. However, these devices are still far away from practical application because of their poor process compatibility, small memory window and slow programming/erasing (P/E) speed. On the other hand, oxide charge trapping materials, including ZnO [11], indium-gallium-zinc-oxide (IGZO) [12], Zn-doped Al_2O_3 [13], $SmTiO_3$ [14] and TiAlO [15], have been studied due to the good compatibility in metal oxide TFTs. Especially, the devices with ZnO charge trapping layer exhibit excellent memory characteristics with memory window of 20 V and programming/erasing speed of 500 ms, since ZnO thin film has a lot of oxygen

vacancies that can capture a large number of electrons, resulting in a large memory window [7]. Therefore, it is considered as an ideal material for the charge trapping layer [7], [16]. In these works, most devices use IGZO thin film as a channel layer and ZnO thin film as a charge-trap layer. Generally, IGZO films are deposited using RF magnetron sputtering, while ZnO films are deposited by atomic layer deposition (ALD). Using different equipment and processes not only increases the cost of the device, but also more likely to introduce impurities to affect the device performance. In order to obtain ultra-thin, high quality and good uniformity tunneling layer, ALD is considered as one of the best deposition techniques. At the same time, ALD deposition of the thin charge-trap layer can effectively reduce the damage of the tunneling or blocking layers. Oruc, *et al.* proposed the floating gate memory TFT with stacked Al_2O_3 blocking/ZnO charge trapping/Al_2O_3 tunneling/ZnO channel layers fabricated in a single ALD step [11]. The window memory of 2.35 V has been realized for the ALD ZnO TFTs, but the systematical measurement of the memory characteristics is lacking. Our previous works revealed good stability and uniformity of the ALD ZnO TFTs [17], which can be applied in many fields [18], such as radio identification tag (RFID) [19] and fingerprint sensor [20]. In the application of the low-cost transparent RFID tags, the absence of oxide TFT based non-volatile random access memory (RAM) becomes the bottleneck.

In this work, we have fabricated a transparent floating gate memory using ZnO as channel and charge-trap layers all in ALD on glass substrate. The effect of the process parameters and geometry size of the charge-trap ZnO TFTs on the memory properties is investigated systematically. The annealing process and the thickness of the charge trapping layers are optimized and analyzed to improve the device performance, and their charge trapping mechanism has been discussed. The proposed transparent ZnO TFT based non-volatile memory exhibits fast P/E speeds, wide and controllable memory window. Furthermore, the fatigue and retention performances of the memory device are also checked.

II. EXPERIMENTAL

The cross-section of the top-gate ZnO floating gate TFT fabricated on glass in this study is illustrated in Fig. 1(a). The fabrication process started from the deposition of a 200 nm thick indium-tin-oxide (ITO) layer using DC sputtering. This ITO layer was patterned by wet etching as source/drain (S/D) electrodes. Then, a 20 nm thick ZnO channel layer was deposited by ALD and annealed at 400 °C for 5 mins in O_2 ambience. Next, a 2 nm thick Al_2O_3 tunneling layer, a 2 nm (10nm or 20 nm) thick ZnO charge-trap layer and a 8 nm thick Al_2O_3 protection layer were deposited by ALD continuously in one-time without opening chamber. The stacked ZnO/Al_2O_3/ ZnO/Al_2O_3 layers were patterned in dilute HF solution and annealed at 400 °C for 5 mins in O_2 ambience. After a 20 nm thick Al_2O_3

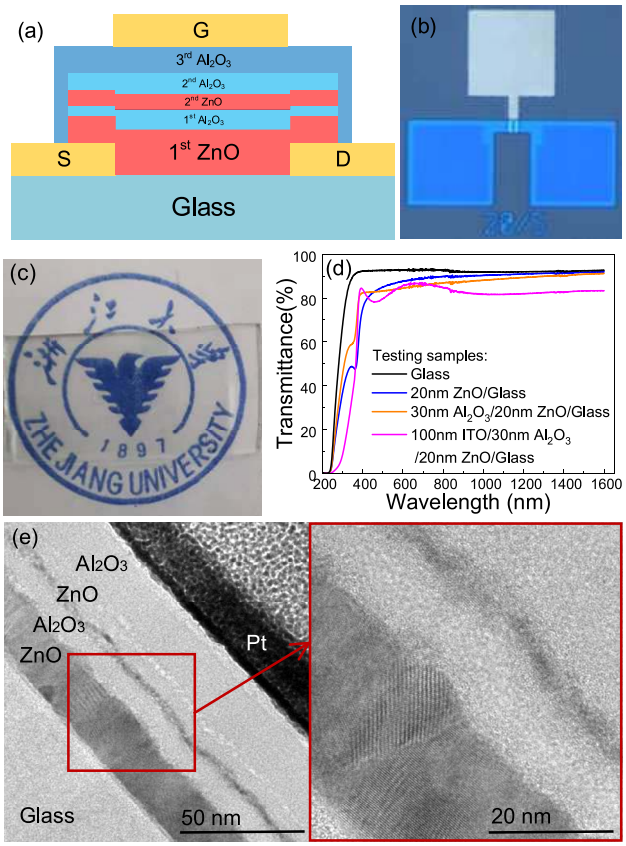

FIGURE 1. (a) Cross sectional schematic of the ZnO floating gate TFT, (b) the optical microscope image of the transparent memory devices, (c) the optical photo of the memory device, (d) the transmittance of different thin film layers, (e) the cross sectional TEM image of the floating gate structure Al_2O_3/ZnO/Al_2O_3/ZnO/glass.

layer was deposited by ALD as the gate insulator, the gate electrode of a 100 nm thick ITO layer was formed by sputtering and lift-off. Fig. 1(b) shows the microscope image of the floating gate memory device. In present device, all of the thin film materials such as ZnO, Al_2O_3, ITO and glass substrate are transparent. Hence, a fully transparent flash memory is fabricated and demonstrated as shown in Fig. 1(c). Fig. 1(d) shows the transmission spectra of several stacked layers. All measured samples exhibit good transparency with an average transmittance higher than 84% in the visible wavelength range. If the transmittance loss caused by glass is ignored, these layers even have a transmittance of more than 90%. The current-voltage characteristics (I–V) and cross-section of the device are tested by a semiconductor characterization system (Keysight B1500A) and a transmission electron microscope (TEM, FEI Tecnai G2 F20 S-TWIN).

III. RESULTS AND DISCUSSION

Fig. 1(e) shows the TEM image of the flash memory device including the channel layer, the tunneling layer, the charge-trap layer and the protection layer. The dark and light gray layers are ZnO and Al_2O_3, respectively. It is clear seen from

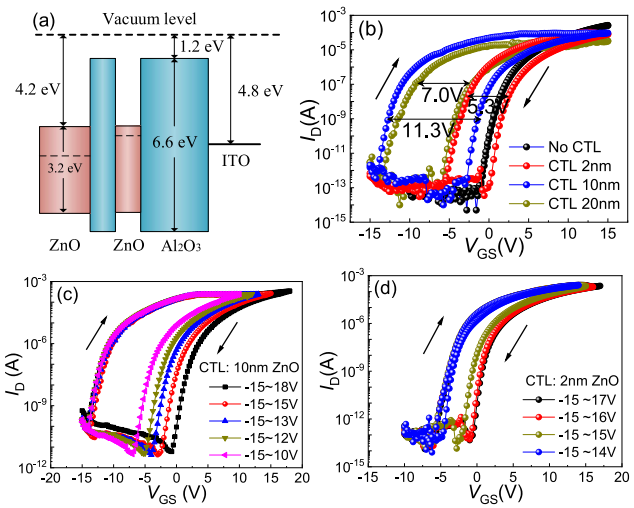

FIGURE 2. **(a) The flat band diagrams of devices, (b) the forward and backward sweeping transfer curves of the floating gate TFTs with different thickness of the trapping ZnO layers and the control device, (c) the transfer characteristics of the floating gate TFTs with 10nm thick trapping layer double swept from −15V to different positive gate voltage, (d) the saturated memory window with the device of 2nm thick trapping layer. All of the transfer curves measured under V_{DS} = 5V.**

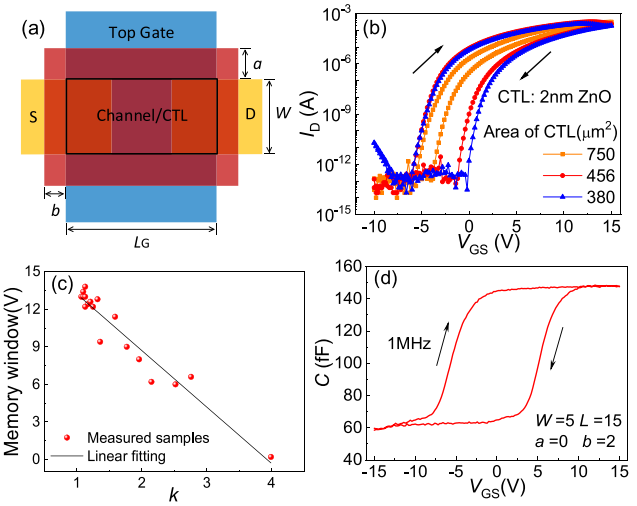

FIGURE 3. **(a) The layout diagram of the memory device, (b) The I–V curves of the floating gate TFTs with different areas of the 2nm thick charge-trap layer, measured under V_{DS} = 5 V, (c) The relationship between the memory window and the k values of the 10nm thick charge-trap layer, (d) The C-V characteristics of the flash memory.**

the enlarged image that the Al_2O_3 thin film is amorphous and the ZnO thin film is poly-crystal, even the 2 nm thick ZnO thin film still exhibits micro-crystal property.

Fig. 2(a) shows the energy band diagram of the memory. The different Fermi levels of the ZnO layers are caused by their different annealing conditions, including annealing temperature, time and atmosphere. Since the ZnO channel layer is annealed and exposed directly to O_2 ambience, the thin film exhibits almost insulating performance [17]. While the ZnO trapping layer is still conductive because of the coverage of the oxide layers in the following heat treatment. The more conductive ZnO trapping layer can capture or provide free electrons for programming or erasing operation [5]. Fig. 2(b) shows the obvious hysteresis *I-V* behaviors of the ZnO TFTs with width/length ratio of 5 μm/5 μm under the sweeping gate voltage from −15 V to +15 V. It is found from the figure that the memory windows of the devices with different thicknesses (2nm, 10 nm and 20 nm) of the ZnO charge-trap layers are measured as 5.7 V, 11.3 V and 7 V, respectively. Compared to the control device without ZnO charge-trap layer [5], the large clockwise hysteresis has been realized, since the tunneling electrons are captured by the ZnO charge-trap layer that has many defects, such as oxygen vacancies and grain boundaries. Unlike the silicon nitride in the SONOS structure memory, the ALD ZnO thin film is conductive and hence provides plentiful free electrons. When the large negative voltage is applied on the gate electrode, these free electrons in trapping layer will be pushed through the tunneling layer to channel. The reserved positive charge results in larger negative shift of the threshold voltage for the devices with 10 nm and 20 nm thick ZnO trapping layers. On the contrary, the device with ultra-thin trapping layer (2 nm) shows smaller negative shift of the threshold voltage due to its fewer numbers of charge carriers in the limited physical space. Owing to the thicker ZnO trapping layers (20 nm) will weaken the effect of gate electrical field on the trapping and the channel layers, this device exhibits smaller memory window and on-current than that of device with 10 nm trapping layer. Here, we choose the 10nm thick ZnO thin film as the optimized charge trapping layer of the memory device. Fig. 2(c) shows the hysteresis *I-V* curves of the device with 10 nm trapping layer measured under the same negative (−15 V) and different positive voltage from 10 V to 18 V. It is noted that the memory window increases as the programming voltage increases. Eventually, the bigger memory window of 15 V is realized at the programming voltage of 18 V. However, it is not the biggest memory window, since the number of the electrons trapped from channel didn't achieve the saturation state for the 10 nm thick trapping layer. Conversely, as shown in Fig. 2(d), the positive shift of the threshold voltage will reach a saturated point for the device with 2 nm trapping layer, when the programming voltage is larger than 16 V. The case proves that the maximal number of the trapped electrons depends on the thickness of the storage layer. If the tunneling electrons exceed the position of the fixed positive charge provided in the trapping layer, internal electrical field will be built to prevent the electron tunneling from channel to trapping layer, resulting in a dynamic balance and limited positive shift.

Fig. 3 (a) shows the layout of our device, where the red, yellow and blue parts represent ZnO channel/trapping layer, S/D and top gate electrode, respectively. The black frame labeled in the red layer represents the effective area of excluding or attracting electrons from the trapping layer to the channel layer. This area equals the device width (*W*)

times the gate length (L_G). The margin of the active layer (a and b) is reserved for the process compatibility of the mis-alignment of photolithography. In order to research the relationship between the area of the trapping layer and the memory window, the devices with the same (W, L_G) but different size of (a, b) were tested as illustrated in Fig. 3 (b). As increment of the area of the trapping layers, the memory windows decrease from 5.6 V to 1.6 V. This is possibility explained by that the same electrons input from the effective area are distributed to the whole trapping layer due to the conductivity of the ZnO thin film. The larger area of the trapping layer, the smaller charge density and hence smaller memory window. In other words, the different margin area of the CTL can be equivalent to one electrode plate of different parasitic capacitors. The input electrons will be used to charge the parasitic capacitors, resulting in varying degrees of reduction of the charge density in the whole CTL. A batch of devices with different area of the trapping layers is measured to analyze this phenomenon quantitatively. All of the physical parameters are normalized to a factor of k that represents the ratio of the total area to the effective area (black frame in Fig. 3 (a)) of the trapping layer: $k = (W + 2a)\ (L + 2b)/WL_G$. Fig. 3(c) concludes the effect of the factor k on the memory window (V_{th}) for various sizes of the devices. It is found that the memory windows of these devices and the factor k basically match the linear relationship. Therefore, these data are fitted linearly to an empirical formula as follows,

$$\Delta V_{th} = -4.52k + 17.74 \tag{1}$$

In the fitting results, the standard deviation of the slope and the intercept are 0.307 and 0.558, respectively. The fitting formula is consistent well with the actual measurement in general. From the equation, we can obtain the devices with different memory windows by controlling the area ratio of the trapping layer precisely. This linear relationship is still reasonable for devices with different thicknesses of charge-trapping layers, and may build the theoretical foundation for many novel designs. For example, in the NAND structure flash memory, the switch or digital transistor without hysteresis and the memory transistor with large hysteresis could be fabricated in the same process, just by setting the k value to realize different functions. Furtherly, the capacitance-voltage (C-V) characteristics of the device with 10 nm thick ZnO trapping layer is tested as shown in Fig. 3(d). Through the C-V behaviors of the device, we can roughly calculate the defect state density of the zinc oxide charge trapping layer according to the following equation [21],

$$N_{CTL} = \frac{1}{qA}\int C(V)dV \tag{2}$$

The defect density of 5.8×10^{12} cm^{-2} is calculated. It not only includes the defects in the ZnO trapping layer, but also includes the defects in the Al_2O_3 tunneling layer and the interface between different thin films. But it is no doubt that the number of defects in the ZnO trapping layer is much larger than that in the others.

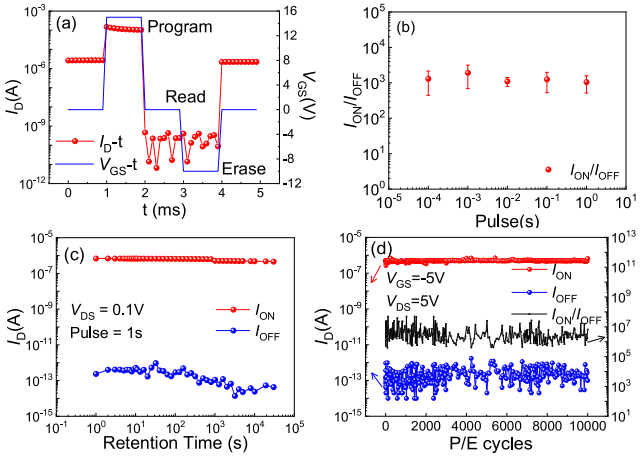

FIGURE 4. (a) The P/E and reading operation measurement of the TFT memory. The blue line represents the gate voltage wave for program, read and erase. The red point line represents the sampled drain current under these operation. (b) The relationship between I_{ON}/I_{OFF} ratio and the programming/erasing pulse time. (c) The retention characteristics of the memory device measured for 30000 s at room temperature. (d) The fatigue characteristics of the device with repeat operating test for 10,000 cycles.

In order to verify the memory function of the device in practical applications, the P/E operations of the floating gate TFTs were tested by the semiconductor analyzer. Fig. 4 shows the sampling drain current (I_D) varied with the gate voltage of programming (+15 V), erasing (−10 V) and reading operation (0V). The current ratio (I_{ON}/I_{OFF}) is proportional to the memory window of the flash device. The pulse widths of the P/E voltages were set as 1ms. Here, the normal programming and erasing functions of the flash device are realized. The stored data can be read under low S/D voltage (V_{DS} = 0.1 V), which will reduce the energy consumption during the operation. The P/E speed of the flash memory is one of the most significant performances in the assessment. As shown in Fig. 4(b), the pulse widths of the P/E voltages are varied from 1s to 100 μs. It is found that the P/E operation can be achieved and the reading current ratio is unchanged even if the pulse time of 100 s is applied. In theory, this device can be operated in faster speed if there is not limitation of our testing condition.

Another important character of the nonvolatile memory is how long its data can be retained after power down. Therefore, the retention property of the device is evaluated in Fig. 4(c). After the device programmed or erased with gate voltage of −15V or +15 V, the drain current is tested at the given time points when the reading gate and S/D voltages are set as 0 V and 0.1 V, respectively. The device is continuously measured for more than 10 hours at room temperature and in normal humidity environment. As a result, no obvious changes of the reading current for programming or erasing states are found over a period of 30,000 s. It is an excellent result that exceeds many reported

TABLE 1. Characteristics of various floating gate memories.

Channel/tunneling layer/CTL	P/E voltage	P/E time	Memory window	Retention (charge loss)	P/E cycles	Ref
$ZnO/Al_2O_3/ZnO$	± 15 V	100 μs	11.3 V	10^4 s (~0)	10^4	This work
$ZnO/Al_2O_3/ZnO$	± 10 V	N/A	2.35 V	N/A	N/A	[11]
α-$IGZO/Al_2O_3/TiAlO$	± 16 V	100 ms	5.74 V	10^4 s (~15%)	N/A	[15]
$IGZO/Al_2O_3/IGZO$	± 11 V	100 ms	3.5 V	10^4 s (~50%)	N/A	[23]
$IGZO/Al_2O_3/(HfO_2/ZnO)$	± 25 V	500 μs	25 V	10^4 s (~60%)	N/A	[12]
$IGZO/Al_2O_3/IGZO$	± 20 V	1 ms	6.6 V	10^4 s (~50%)	N/A	[24]
$IGZO/SiO_2/Sm_2O_3$	± 15 V	100 ms	2.7 V	10^5 s (~15%)	10^4	[14]
IGZO/Al2O3/ZAO	+12/-20 V	1 ms	3.21 V	10^4 s (>75%)	N/A	[13]
SONOS	± 7.5 V	100 ms	2 V	10^6 s (~35%)	10^5	[2]
SiO_2/Au-NCs/IGZO	± 35 V	3/25 s	4.7 V	N/A	1050	[25]
IGZO/HfLaO/HfON	± 8 V	1/0.1 ms	1.2 V	10^5 s (>60%)	10^2	[26]
p-Si/SiO_2/IGZO	+18/-23 V	10/100 ms	5.6 V	N/A	N/A	[27]
IGZO/ Al_2O_3/ZnO	± 20 V	N/A	18.2 V	N/A	N/A	[28]

researches [13], [22]. This may be due to the formation of the Al_2O_3 tunneling and the ZnO trapping layers in one-time ALD deposition at 200 °C and etching together. High qualitative tunneling layer ensures that the charges are trapped in the trapping layer for long time. Moreover, the fatigue characteristics of the memory device are also tested as shown in Fig. 4(d). After 10,000 cycles of programming-reading-erasing- reading operation, the reading drain current is still unchanged, demonstrating good reliability of the memory device. Table 1 summarizes the characteristics of various charge trapping memory devices. Compared with the published works, this fabricated device exhibits excellent comprehensive performance.

IV. CONCLUSION

We propose a transparent floating gate memory based on ZnO TFT using one-time ALD growth of Al_2O_3 and ZnO as the tunneling layer and the trapping layer. This approach minimizes the effects of external environment on the device during the fabrication process. The particular mechanism of the charge trapping/detrapping of the floating ZnO layer is deeply analyzed. We also investigate the relationship between the area of the charge-trap layer and the memory window. The linear empirical expression has been extracted for reference of controlling the memory window. When the programming and the erasing voltages are set as +18 V and −15 V, respectively, the optimized memory TFTs with a 10 nm thick ZnO trapping layer exhibit outstanding characteristics, such as large memory window of 15V and fast P/E speed of <100 μs, almost unchanged reading current ratio after long retention time more than 30,000 seconds and 10,000 times cycling P/E operation. It is believed that this device will play an important role in the future transparent or flexible circuit application.

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