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Self-Aligned Transparent-Gate ITO/Germanium Nanospheres/SiO_2/SiGe-Nanosheets photoMOSFETs on Silicon Nitride Platform

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ABSTRACT We report experimental fabrication and characterization of photoMOSFETs with self-aligned gate-stacking heterostructures of indium-tin-oxide (ITO)/Ge nanospheres/SiO_2-shell/$Si_{1-x}Ge_x$-nanosheets. Array of Ge-nanosphere/SiO_2-shell/SiGe-nanosheet heterostructures was created in a self-organized, CMOS approach using the thermal oxidation of lithographically-patterned poly-$Si_{0.85}Ge_{0.15}$ nanopillars over buffer layers of Si_3N_4 on top of SOI substrates. With a polysilicon dummy-gate, source and drain self-align with the transparent ITO gate using a replacement-metal-gate process. Very high photocurrent gain, large photoresponsivity, as well as improved input capacitance and 3dB frequency were experimentally achievable in our photoMOSFETs. The pivotal roles of Ge-optical gate and SiGe-channel for large photoresponsivity and current gains were analyzed via numerical simulation.

INDEX TERMS photoMOSEFT, germanium nanosphere, SiGe, self-organization, photoconductive, photovoltaic.

I. INTRODUCTION

The gigantic data connectivity is strongly driven by wide-ranging applications from social networks, streaming media to the connected devices within the "Internet of Things". The data-intensive processing comes at a cost of energy dissipation and faces major challenges of bandwidth-latency. It is difficult to solve all these issues using conventional electrical interconnect that requires metal-wires to transfer electronic data, taking both energy and time.

Si photonic integrated circuits (PICs) are great enablers for 5G networking and data centric applications due to their great promise of high-speed and low-power interconnects. In addition to the holy-grail of light sources in Si PICs, high-performance and energy-efficient receiver circuitry is particularly important for Si optical interconnect [1]–[3]. While high-speed germanium (Ge) PIN photodiodes have been demonstrated on silicon-on-insulator (SOI) [4]–[6] and Si_3N_4 platform [7], high dark current and low photoresponsivity remain to be improved. Another technical challenge for Ge photodiodes lies in their large form factor, leading to not only excess energy dissipation due to large parasitic capacitance, but also difficulties in the integration of Ge photodetectors with CMOS amplifiers due to the incompatibility in physical-sizes.

A phototransistor (PT) is a unique phototransducer that simultaneously conducts photoelectric conversion via photodiodes and electrical amplification via transistors within a single device, minimizing wiring resistance and capacitance between photodiodes and electrical amplifiers, noise increment, and energy dissipation. Several Ge-based phototransistors have been proposed, including heterojunction bipolar transistors, [8], [9] photoMOSFETs, [10] PIN phototransistors, [11] and tunneling phototransistor [12]–[14]. However, many works simply focus on the device structure design and performance evaluation using numerical simulation [12]–[16]. This is because experimental implementation of Ge phototransistors involves exquisite Ge epitaxial growth, source/drain (S/D) engineering, and transparent metal-gate

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fabrication, which require ingenious co-design of device structure and advanced process integration.

Our previous reports have demonstrated the formation of self-organized heterostructures of Ge nanospheres/SiO_2/$Si_{1-x}Ge_x$ nanosheets using the thermal oxidation of poly-$Si_{0.85}Ge_{0.15}$ pillars over buffer layers of Si_3N_4/Si [17]–[21]. Based on the self-organized gate-stacking heterostructures, we have fabricated photoMOSFETs with non-self-aligned ITO gates [22] and demonstrated low dark current and high photoresponsivity simultaneously achievable. Both Ge nanospheres within gate-dielectrics and $Si_{1-x}Ge_x$ nanosheets on top of Si surface actively absorb light, effectively modulate surface potential, and efficiently contribute photocarriers within the channel [22]. The appeal of our proposed photoMOSFETs approach lies in the engineering advantages of controllably forming gate-stacking heterostructures [17]–[21] in terms of the Ge nanosphere's size and the Ge content of $Si_{1-x}Ge_x$ nanosheets using a single thermal oxidation step, offering a large parameter space within which to design high-performance MOSFETs.

In this paper, we advanced the fabrication of self-organized gate-stacking heterostructures in combination with self-aligned ITO gates using replacement-metal-gate (RMG) processes via dummy poly-Si gates to boost speed of photoMOSFETs by reducing gate-to-source (C_{GS}) and gate-to-drain (C_{GD}) capacitances.

II. EXPERIMENTS

Process flow and key process modules for fabricating our photoMOSFETs are summarized in Figs. 1 and 2, respectively. Starting with an SOI substrate with a 200 nm-thick single-crystalline Si layer on top of a 400 nm-thick buried oxide layer (Fig. 1(a)), bi-layers of 20 nm-thick Si_3N_4 and 60 nm-thick poly-$Si_{0.85}Ge_{0.15}$ were sequentially deposited (Fig. 1(b)) using low-pressure chemical vapor deposition (LPCVD). Following lithographic patterning of active-area mesas of poly-$Si_{0.85}Ge_{0.15}$/Si_3N_4/Si (Fig. 1(c)), array of poly-$Si_{0.85}Ge_{0.15}$ pillars with pillar width/pitch of 100 nm/140 nm was produced using electron-beam lithography (EBL) in combination with SF_6/C_4F_8 plasma etching (Figs. 1(d) and 2(a)). Next, thermal oxidation at 900 °C in an H_2O ambient was conducted to convert the Si content of poly-SiGe pillars to SiO_2, within which segregated Ge interstitials coarsened and coalesced into a single Ge nanosphere with a diameter of 50 nm per oxidized pillar (Figs. 1(e) and 2(b)). Concurrent with the formation of Ge nanospheres, self-organized SiO_2 shells and single-crystalline $Si_{1-x}Ge_x$ nanosheets were also formed due to a unique penetration of Si_3N_4 and Si layers by Ge nanospheres as a consequence of exquisite interplay of Ge, Si, and oxygen interstitials [21].

Following the formation of self-organized heterostructures of Ge nanosphere/SiO_2/$Si_{1-x}Ge_x$ nanosheet array, SiO_2 layers were deliberately deposited to fill the gaps between oxidized pillars (Figs. 1(f) and 2(c)). Next, a direct etch-back process was conducted for planarization (Figs. 1(f) and 2(d)).

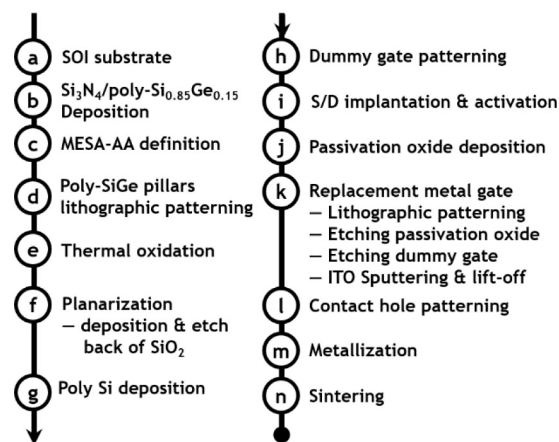

FIGURE 1. Process flow for the fabrication of Ge nanosphere/SiO_2/SiGe-nanosheet MOSFETs with self-aligned ITO gates. (a) on top of a SOI substrate, (b) Si_3N_4 and poly-$Si_{0.85}Ge_{0.15}$ were deposited, followed by (c) lithographic patterning of mesa-active areas. (d) poly-$Si_{0.85}Ge_{0.15}$-pillars array was formed using EBL/plasma etching. (e) thermal oxidation converted the poly-$Si_{0.85}Ge_{0.15}$ pillar to a self-organized heterostructure of Ge nanosphere/SiO_2/SiGe nanosheet per pillar. (f) gate-stacking heterostructures were planarized by the deposition and direct etch-back of SiO_2. A poly-Si layer was (g) deposited and (h) lithographically patterned as dummy gates. (i) As^+ ions were implanted and activated by thermal annealing forming S/D. (j) a SiO_2 layer was deposited for passivation. (k) passivation SiO_2 and dummy poly-Si gates were removed by lithography, CHF_3 and SF_6/C_4F_8 plasma etching, respectively, using photoresists of LOR 5A/PMMA photoresist mask, followed by ITO sputtering and lift-off. (l) contact-hole, (m) metallization, and (n) sintering processes were conducted for forming electrodes.

It is noted that a 5–10 nm thick SiO_2 layer remained on top of the Ge nanospheres after planarization. A 350 nm-thick poly-Si layer was deposited and lithographically patterned as dummy gates (Figs. 1(g), 1(h), and 2(e)) for the subsequent formation of S/D via As^+ implantation (Fig. 1(i)). After thermal annealing at 900 °C for 30 sec for activation, a 400 nm-thick LPCVD SiO_2 layer was deposited over the dummy poly-Si gates (Figs. 1(j) and 3(a)) for the subsequent RMG processes. Following lithography using bi-layered photoresists of LOR 5A/PMMA (Figs. 1(k) and 3(b)), SiO_2 layers and dummy poly-Si gates were etched using CHF_3 and SF_6/C_4F_8 plasma, respectively. Then, a 350 nm-thick ITO layer was sputtered and lifted off, forming self-aligned, transparent gates (Figs. 1(k) and 3(c)). Finally, contact, Al metallization, and sintering (in an H_2/N_2 (5%/95%) ambient at 400 °C for 30 min) processes completed the device fabrication (Figs. 1 l–n).

Current-voltage characteristics of Ge nanospheres/SiO_2/$Si_{1-x}Ge_x$-nanosheets photoMOSFETs were measured using an Agilent B1500A semiconductor parameter analyzer in the darkness and under 850 nm−1550 nm illumination via normal incidence onto the transparent ITO gates.

III. RESULT AND DISCUSSION

A. SELF-ORGANIZED GATE-STACKING HETEROSTRUCTURES OF GE NANOSPHERE/SIO_2/SIGE NANOSHEET

It is clearly seen in Figs. 2(b-e) that a single, 50 nm-diameter Ge nanosphere is formed per oxidized pillar with

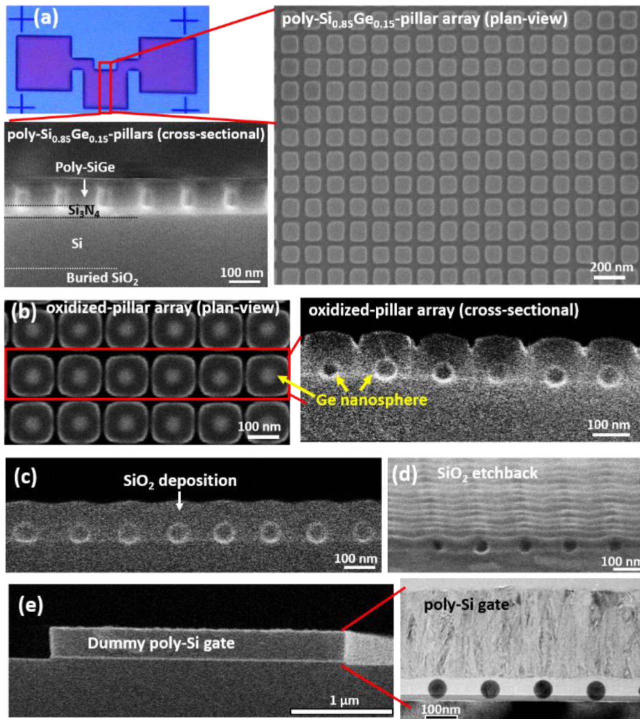

FIGURE 2. Plan-view and cross-sectional SEM observations of (a) poly-$Si_{0.85}Ge_{0.15}$ pillars array formed using EBL/plasma etching, (b) a single Ge nanosphere generated per oxidized pillar following thermal oxidation, (c) deposition and (d) etch back of SiO_2 for planarization, and (e) dummy poly-Si gate formed by deposition and lithographic patterning of poly-Si layers for subsequent S/D and RMG processes.

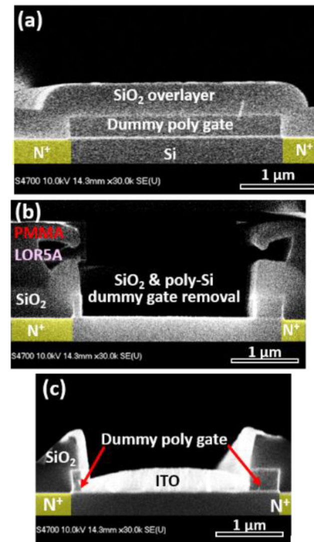

FIGURE 3. Self-aligned ITO gate formed by RMG processes. Dummy poly-Si gates were (a) encapsulated by a 400 nm-thick SiO_2 layer and (b) etched by SF_6/C_4F_8 plasma using LOR 5A/PMMA mask. (c) ITO layers were sputtered and lift-off.

high degree of uniformity and reproducibility in terms of diameter and spatial locations within a 3 µm × 20 µm array. Another important finding of notes is that the Ge nanospheres are not static within oxidized pillars but penetrate underlying buffer layers of Si_3N_4, and even get in touch with Si layers as seen from plan-view and cross-sectional scanning-electron microscopy (SEM) and transmission-electron microscopy (TEM) micrographs in Figs. 2(b-e). Our previous reports have shown that the unique migration of Ge nanospheres also leads to the simultaneous formation of (1) a conformal 10–20 nm-thick, single-crystalline $Si_{1-x}Ge_x$ nanosheet on the surface of Si layers due to Ge interstitials diffusion from the penetrating Ge nanosphere and (2) a conformal 2–3 nm-thick SiO_2 layer between the penetrating Ge nanosphere and underlying $Si_{1-x}Ge_x$ nanosheet. The unique migration of Ge nanospheres and formation of conformal SiO_2-shell and SiGe nanosheets relate to dynamic SiO_2 destruction-construction processes occurring near the surface of Ge nanospheres, [17] resulting from the interplay of Ge, Si, and Oxygen interstitials. Detailed mechanisms have been elaborated elsewhere [17]–[21].

B. SELF-ALIGNED ITO GATE

In our proposed RMG approach, the dummy poly-Si gate allows n^+-Si S/D to self-align with the ITO gate and thereby eliminates parasitic capacitances due to the gate overlapping S/D (Fig. 2(e)). Following S/D formation, a 400 nm-thick, conformal layer of SiO_2 encapsulating the dummy poly-Si gates was deliberately deposited (Fig. 3(a)) to improve the tolerance for overlay misalignments during the subsequent lithography process for forming ITO gates. The dummy poly-Si gate was then replaced by a transparent ITO gate using combination processes of lithographic patterning using LOR 5A/PMMA photoresists (Fig. 3(b)), removal of dummy poly-Si gate using SF_6/C_4F_8 plasma etching with a high etching selectivity (>20) of poly-Si over SiO_2, as well as ITO sputtering and lift-off (Fig. 3(c)). Fig. 3(c) shows the success in forming ITO gate over array of Ge nanospheres/SiO_2/SiGe nanosheets and the self-alignment of ITO/poly-Si gate with S/D, minimizing parasitic C_{GS} and C_{GD}.

C. STEADY-STATE TRANSFER CHARACTERISTICS OF GE NANOSPHERES/SIO_2/ SIGE-NANOSHEETS PHOTOMOSFETS

Fig. 4 shows transfer characteristics of Ge nanospheres/SiO_2/SiGe-nanosheets photoMOSFETs biased at $V_D = +1$ V and measured either in the darkness or under 850 nm, 1310 nm and 1550 nm illuminations with variable-incident power (P_{IN}). It is clearly seen that illumination indeed induces considerable photocurrent. For instance, 850 nm illumination with $P_{IN} = 242$ µW significantly enhances the ON-state current (I_{ON} at $V_G - V_{th} = +1.4$ V) and OFF-state current (I_{OFF} at $V_G - V_{th} = -3$ V) by a large factor of 13 and 2.8×10^8 in magnitude, respectively, as compared to drain current measured in the darkness (Fig. 4(a)). Similarly, 1310 nm (1550 nm) illumination with $P_{IN} = 1.3$ mW (2.2 mW) induces a current gain (I_{photo}/I_{dark})

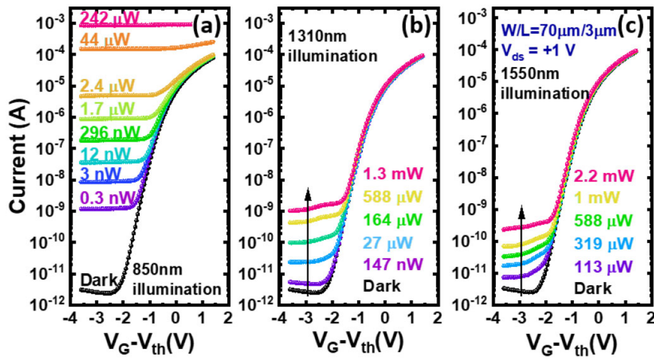

FIGURE 4. $I_D - V_G$ **characteristics of Ge nanospheres/SiO_2/SiGe photoMOSFETs measured in the darkness and under (a) 850 nm, (b) 1310 nm, and (c) 1550 nm illuminations.**

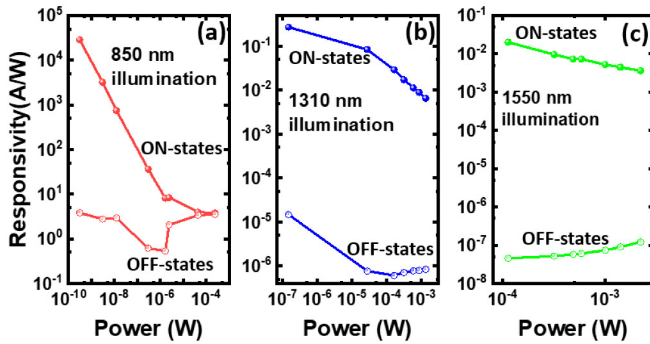

FIGURE 5. Power-dependent photoresponsivity of 50 nm Ge-nanosphere/SiO_2/SiGe photoMOSFETs measured under (a) 850 nm, (b) 1310 nm, and (c) 1550 nm illumination.

of 1.1 A/A (1.1 A/A) and 323 A/A (120 A/A) for photoMOSFETs electrically operating at the ON-state and OFF-state, respectively, as shown in Fig. 4(b) (Fig. 4(c)).

When our photoMOSFETs operating at $V_G - V_{th} = +1.4$ V, a low-power (0.3 nW) illumination at 850 nm induces very large photoresponsivity ($\Re \equiv (I_{photo} - I_{dark})/P_{IN}$) of 2.8×10^4 A/W (Fig. 5(a)). Similarly, photoresponsivity of 0.27 A/W and 20 mA/W are measured at 1310 nm illumination with $P_{IN} \sim 147$ nW (Fig. 5(b)) and 1550 nm illumination with $P_{IN} \sim 113$ μW (Fig. 5(c)), respectively. For 850 nm photodetection, our photoMOSFETs biased at $V_G - V_{th} = -3$ V show a wide dynamic range of photocurrent linearity of more than 6 decades. A nearly constant photoresponsivity of 4 A/W over a range of P_{IN} from 0.3 nW to 0.3 mW (Fig. 5(a)), suggests a good photocurrent linearity of our photoMOSFETs operating at the OFF-state. While high photoresponsivity of $>10^4$ A/W is achievable from our photoMOSFETs operating at the ON-state, the photoresponsivity significantly decreases with increasing P_{IN} from 0.3 nW to 242 μW. The photocurrent nonlinearity is possibly attributed to the set-in of series resistance at high current levels. A considerable improvement in the photocurrent linearity is observed when photoMOSFETs operating at the ON-state under illumination at 1310 nm (Fig. 5(b)) and 1550 nm (Fig. 5(c)).

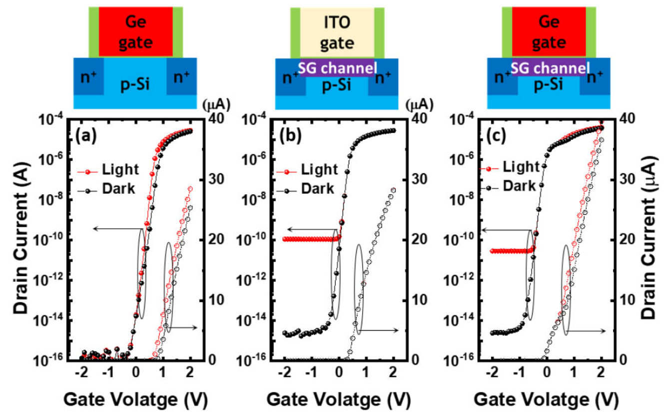

FIGURE 6. Calculated $I_D - V_G$ **curves of three different MOSFETs with gate-stacking heterostructures of (a) Ge-gate/SiO_2/Si-channel, (b) ITO gate/SiO_2/SiGe-channel, and (c) Ge-gate/SiO_2/SiGe-channel on Si substrates in the darkness and under 1550 nm illumination with P_{IN} at 1 W/cm^2.**

D. MECHANISMS FOR LARGE PHOTORESPONSIVITY

Using Silvaco TCAD simulator, we have carried out numerical calculations in order to gain insights to origins of large photoresponsivity in our studied photoMOSFETs. Transverse field-dependent mobility, Shockley-Read-Hall recombination, and Fermi-Dirac carrier statistics are included in simulation. Three device configurations including Ge gate/SiO_2/Si-channel MOSFETs, ITO-gate/SiO_2/SiGe-channel MOSFETs, and Ge-gate/SiO_2/SiGe-channel MOSFETs are considered to resolve the pivotal role of Ge-gate and SiGe-channel individually in response to illumination. Among these configurations, the thicknesses of gate, gate-oxide and $Si_{1-x}Ge_x$ channel are set to be 200 nm, 4 nm and 20 nm. The Ge content in the $Si_{1-x}Ge_x$ channel is set to be 0.55 according to our previous analysis [19]. In order to exclude the contribution from Si substrates, illumination wavelength of 1550 nm is chosen because of an extremely low absorption coefficient in Si.

Fig. 6 shows that three studied configurations exhibit completely different photocurrent behaviors in response to 1550 nm illumination with $P_{IN} = 1$ W/cm^2. Firstly, illumination simply makes a negative shift in the threshold voltage (V_{TH}) of Ge-gate/SiO_2/Si-channel MOSFETs, leading to visible photocurrent enhancement at the ON-state but no photocurrent gain at the OFF-state (Fig. 6(a)). A negative V_{TH} shift in the Ge-gate/SiO_2/Si-channel MOSFETs is attributable to the presence of large amounts of excess photoholes within the entire Ge-gate. For instance, Fig. 7(a) shows that calculated hole concentration near the Ge-gate/SiO_2 interface increases from 10^{13} cm^{-3} in the darkness to 10^{17} cm^{-3} under 1550 nm illumination, indicating that Ge-gate is an effective optical gate modulating the vertical potential of Ge-gate/SiO_2/Si. Therefore, the photocurrent gain achieved from the Ge-gate/SiO_2/Si-channel MOSFETs operating at the ON-state is due to the Ge-gate induced photovoltaic effects. Secondly, ITO-gate/SiO_2/SiGe-channel

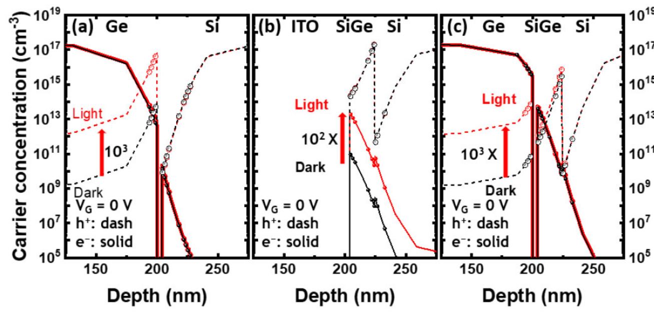

FIGURE 7. Calculated carrier distribution (at $V_G = 0$ V) across the gate-stacking heterostructures of (a) Ge-gate/SiO_2/Si-channel, (b) ITO-gate/SiO_2/SiGe-channel, and (c) Ge-gate/SiO_2/SiGe-channel in the darkness and under illumination at 1550 nm. (dashed line and solid line denote hole and electron concentration profiles, respectively).

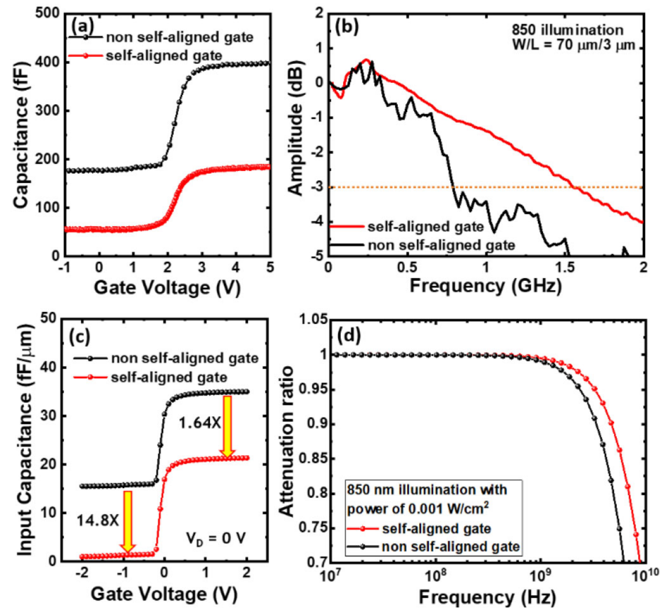

FIGURE 8. Experimental/calculated (a)/(c) input capacitance and (b)/(d) frequency response of our Ge photoMOSFETs with self-aligned and non-self-aligned ITO gates.

MOSFETs show large photocurrent gain at the OFF-state but invisible changes on the V_{TH} and the ON-state current under 1550 nm illumination (Fig. 6(b)). The substantial photocurrent enhancement in ITO-gate/SiO_2/SiGe-channel MOSFETs electrically-operating at the OFF-state, arises from the efficient generation of photoelectrons (that is, 10^{11} cm^{-3} electrons in the darkness versus 10^{13} cm^{-3} photoelectrons under illumination as shown in Fig. 7(b)) directly within the SiGe channel, contributing additionally photoconductive current. Lastly but most importantly, our proposed Ge-gate/SiO_2/SiGe-channel MOSFETs exhibit visible photocurrent gains at both electrically OFF-state and ON-state under illumination (Figs. 6(c) and 7(c)) due to photoconductive and photovoltaic current enhancement in the SiGe-channel and Ge-gate, respectively. Both calculated $I_D - V_G$ curves shown in Fig. 6 and photocarrier distribution displayed in Fig. 7 clearly point out the pivotal roles of Ge-gate and SiGe-channel. That is, Ge gate is an efficient optical-gate tuning V_{TH} of photoMOSFETs and giving rise to photovoltaic current gain when photoMOSFETs electrically-operating at the ON-state, whereas the photoelectrons generated within the SiGe channel contribute considerable photocurrent and large photocurrent gain when photoMOSFETs electrically-operating at the OFF-state.

E. TRANSIENT RESPONSE OF GE NANOSPHERE/SIO_2/SIGE-NANOSHEET PHOTOMOSFETS

Benefits of our proposed self-aligned ITO gate structures for improving 3 dB frequency are verified by both experimental measurement and numerical simulation. Fig. 8(a) and (b) show experimentally-measured input capacitance and frequency response, respectively, of our Ge nanosphere/SiO_2/SiGe-nanosheet photoMOSFETs with self-aligned and non-self-aligned ITO gates. It is clearly seen that the input capacitance is reduced by a factor of 2–3X and the 3dB frequency is improved from 0.8 GHz to 1.6 GHz when the non-self-aligned ITO gate is replaced by self-aligned ITO gate. Calculated input-capacitance values of photoMOSFETs with self-aligned ITO gates are 1.05 fF/μm and 21.34 fF/μm when operating at electrically OFF-state and ON-state, respectively, which are lower than that of non-self-aligned photoMOSFETs by 14.8-fold and 1.64-fold as shown in Fig. 8(c). Figure 8(d) shows that calculated 3 dB frequency of photoMOSFETs improves from 6.0 GHz to 8.5 GHz when replacing non-self-aligned ITO gates by self-aligned ITO gates. Considering the difference between calculated and experimental values of input capacitance and 3dB frequency, it appears that we are able to further improve experimental data by reducing series resistance and contact resistance of S/D using self-aligned silicdation processes.

Another possible benefit of our proposed Ge photoMOSFETs is the feasibility of Si_3N_4-waveguided phototransistors. This is because our self-organized gate-stacking heterostructures are surrounded by Si_3N_4 buffer layers, which could be fabricated as waveguides by proper structure design.

F. BENCHMARK OF GE NANOSPHERE/SIO_2/SIGE-NANOSHEET PHOTOMOSFETS

Key performance metrics in terms of dark current, photoresponsivity, current gain, 3dB frequency of Ge bipolar phototransistors, [8] Ge-gate photoMOSFETs, [10] and our Ge-nanosphere/SiO_2/SiGe-nanosheet photoMOSFETs with self-aligned and non-self-aligned ITO gates [21] are compared in Table 1. Dark current, current gain, and 3dB frequency are much improved in Ge-nanosphere/SiO_2/SiGe-nanosheet photoMOSFETs when the non-self-aligned ITO gate is replaced by the self-aligned ITO gate. Compared to previously-reported Ge bipolar phototransistors and Ge-gate photoMOSFETs, our proposed Ge photoMOFETs feature much lower dark current (at least of 5 orders reduction in magnitude) and comparable 3dB frequency.

TABLE 1. Comparison of reported Ge phototransistors and our Ge-nanosphere/SiO_2/SiGe nanosheet photoMOSFETs.

Transistor	Responsivity (A/W) @1550nm	Current gain (A/A)	Dark current (A)	3dB frequency (GHz)	Ref.
Ge bipolar transistor	2 @ 1 V, P_{IN} = 0.1 mW	6.5	16 μA	1	[8]
Ge-gate nMOSFET (L = 1 μm)	0.152 @1 V, P_{IN} = 0.5 mW	1.46	240 nA	2.5 @ P_{IN} = 0.9 mW	[10]
Ge-nanosphere/SiO_2/ SiGe nanosheet nMOSFET (L = 3 μm)					
non-self-aligned ITO gate	0.017 @ 3 V, P_{IN} = 1.1 mW	1.1	45 pA	1.2 @ P_{IN} = 0.9 mW	[21]
self-aligned ITO gate	0.02 @ 1.4V, P_{IN} = 0.1mW	1.1	2 pA	1.6 @ P_{IN} = 0.9 mW	This work

IV. CONCLUSION

We reported the advanced fabrication of self-aligned ITO-gate Ge-nanosphere /SiO_2/SiGe-channel photoMOSFETs using our proposed RMG process for the improvement of dark current, input capacitance, and 3 dB frequency simultaneously. When electrically-operating at the ON-state ($V_G - V_{th} = +1.4$ V), our photoMOSFETs exhibit very large photoresponsivity of 10^2 A/W and 0.27 A/W under 850 nm and 1310 nm illumination, respectively, with low-power excitation at 100 nW. Whereas very large photocurrent gains of 2.8×10^8, 323, and 95 (A/A) are achievable from our phtoMOSFETs electrically-operating at OFF-state under 850 nm, 1310nm, and 1550nm illumination with P_{IN} of 242 μW, 1.3 mW, 2.2 mW, respectively. The effectiveness of self-aligned ITO gates for improving input capacitance and 3dB frequency is evidenced by both experimentally-measured and calculated data in comparison to their counterpart transistors with non-self-aligned ITO gates. Our detailed simulation analysis further points out the pivotal roles of Ge gate and SiGe channel for inducing photovoltaic and photoconductive current, respectively.

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