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GaN-Based GAA Vertical CMOS Inverter

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ABSTRACT In this work, we simulate the static and dynamic characteristics of gallium nitride (GaN)-based gate-all-around (GAA) vertical nanowire complementary metal–oxide–semiconductor (CMOS) inverter. Based on the 3-D simulator of Silvaco-TCAD, the simulated physical models and associated model parameters have been well calibrated with the reported experimental results of GaN n-channel NWFET and the simulated typical electrical parameters match the measured data. According to the simulation results, the GaN GAA vertical nanowire CMOS inverter exhibits rail-to-rail operation, low static power dissipation, large noise margins, high thermal stability and good scalability.

INDEX TERMS GaN, nanowire CMOS inverter, simulation, high thermal stability, good scalability.

I. INTRODUCTION

Gallium nitride (GaN) has become important semiconductor for power device applications due to its superior material properties such as wide bandgap energy, high breakdown field, high electron mobility and superior thermal stability [1]–[4]. In addition, GaN-based gate-all-around (GAA) vertical nanowire field-effect transistor (NWFET) with three-dimensional (3-D) gate structures have shown further improved performances, such as high on-and-off-state current ratio, low off-state leakage current and linearity, due to the excellent gate controllability [5]–[8]. Moreover, complementary metal-oxide-semiconductor (CMOS) technology is dominant because it consumes low static power dissipation, reduces the circuit complexity and also offers higher noise immunity and the scalability [9]. The main benefits of scalability are (1) smaller device sizes and thus reduced chip size (increased yield and more parts per wafer), (2) lower gate delays, allowing higher frequency operation, and (3) reduction in power dissipation [10]. Therefore, GaN-based GAA vertical nanowire CMOS inverter may be useful for integrating some digital functions with power GaN devices.

Recently, there has been a number of demonstrations of GaN CMOS inverter [11]–[16]. However, all of these demonstrations rely on the integration of lateral AlGaN/GaN high-electron-mobility transistors (HEMTs) and the importance of the scaling theory is not well proven. To demonstrate the potential of vertical NWFET and scaling MOS transistors, it is important to simulate the characteristics of GaN GAA vertical nanowire CMOS inverter.

In this paper, we study the effects of nanowire diameter, temperature and scalability on GaN-based GAA vertical nanowire CMOS inverter by Silvaco-TCAD 3-D simulator. The simulation results show that well-placed switching point voltage and a sharp transition region, offering good noise margins and robustness for multistage logic gate integration. In addition, the inverter also exhibits rail-to-rail operation, low static power dissipation, high thermal stability and excellent scalability. Due to many excellent characteristics, GaN-based nanowire CMOS inverter could be used in high-temperature, high-frequency, high-power-density applications.

II. DEVICE STRUCTURE AND SIMULATION MODELS

Fig. 1 (a) shows the 3-D structural schematic of the GaN GAA vertical nanowire CMOS inverter. The nanowires are formed by inductively coupled plasma reactive ion etching (ICP RIE) from epitaxial layers, which are grown by metal-organic vapor phase epitaxy (MOVPE) on Fe-doped GaN substrate with high resistance characteristics. Firstly, a

0.2-μm-thick Mg-doped GaN with doping concentration of 2×10^{18} cm^{-3} is grown as a bottom drain access layer. Then, ion implantation is used to selectively dope the p^+ epitaxial layer to form n^+ GaN with doping concentration of 2×10^{18} cm^{-3}. Secondly, a 0.4-μm-thick Si-doped GaN with doping concentration of 2×10^{15} cm^{-3} is grown as a channel layer. Similarly, ion implantation is used to selectively dope the n^- epitaxial layer to form p^- GaN with doping concentration of 2×10^{15} cm^{-3}. Finally, a 0.2-μm-thick Mg-doped GaN is grown for the top source contact with doping concentration of 2×10^{18} cm^{-3}. Ion implantation is used to selectively dope the p^+ epitaxial layer to form n^+ GaN with doping concentration of 2×10^{18} cm^{-3}. The nanowire channel is completely covered with 20-nm-thick Al_2O_3 dielectric layer and 200 nm-thick Cr gate metal. The details of the nanowire device fabrication can be found in [5]. In order to increase the pull-up current of the p-NWFET, the ratio (α) of nanowire number for p-NWFET and n-NWFET is 8:1 to compensate lower mobility of carriers (holes) in p-NWFET. Moreover, the diameter of p-NWFET ($d_{NW,p}$) is also widened to further increase the pull-up current. The device structure information and key parameters used in this work are given in Fig. 1(b) and 1(c), which are the corresponding 2-D cross-sectional view of the n-NWFET and p-NWFET. It can be clearly seen that the doping concentration of n-NWFET and p-NWFET exhibits a complementary relationship. The schematic of GaN CMOS inverter circuit is shown in Fig. 1(d). The source, gate and drain electrodes are denoted as 'S', 'G' and 'D', respectively.

All the work in this paper is based on the 3-D simulator of Silvaco-TCAD. The models considered in this simulation include field dependent mobility (FLDMOB), the Shockley–Read–Hall (SRH) recombination model, the Auger recombination model, the low field mobility model, the impact ionization model and incomplete ionization model [17]. Moreover, based on the experimental data of GaN-based n-NWFET reported in [5], all models parameters have been further calibrated. The transfer and output characteristic curves are presented in Fig. 1(e) and 1(f). It is noted that these models in the simulations have been well calibrated with the measured results of n-NWFET devices reported in [5], and the simulated typical electrical parameters match the measured data. Based on the calibrated physical models and associated model parameters of n-NWFET, we change the doping type when performing p-NWFET simulations (e.g., changing n-type doping to p-type doping), to form complementary NWFET. In other words, the whole simulation study is also stable to the physical model of the p-NWFET. Thereby, the simulation platform has great reference value.

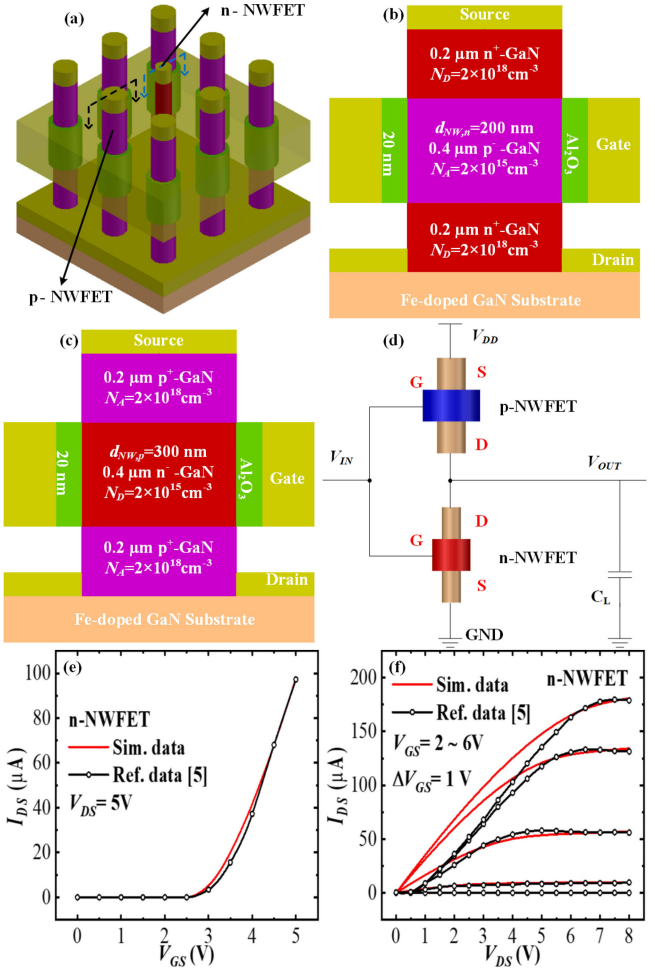

FIGURE 1. (a) 3-D structural schematic of the GaN GAA vertical nanowire CMOS inverter with 8:1 ratio of p-NWFET to n-NWFET. (b) 2-D cross-sectional view of n-NWFET and (c) p-NWFET along the cutline shown in (a). (d) Circuit schematic of GaN-based nanowire CMOS inverter. (e) Comparison of simulated GaN n-NWFET transfer and (f) output characteristics with experimental data [5].

III. SIMULATION RESULTS AND DISCUSSION

Fig. 2(a) and 2(b) show the transfer characteristics of n-NWFET and p-NWFET in linear and logarithmic scale constituting the GaN-based GAA vertical nanowire CMOS inverter. The threshold voltage of n-NWFET (V_{THN}) and p-NWFET (V_{THP}), defined at $|I_{DS}| = 1$ μA and $|V_{DS}| = 5$ V, are 0.8 V and −0.8 V respectively. Therefore, both devices are truly enhancement mode (E-mode) with almost symmetric threshold voltages. It is noted that the fixed positive surface/interface charges of 1×10^{12} cm^{-2} is assumed in the simulation [18]. In addition, the current on-and-off-ratio (I_{on}/I_{off}) of both are about 10^8 when I_{on} and I_{off} are defined at $|V_{GS}| = 5$ V and $|V_{GS}| = 0$ V, respectively. The subthreshold swing (SS) of the n-NWFET and p-NWFET are 62 mV/dec and 68 mV/dec respectively, both of which are close to theoretical limit at room temperature (i.e., 60 mV/dec). Both devices exhibit a high I_{on}/I_{off} and small subthreshold swing, owing to the 3-D gate nanowire structures.

Fig. 2(c) shows the output characteristics of n-NWFET and p-NWFET constituting the GaN CMOS inverter. The effective switch resistance of n-NWFET (R_n) and p-NWFET (R_p) at $|V_{GS}| = 2.5$ V and $|V_{DS}| = 2.5$ V are nearly equal, which is about 8 kΩ. It is also the requirement for equating

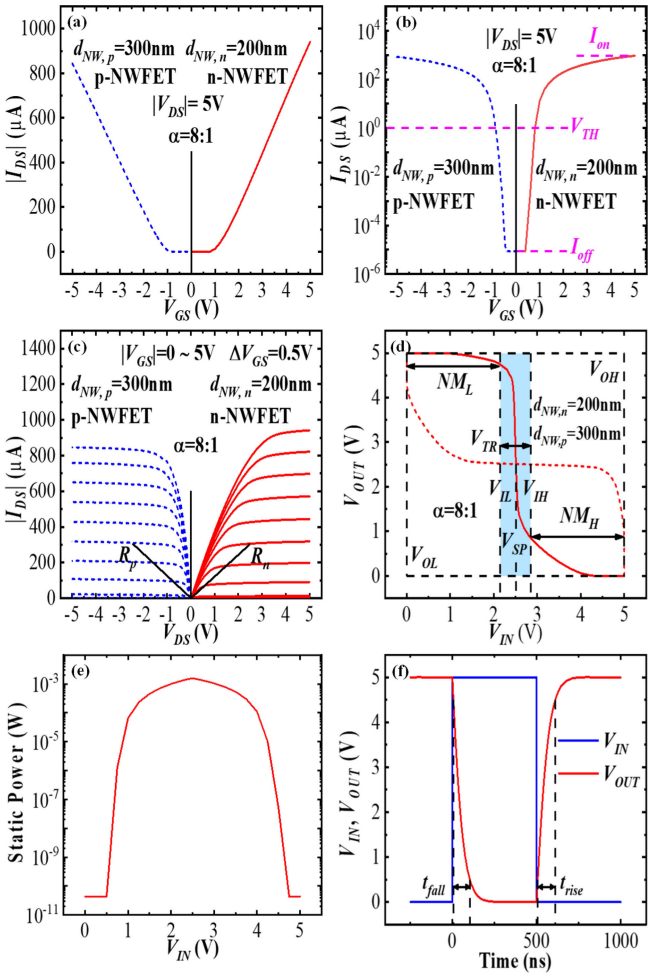

FIGURE 2. **(a) Transfer characteristics of n-NWFET and p-NWFET in linear and (b) logarithmic scale. (c) Output characteristics of n-NWFET and p-NWFET. (d) Butterfly curves for GaN-based nanowire CMOS inverter VTC. (e) Static power dissipation by sourcing current from the power supply of GaN-based nanowire inverter. (f) Dynamic switching characteristics of GaN-based nanowire inverter for an input logic pulse.**

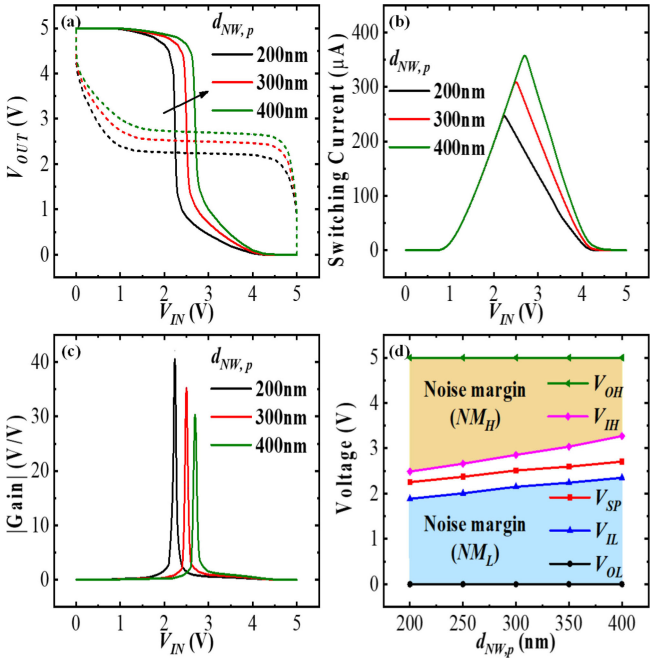

FIGURE 3. **(a) Voltage transfer characteristics, (b) switching current and (c) voltage gain of GaN-based nanowire inverter at different p-NWFET diameter ($d_{NW,p}$). (d) Summary of V_{OL}, V_{IL}, V_{SP}, V_{IH} and V_{OH} under 5 V V_{DD} at different p-NWFET diameter ($d_{NW,p}$).**

the propagation delays of n-NWFET and p-NWFET. The voltage transfer characteristics (VTC) in butterfly shape is shown in Fig. 2(d). The high-level output voltage (V_{OH}) and low-level output voltage (V_{OL}) are 5 V and 0 V, respectively, achieving rail-to-rail operation. The low-level input voltage (V_{IL}) and high-level input voltage (V_{IH}), defined at the unity-voltage-gain points (with $dV_{OUT}/dV_{IN} = -1$), are 2.15 V and 2.85 V respectively. The VTC consists of three main regions: the low-input region at $V_{IN} < V_{IL}$, the transition region at $V_{IL} \leq V_{IN} \leq V_{OH}$, and the high-input region at $V_{IN} > V_{IH}$. The width of the transition voltage region ($V_{TR} = V_{IH} - V_{IL}$) is a way of measure the ambiguity of the digital logic inverter, which must be as low as possible. The transition voltage width is 0.7 V/5 V (14%). The low-input-logic noise margin ($NM_L = V_{IL} - V_{OL}$) and high-input-logic noise margin ($NM_H = V_{OH} - V_{IH}$) are 2.15 V/2.5 V (86%) and 2.15 V/2.5 V (86%) respectively, which are equal to ensure the best performance. In other words, a noise margin isn't improved at the cost of the other margin. The CMOS inverter exhibits good characteristics with excellent symmetry. In addition, both noise margins are sufficiently large, so GaN-based nanowire CMOS inverter is equipped with high immunity to miscellaneous noises, such as electromagnetic interferences produced by high-frequency power switches. When the input voltage is equal to the output voltage, the input (or output) voltage is called the inverter switching point voltage (V_{SP}), which is equal to $V_{DD}/2$ (2.5 V) because of the symmetric threshold voltage of n-NWFET and p-NWFET. At this point, both MOSFETs in the inverter are in the saturation region and the drain current in each MOSFETs must be equal.

Fig. 2(e) presents the static power dissipation of CMOS inverter under 5 V V_{DD}. Such power dissipation only occurs during the transition, but it is greatly suppressed at both static logic states (with $V_{IN} = 0$ V or 5 V). When V_{IN} is 0 V or 5 V, one transistor is turned off and the other is turned on. Therefore, there is almost no quiescent current from V_{DD} to GND. The most important benefit of CMOS circuits has been demonstrated. As illustrated in Fig. 2(f), the dynamic response of the inverter is characterized for the input to a pulse and the output to a 20 pF capacitance at 1 MHz. The voltage of the input pulses varied from 0 V to 5 V with a ramp time of 50 ps. The output rise and fall times required for V_{OUT} to go from 0.1 V_{DD} (0.9 V_{DD}) to 0.9 V_{DD} (0.1 V_{DD}) are labeled t_{rise} and t_{fall}, respectively. The rise time is 105 ns and fall time is 98 ns, which are nearly equal.

Fig. 3(a) and 3(b) show the voltage transfer characteristics and switching currents at different values of $d_{NW,p}$.

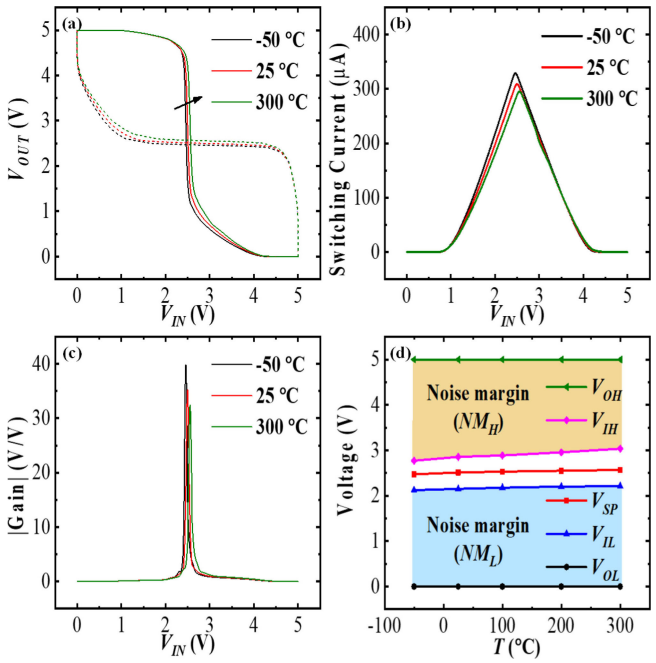

FIGURE 4. (a) Voltage transfer characteristics, (b) switching current and (c) voltage gain of GaN-based nanowire inverter at different temperatures (T). (d) Summary of V_{OL}, V_{IL}, V_{SP}, V_{IH} and V_{OH} under 5 V V_{DD} at different temperatures (T).

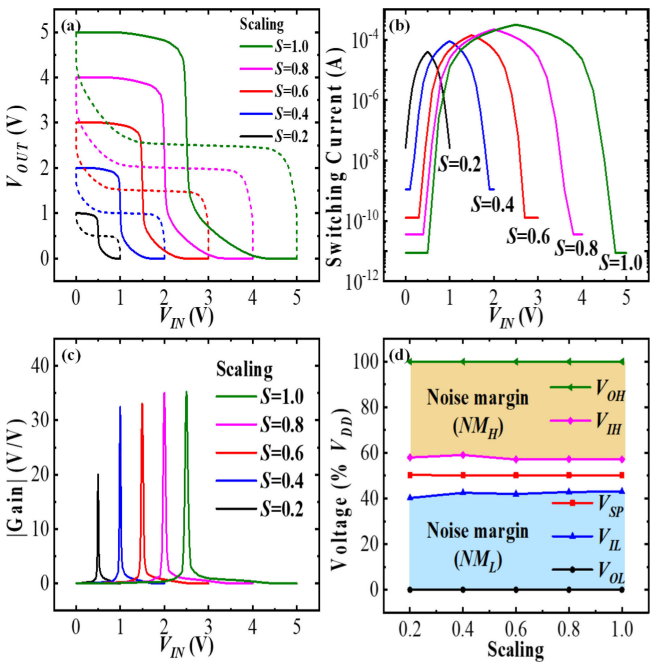

FIGURE 5. (a) Voltage transfer characteristics, (b) switching current and (c) voltage gain of GaN-based nanowire inverter at different scaling (S). (d) Summary of V_{OL}, V_{IL}, V_{SP}, V_{IH} and V_{OH} at different scaling (S).

Both V_{SP} and peak value of switching current increase as $d_{NW,p}$ increases. With the increase of $d_{NW,p}$, R_p of p-NWFET decreases, so the pull-up current strength of p-NWFET increases. V_{SP} at $d_{NW,p}$ = 400 nm is 2.7 V/5 V (54%), with 4% deviation compared with the value at $d_{NW,p}$ = 300 nm. As shown in the Fig. 3(c), the peak value of voltage gain is reduced as $d_{NW,p}$ is increased, because the transition voltage region becomes widen with increasing $d_{NW,p}$. The peak gain of 35 V/V is achieved at $d_{NW,p}$ =300 nm. The summary of V_{OL}, V_{IL}, V_{SP}, V_{IH} and V_{OH} under 5 V V_{DD} at various $d_{NW,p}$ (from 200 nm to 400 nm) is presented in Fig. 3(d). It is obvious that NM_L increases and NM_H decreases as $d_{NW,p}$ increases. NM_L and NM_H at $d_{NW,p}$ = 400 nm are 2.35 V/2.5 V (94%) and 1.73 V/2.5V (69.2%), respectively, with 8% increasing and 16.8% decreasing compared with the value at $d_{NW,p}$ = 300 nm. Therefore, it shows that low-input-logic noise margin NM_L is improved at the cost of high-input-logic noise margin NM_H.

Fig. 4(a)-4(c) present the voltage transfer, switching currents and voltage gain curves of GaN-based nanowire CMOS inverter measured from −50 °C up to 300 °C, from which the characteristic transition voltages are extracted and summarized in Fig. 4(d). The CMOS inverter has high temperature performance, revealing a very good behavior at 300°C with V_{IL} and V_{IH} equal to 2.21 V and 3.03 V, respectively. NM_L and NM_H at 300°C are 2.21 V/2.5 V (88.4%) and 1.97 V/2.5V (78.8%), respectively, which shows an excellent operation even at 300°C. V_{SP} at 300°C is 2.57 V/5 V (51.4%), with 1.4% degradation compared with the value at 25°C. Despite a slight expansion in the transition voltage region and deviations in V_{SP} at high temperatures, superior properties of the GaN CMOS inverter, such as rail-to-rail operation, wide noise margins and sharp logic state transition, are well preserved. At higher temperatures up to 300 °C, decent I_{on}/I_{off} and voltage gains (above 30 V/V) are still available. For conventional bulk silicon CMOS circuits, due to a relatively narrow bandgap of 1.1 eV in Si, their operating temperatures are commonly limited at 125°C for certain special applications, as Si MOSFETs cannot be effectively turned off and thermally induced junction leakage current can easily lead to latch-up and malfunction. GaN possesses a wide bandgap of 3.4 eV and provides a favorable platform to develop device and circuits for applications at high temperatures. Furthermore, the GaN CMOS inverter presented herein has demonstrated substantial high-temperature ruggedness, unveiling its promising potential to be deployed in harsh environments.

Fig. 5(a)-5(d) describes how scaling parameter S ($S \leq 1$) affects the characteristics of GaN-based nanowire CMOS inverter. S is used to scale the dimensions of a MOSFET. The value of S is typically in the neighborhood of 0.7 from one CMOS technology generation to the next. The ideal scaling theory follows three rules [9]: (1) reduce all lateral and vertical dimensions to S times the original (2) reduce threshold voltage and the supply voltage to S times the original; (3) increase all of the doping levels to 1/S times the original. Since the dimensions and voltages scale together, all electric fields in the transistor remain constant, hence the name "constant-field scaling". The off-state leakage current

is increased as S is decreased, because the channel length of NWFET becomes shorten with decreasing S. Similarly, due to the reduction of channel length, the output resistance decreases and therefore the voltage gain decreases. At lower S down to 0.2, off-state leakage current and voltage gain are 25 nA and 20 V/V, respectively. V_{SP} is almost at half of V_{DD} (from 1 V to 5 V) in spite of different scaling. In addition, NM_L and NM_H at $S = 0.2$ are 0.4 V/0.5 V (80%) and 0.42 V/0.5V (84%), respectively, with 6% and 2% degradation compared with the value at $S = 1$. Therefore, the scaling parameter is not suitable to be lower than 0.2.

Compared to the lateral GaN inverters [11]–[16], the GaN-based nanowire CMOS inverter in this work has the following advantages. Firstly, it realizes rail-to-rail operation. Only [13] achieves rail-to-rail operation, while the rest of the references cannot. Secondly, NM_L is equal to NM_H, ensuring symmetry of inverter. In other words, a noise margin isn't improved at the cost of the other margin. In addition, both noise margins are sufficiently large, ensuring high immunity to miscellaneous noises, such as electromagnetic interferences produced by high-frequency power switches. Finally, the rise and fall delays of the inverters are also nearly equal, indicating that the pull-up capability of the PMOS is the same as the pull-down capability of the NMOS (8:1 ratio).

IV. CONCLUSION

In this work, we have simulated GaN-based nanowire CMOS inverter circuit. The simulation results show that the inverter exhibits rail-to-rail operation, low static power dissipation, well-placed switching point voltage and sharp transition region with high voltage gain and large noise margins. In addition, the inverter also exhibits good thermal stability, which suggests that they could be suitable for application in harsh environments. Therefore, GaN-based nanowire CMOS inverter circuit could be used in monolithically integrated peripheral circuits for the driving, control and protection of GaN devices that are deployed in high-temperature, high-frequency, high-power-density applications.

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