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Implant Straggle Impact on 1.2 kV SiC Power MOSFET Static and Dynamic Parameters

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ABSTRACT Significant impact of the ion-implant straggle of the P^+ shielding region on the static and dynamic characteristics of 1.2 kV 4H-SiC power MOSFETs is demonstrated in this paper by using analytical and TCAD modeling. The P^+ region ion-implant straggle not only reduces the JFET width but increases the channel length. This combination is shown to displace a SiC power MOSFET structure optimized without ion-implant straggle away from the optimum JFET width required to achieve the lowest specific on-resistance, resulting in an increase in the specific on-resistance by a factor of 2-3x for the typically used JFET width of 0.7 μm. The theoretical analysis is supported by data measured on 1.2 kV SiC power MOSFETs fabricated with channel lengths of 0.3 and 0.5 μm using both accumulation and inversion mode channels. The presence of the P^+ shielding region ion-implant straggle is shown to: (a) increase specific on-resistance by 15-30%; (b) suppress short-channel effects; (c) reduce electric field in the gate oxide; (d) reduce the transconductance; (e) reduce saturated drain current; and (f) significantly reduce the gate-drain capacitance and gate charge. Impact of P^+ shielding region lateral straggle on device cell optimization is an important contribution of this paper.

INDEX TERMS 4H-SiC, accumulation, capacitance, cell optimization, gate charge, inversion, ion-implant straggle, on-resistance, silicon carbide, short-channel effect, transconductance.

I. INTRODUCTION

Silicon carbide (SiC) power MOSFETs are under development and commercialization for many applications requiring blocking voltages ranging from 600 V to 1700 V [1]. These applications include photovoltaic inverters and electric vehicles. Many papers have been published on 1.2 kV devices to demonstrate superior characteristics compared with silicon IGBTs for these applications [2], [3], [4], [5]. Device with 1.7 kV blocking voltage are also of interest for solar inverters [6], [7], [8], [9]. Even higher blocking voltage devices are needed for high power industrial motor drives and solid-state transformers used in power grids [10].

SiC power devices are fabricated by ion-implantation of aluminum and nitrogen to form the p and n-type regions [11]. The ion-implant for the n and p type dopants is staggered to create the channel because the dopants do not diffuse during the subsequent activation anneal step [12]. The scattering of the implanted dopants produces sideways excursion of the dopant beyond the edge defined by the SiO_2 masking material. This phenomenon is called the lateral straggle. The magnitude of the lateral straggle is proportional to the energy used for the ion-implantation. It has recently been reported that lateral straggle of the P-well region has a strong impact on the performance of 13 kV SiC planar-gate power MOSFETs [13]. It was demonstrated that the lateral straggle reduces the width of the JFET region producing an increase in on-resistance and even non-linear on-state characteristics. It was also pointed out that lateral straggle of the P-well impacts the edge termination performance, an effect that had been previously documented with simulations and experimental results [14]. However, the magnitude of the lateral straggle was not quantified in the paper [13]. The authors state that the straggle of the P-well is significant for their 13 kV devices due to the low drift region doping level, *unlike* in the case of 1.2 kV SiC power MOSFETs with a JFET width of 1.4 μm. A detailed analysis with experimental data was recently published on the impact of changing the channel length and JFET width for accumulation-channel 1.2 kV SiC power MOSFETs with 50 nm gate oxide thickness [15]. Consideration of the impact of ion-implant straggle of the

P-well on device performance and cell optimization is not mentioned in that paper.

In this paper, it is demonstrated for the first time that lateral straggle of the P^+ shielding region (or P-well) has a significant impact on the performance of both inversion and accumulation channel 1.2 kV SiC planar-gate power MOSFETs. The ion-implant energy used for the N^+ source implants are 10-times smaller than for the P^+ shielding region making its straggle negligible. Measurements performed on both accumulation-channel and inversion-channel 1.2 kV SiC power MOSFETs with channel lengths of 0.3 and 0.5 μm are presented in this paper in support of the analysis. The presence of lateral straggle is shown to not only reduce the JFET width but to also increase the channel length, which was not recognized in the previous publications. This has a strong impact on the transconductance and saturated drain current of the 1.2 kV SiC power MOSFET. All the experimental and theoretical results discussed throughout this paper are at 27 °C (300 °K).

In addition, the impact of lateral straggle of the P^+ shielding region on the dynamic characteristics of the SiC power MOSFET was not discussed in the previous publications [13], [15]. The analysis presented in this paper shows a substantial reduction in the gate-drain capacitance and the gate-drain charge due to the implant straggle of the P^+ shielding region that is favorable for obtaining faster transients in hard switching power circuits to reduce power losses. The lateral straggle of the P^+ shielding region is also shown to be beneficial in the blocking mode by suppressing short-channel effects and reducing the electric field in the gate oxide. These new insights are valuable for understanding the performance of 1.2 kV SiC power MOSFETs and optimizing their design.

Optimization of the overall static and dynamic performance of SiC power MOSFETs is a key aspect during their design. In this paper, the implications of the lateral straggle of the P^+ shielding region on optimization of cell design are discussed to allow minimizing the specific on-resistance and achieving the best high-frequency figures-of-merit (HF-FOM). The optimum JFET width designed on the mask to achieve the lowest specific on-resistance is shown to shift from 0.7 to 1.0 μm. However, the lowest high-frequency figures-of-merit FOM[$R_{on,sp}$*$C_{gd,sp}$] and FOM[$R_{on,sp}$*$Q_{gd,sp}$] are shown to occur at a JFET width of 0.75 μm.

II. DEVICE STRUCTURES AND FABRICATION

The 1.2 kV SiC power MOSFETs discussed in this paper utilize the commonly used linear cell topology. Both inversion and accumulation channel devices were fabricated for evaluation of electrical performance. The cell cross-section illustrated in Fig. 1(a) for the device without lateral straggle of the P^+ shielding region (L_{SP+}) represents the structure defined by the masks used to fabricate the devices. All the cell dimensions are provided in the figure, leading to a cell pitch of 2.6 μm (W_{cell} = 5.2 μm). In the accumulation-channel structures shown in Fig. 1, the N-base region was

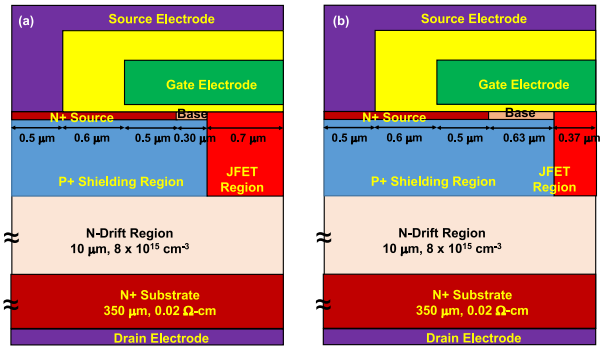

FIGURE 1. Cross-sectional view of 1.2 kV 4H-SiC accumulation-channel planar-gate power MOSFETs: (a) Without impact of P^+ shielding region ion-implant straggle; (b) With impact of P^+ shielding region ion-implant straggle.

formed above the P^+ shielding region by adjusting the profiles of the phosphorus and aluminum ion-implants performed with the same mask opening [16]. The N-base region is therefore self-aligned to the P^+ shielding region at its right-hand-side edge.

The lateral straggle of the P^+ shielding region is determined by the ion-implant energy used for its aluminum dopant. This energy is decided by the desired depth of the P^+ shielding region to achieve adequate shielding of the gate oxide. The cell cross-section in Fig. 1(b) shows the structure after including the straggle L_{SP+}. The lateral straggle L_{SP+} has been previously found to be 0.33 μm for the P^+ region used to fabricate 4H-SiC JBS rectifiers with the same implant conditions used for the MOSFETs in this paper [14], [17]. The channel length is increased from 0.3 to 0.63 μm due to straggle L_{SP+}, a large factor of 2.1x change.

Similar cross-sections are applicable for the inversion channel device because the P-base region is formed above the P^+ shielding region during the same masking step by tailoring the aluminum ion-implant dose and energy. In addition, devices with a channel length of 0.5 μm were included on the masks. They have similar cross-sections to those shown in Fig. 1 with a cell pitch of 2.8 μm due to the longer channel length with all other dimensions unchanged. In this case, the channel length increases from 0.5 to 0.83 μm due to straggle L_{SP+}, a significant change by a factor of 1.66x. The fabricated devices had an active area of 0.045 cm^2 and utilized the hybrid-JTE edge termination [18].

The 1.2 kV SiC power MOSFETs were manufactured in a 6-inch commercial foundry (X-Fab, TX) using the PRESiCE technology engineered by NCSU [19]. This is a non-self-aligned source/base process with alignment tolerance of 0.2 μm. It has been previously shown that 600 V SiC power MOSFETs with channel length of 0.3 μm can be manufactured with good yield for the case of a gate oxide thickness of 54 nm in spite of this alignment tolerance [20]. The doping concentration for the N-type JFET region was enhanced to 3 x 10^{16} cm^{-3} with nitrogen ion-implantation [21]. A JFET width of 0.7 μm was designed on the mask as employed in previous papers [16], [22] for the linear cell topology. A gate

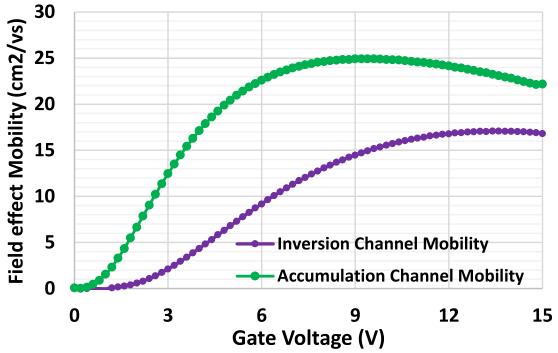

FIGURE 2. Measured accumulation and inversion mode channel mobility using FATFET test structures fabricated with the 1.2 kV SiC power MOSFETs.

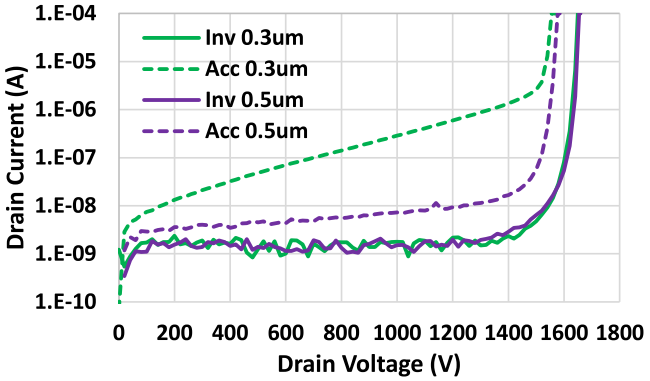

FIGURE 3. Measured blocking characteristics of the 1.2 kV SiC accumulation and inversion channel power MOSFETs with 0.3 μm and 0.5 μm channel length.

oxide thickness of 27 nm was grown by thermal oxidation. An NO annealing step similar to that used commonly for SiC power MOSFETs was utilized to enhance the channel mobility.

Previously reported 1.2 kV SiC power MOSFETs with 27 nm gate oxide thickness [23] used a N^+ source ohmic contact anneal temperature of 900 °C because they were fabricated together with JBSFETs. Higher contact anneal temperatures cannot be used for JBSFETs due to degradation of the Schottky contact in these devices [25], [26]. This anneal temperature produces a high N^+ source ohmic contact specific resistance of $\sim$ 0.8 mΩ-cm^2 that increases the specific on-resistance of the SiC power MOSFETs. The 1.2 kV SiC power MOSFETs with 27 nm gate oxide thickness reported in this paper were fabricated using a high ohmic contact anneal temperature of 1000 °C. TLM measurements of the ohmic contact resistance for the N^+ source region show a specific contact resistance of less than 1 x 10^{-5} Ω-cm^2 which makes this contribution negligible for the SiC power MOSFETs reported in this paper. This resulted in much lower specific on-resistances measured on these devices compared with previously reported devices [23].

The accumulation channel has been shown to produce larger channel mobility [16]. The inversion and accumulation channel mobility data extracted using FATFET test structures fabricated together with the 1.2 kV SiC power MOSFETs are provided in Fig. 2. The FATFET structure is a lateral MOSFET with a large channel length that is commonly used to extract the inversion or accumulation channel mobility [13], [16]. Accumulation channel MOSFETs utilize an N-base region that is completely depleted at zero gate bias by the built-in potential of the junction between the N-base region and the P^+ shielding region [11]. The channel is formed by an accumulation layer when a positive gate bias is applied. Less scattering at the oxide interface occurs for carriers in an accumulation layer, which makes the accumulation mobility larger than the inversion mobility as observed in Fig. 2. The accumulation channel mobility is observed to be significantly larger than the inversion channel mobility for gate bias ranging from 11 to 15 V. This is the relevant range of gate voltages for the operation of the power MOSFETs with gate oxide thickness of 27 nm from the reliability standpoint as discussed later in the paper. This data is used for the device analysis in subsequent sections.

III. MEASURED DEVICE CHARACTERISTICS

Static and dynamic characteristics of the 1.2 kV SiC power MOSFETs were obtained at wafer level using a Signatone semi-automated probe station and a Keysight B1505A curve tracer. The measured static device characteristics are: blocking voltage; leakage current; on-resistance; threshold voltage; and transconductance. These static characteristics are relevant to on-state and off-state performance. The blocking characteristics were measured with Flourinert over the wafer surface to avoid surface arcing problems. 76 devices were measured across the 6-inch wafer to obtain statistical distributions of these device parameters. The measured dynamic characteristics at wafer-level are: input, output, reverse-transfer capacitances, and gate charge. These parameters are a measure of switching performance in lieu of actual switching loss measurements that require packaging the devices. They have been used in previous publications to generate figures-of-merit for SiC power MOSFETs [23].

The measured characteristics of typical 1.2 kV SiC power MOSFETs with accumulation and inversion channels are provided in this section for the case of channel length of 0.3 and 0.5 μm. The analysis of these characteristics is performed in a subsequent section.

A. BLOCKING CHARACTERISTICS

The blocking characteristics were measured using zero gate bias. The performance of the accumulation and inversion channel devices with channel length of 0.3 and 0.5 μm can be compared in Fig. 3. The breakdown voltage at a typical leakage current of 100 μA used in datasheets is 1650 V for the inversion channel cases and 1560 V for the accumulation channel cases, both well above the rating of 1.2 kV. These values are determined by the hybrid-JTE edge termination used for the chips [18]. The breakdown voltage of these devices is much larger than the rating of 1.2 kV used in

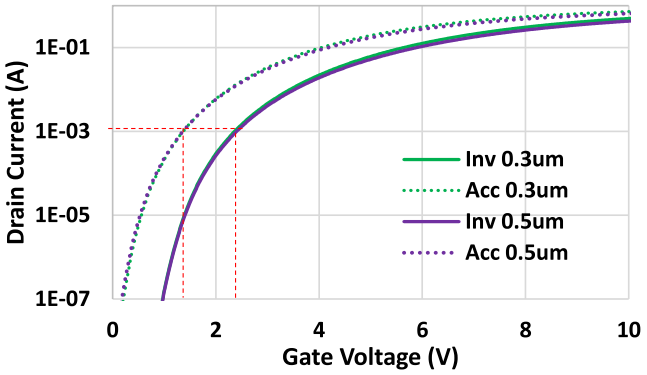

FIGURE 4. Measured transfer characteristics of the 1.2 kV SiC accumulation and inversion channel power MOSFETs with 0.3 μm and 0.5 μm channel length in the linear region.

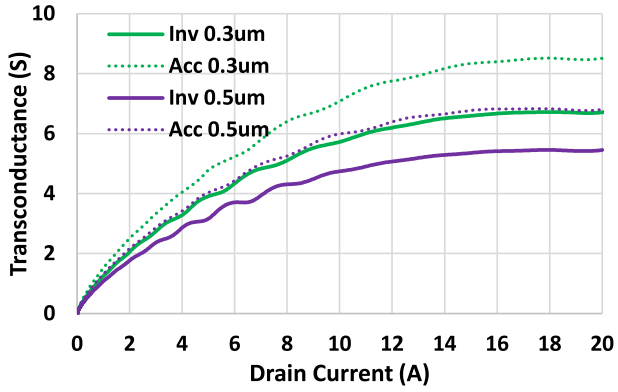

FIGURE 5. Measured transconductance of the 1.2 kV SiC accumulation and inversion channel power MOSFETs with 0.3 μm and 0.5 μm channel length at drain bias of 10 V.

the title and device descriptor in this paper, similar to the nomenclature used in previous publications [10]. The leakage current at 1200 V for the inversion channel SiC power MOSFET discussed in this paper is very low (< 2 nA). In contrast, the leakage current at 1200 V for the accumulation channel SiC power MOSFET is much larger (~ 1 μA for the 0.3 μm case and 10 nA for the 0.5 μm case). The leakage current for a 1.2 kV SiC power MOSFET product is typically 1 μA with a maximum value of 100 μA at 25 °C [28]. Consequently, the measured leakage current values are well within acceptable limits according to the datasheet. The high leakage current for the 0.3 μm accumulation channel device is explained in the device analysis section.

B. THRESHOLD VOLTAGE

The threshold voltages for all the devices were extracted using the transfer characteristics measured in the linear region using a drain bias of 0.1 V. The threshold voltages for the accumulation-channel SiC power MOSFETs are lower (1.4 V) than for inversion-channel MOSFETs (2.4 V) as previously reported for 54 nm gate oxide devices [22]. The physics determining the threshold voltage for accumulation-mode MOSFETs is different from inversion-mode MOSFETs [11]. The lower threshold voltage for the accumulation-channel devices discussed in this paper is determined by the doping profile and thickness of the N-base layer. A model for threshold voltage and the N-base parameters have been previously published [16]. The threshold voltage is observed to be independent of the channel length.

C. TRANSCONDUCTANCE

The transconductances of the 1.2 kV SiC power MOSFETs with gate oxide thickness of 27 nm were measured using the transfer characteristics in the current saturation region with a drain bias of 10 V. The extracted values are plotted in Fig. 5 to allow comparing the 4 cases. The largest transconductance is observed for the accumulation channel device with channel length of 0.3 μm. The lowest value for the transconductance is observed for the inversion channel device with channel length of 0.5 μm. The values for the 4 device cases is provided in Table 1 at a drain current of 10 A for comparison. The differences between these cases can be understood only after including the impact of the ion implant straggle as described in the subsequent analysis section.

TABLE 1. Summary of measured data on 1.2 kV SiC power MOSFETs.

MOSFET Device	1	2	3	4
Channel Type	Accu	Accu	Inver	Inver
$L_{CH,M}$ (μm)	0.5	0.3	0.5	0.3
BV (V)	1585	1572	1659	1657
I_L @ V_{DS}=1.2kV (μA)	0.009	0.6	0.002	0.002
$R_{on,sp}$ @ V_{GS}=11V, I_D=1A (mΩ-cm^2)	5.0	4.9	9.0	7.7
V_{TH} (V)	1.4	1.4	2.4	2.35
G_m @ V_{DS}=10 V, I_D=10A (S)	5.9	7.4	4.6	5.6
$C_{iss,sp}$ @ V_{DS}=1kV (pF/cm^2)	42417	40899	42640	40843
$C_{oss,sp}$ @ V_{DS}=1kV (pF/cm^2)	1097	1080	1053	1041
$C_{rss,sp}$ @ V_{DS}=1kV (pF/cm^2)	122	121	116	117
$Q_{gd,sp}$ (nC/cm^2)	313	296	318	304
FOM[$R_{on,sp}$*C_{rss}] (m□-pF)	610	593	1044	901
FOM[$R_{on,sp}$*Q_{gd}] (m□-nC)	1565	1450	2862	2341
FOM[$C_{iss,sp}$*$C_{gd,sp}$]	348	338	368	349

D. OUTPUT CHARACTERISTICS

Output characteristics were measured for the four types of 1.2 kV SiC power MOSFETs with gate voltage up to 15 V. The characteristics of the accumulation and inversion channel devices with channel length of 0.5 μm are shown in Fig. 6. The difference between the accumulation and inversion channel device characteristics is due a different effective gate drive voltage (V_G – V_{TH}) for the two cases because of different V_{TH} values; and due to the different channel mobilities for the accumulation and inversion mode cases.

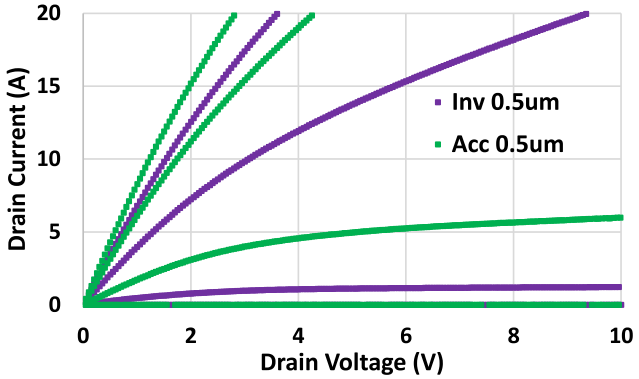

FIGURE 6. Measured output characteristics of the 1.2 kV SiC accumulation and inversion channel power MOSFETs with 0.5 μm channel length. Gate bias values of 0, 5, 10, and 15 V were used for these plots.

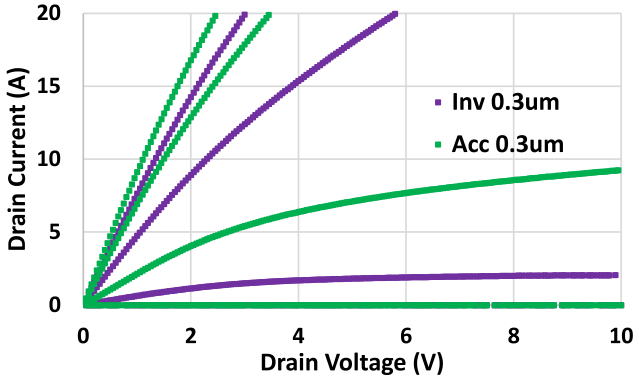

FIGURE 7. Measured output characteristics of the 1.2 kV SiC accumulation and inversion channel power MOSFETs with 0.3 μm channel length. Gate bias values of 0, 5, 10, and 15 V were used for these plots.

It is obvious that the on-state resistance at a gate bias of 15 V is smaller for the accumulation channel case. The output characteristics measured for the devices with channel length of 0.3 μm can be compared in Fig. 7. The same trend is observed in this case. The differences in specific on-resistances for these four cases require inclusion of the impact of straggle L_{SP+} as discussed in the next section.

E. CAPACITANCES

The input, output, and gate-drain capacitances for the 1.2 kV accumulation-mode SiC power MOSFETs with channel lengths of 0.3 and 0.5 μm are shown in Fig. 8 as a function of the drain bias. All capacitance values are similar for both cases. The capacitance plots for the inversion-mode devices were found to be very close to those in Fig. 8 and are not shown. The values for these capacitances at a drain bias of 1 kV are provided in Table 1 for comparison the 4 cases.

F. GATE CHARGE

The gate charge characteristics can be used to assess the switching performance of power MOSFETs [24]. They are provided in SiC power MOSFET product datasheets. The gate charge waveforms for the fabricated 1.2 kV SiC power

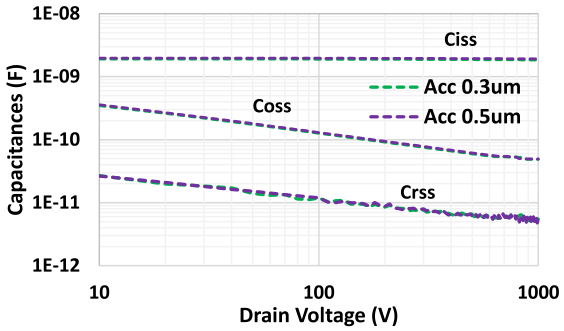

FIGURE 8. Measured input, output, and reverse-transfer capacitance (C_{rss}) for the fabricated accumulation-mode 1.2 kV SiC power MOSFETs with channel length of 0.3 and 0.5 μm.

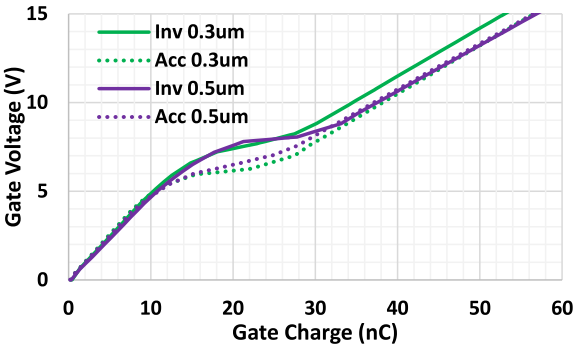

FIGURE 9. Measured gate charge waveforms for the fabricated accumulation-mode 1.2 kV SiC power MOSFETs with channel length of 0.3 and 0.5 μm.

MOSFETs were measured using a drain bias of 800 V and drain current of 10 A. The waveforms obtained for the accumulation and inversion channel devices with channel length designs of 0.3 and 0.5 μm can be compared in Fig. 9. The plateau voltages for the inversion channel devices is larger due the larger threshold voltage and smaller transconductance. The gate-drain charge for all cases is very similar as given in Table 1.

G. SUMMARY OF MEASURED DATA

A summary of the measured data for the four devices – accumulation and inversion channel, 0.3 and 0.5 μm channel length – is provided in Table 1. The specific on-resistance values are provided for the case of a gate bias of 11 V. These cases are discussed in the analysis section. The FOMs were computed using C_{rss} at a drain bias of 1000 V. It is shown in the next section that an understanding of this data requires inclusion of the impact of straggle L_{SP+}.

IV. DEVICE ANALYSIS

The analysis of the impact of straggle L_{SP+} is performed in this section using analytical models and TCAD simulations. These models were applied to the two structures illustrated in Fig. 1 with and without implant straggle to elucidate the significant differences. The straggle L_{SP+} increases the channel length by 0.33 μm and reduces the JFET width by the same amount.

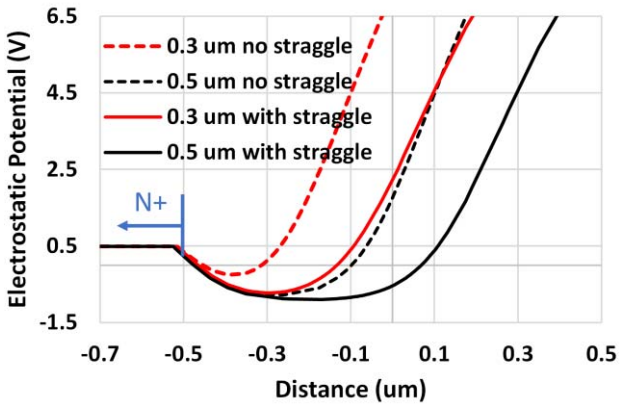

FIGURE 10. Channel potential barrier at a drain bias of 1200 V for the 0.3 and 0.5 μm channel length accumulation channel 1.2 kV SiC power MOSFETs with and without ion implant straggle of the P^+ shielding region.

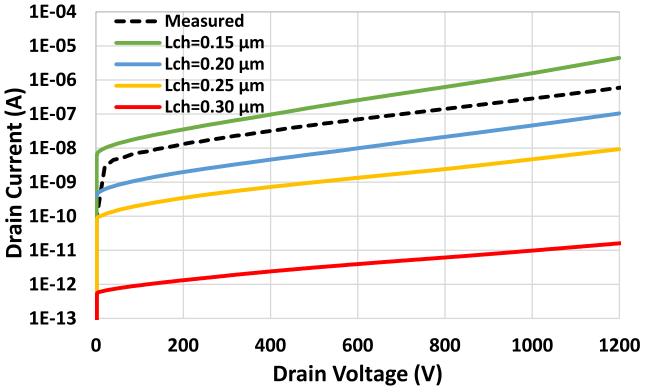

FIGURE 11. Numerical simulation results for the blocking characteristics of the 1.2 kV SiC accumulation channel power MOSFETs with mask defined channel lengths ranging from 0.3 to 0.15 μm. Implant straggle of the P^+ shielding region was included for each case.

A. BLOCKING CHARACTERISTICS

It has been previously shown that the channel potential barrier, which suppresses leakage current in the blocking mode, has a smaller value for the accumulation channel structure compared to the inversion channel structure [11]. The increase in leakage current due to the short-channel effect is consequently worse for the accumulation channel device compared to the inversion channel device. The accumulation channel structure was therefore chosen for the TCAD modeling of the blocking characteristics.

It can be observed in Fig. 3 that the leakage current for the 0.5 μm channel length case is determined by the noise limit of the wafer probing equipment. The TCAD modeling [29] was therefore performed for the 0.3 μm channel length case using commonly used SiC material parameters and models such as doping dependence and electric field dependence of mobility, incomplete ionization, Shockley-Read-Hall recombination, band gap narrowing, etc. [30]. In this paper, lateral straggle was implemented during device simulations by specifying a Gaussian profile for the P^+ implant including a 'lateral factor' in the device structure editor [29].

The potential barrier for electrons determines the leakage current for the accumulation channel power MOSFETs. The impact of the straggle L_{SP+} on the potential barrier in the channel can be obtained using TCAD simulations by using zero gate bias and a drain bias of 1200 V. Devices with mask defined channel length of 0.3 and 0.5 μm were evaluated. For the 0.3 μm case, both devices have the same cell pitch of 2.6 μm but the channel length with straggle is increased from the mask design dimension of 0.30 μm to a larger value of 0.63 μm by the straggle. The JFET region width with straggle is simultaneously reduced from the mask design dimension of 0.7 μm to a smaller value of 0.37 μm. The channel potential barrier for the devices with and without straggle L_{SP+} is shown in Fig. 10 by the red lines. It can be observed that the width of potential barrier and its magnitude is increased due to the ion implant straggle. This is beneficial to reducing the leakage current of the device designed with a 0.30 μm channel length.

The TCAD simulation results obtained for a mask defined 0.5 μm channel length case are shown in Fig. 10 by the black lines with and without including straggle L_{SP+}. The channel length is increased in this case from 0.5 to 0.83 μm. It can be observed that the width of potential barrier is increased by the implant straggle but its magnitude is not changed significantly. It can be concluded that the smaller measured leakage current observed in Fig. 3 for the larger mask defined channel length case of 0.5 μm is associated with the wider potential barrier.

Explanation for the measured leakage current in Fig. 3 for the 1.2 kV SiC power MOSFET with 0.3 μm mask designed channel length requires inclusion of the impact of the process alignment tolerance. These power MOSFETs were designed with a mask defined channel length of 0.3 μm between the implant edges of the N^+ source and P^+ shielding regions. The non-self-aligned fabrication process used for these power MOSFETs has an alignment tolerance of 0.2 μm. This implies that the mask defined channel length can be reduced by misaligned from 0.3 μm to as low as 0.1 μm. The reduction of channel length by the misalignment decreases the channel potential barrier, which results in an increase in the leakage current. In order to demonstrate this, TCAD simulations were carried out for mask defined channel lengths ranging from 0.15 to 0.30 μm in 0.05 μm increments. Implant straggle of the P^+ shielding region was included in all cases. The blocking characteristics obtained with the simulations are shown in Fig. 11 up to 1200 V. It can be seen that the leakage current increases as the mask defined channel length is reduced. A match with the experimental data for the measured 0.3 μm accumulation channel device, shown by the black dashed line, occurs for the case of a mask defined channel length between 0.20 and 0.15 μm. These results demonstrate that the leakage current for devices will vary across a wafer due to the alignment tolerance but the magnitude of the leakage current is still acceptable because

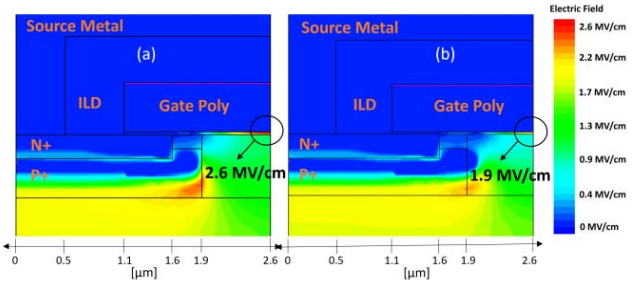

FIGURE 12. Electric field in the gate oxide in the blocking mode at 1200 V for the SiC power MOSFET structure with: (a) mask defined structure without lateral straggle; (b) structure with lateral straggle.

the implant straggle increases the channel length uniformly for all devices. These results show that the presence of the P^+ region implant straggle is an important beneficial effect to prevent very high leakage currents in power MOSFETs fabricated with 0.3 μm mask defined channel length using a non-self-aligned process.

The electric field distribution in the blocking mode, obtained with the TCAD simulations of the two 1.2 kV SiC power MOSFET structures shown in Fig. 1, was extracted at a drain bias of 1200 V. The electric field distributions for the two cases can be compared in Fig. 12. These TCAD simulation results demonstrate that the electric field in the gate oxide is significantly reduced from 2.6 MV/cm to 1.9 MV/cm by the presence of straggle L_{SP+}. This is a beneficial outcome that has not been reported in previous publications. A reduced electric field in the gate oxide under the blocking mode is desirable for achieving improved SiC power MOSFET reliability [5].

B. TRANSCONDUCTANCE

The transconductance (G_m) of the SiC power MOSFET in the drain current saturation regime of operation can be analytically computed by using [24]:

$$G_m = \frac{Z\mu_{ni}C_{OX}}{L_{CH}}(V_G - V_{TH}) \tag{1}$$

where Z is the channel width, μ_{CH} is the channel mobility, C_{OX} is the specific capacitance of the gate oxide, V_G is the gate bias, V_{TH} is the threshold voltage, and L_{CH} is the channel length. This expression can be used to assess the impact to changing the channel length from 0.3 to 0.5 μm on the mask design. For the accumulation channel cases, both devices have the same threshold voltage and channel mobility. Consequently, the G_m for the 0.3 μm channel length case should be 1.67x larger than the 0.5 μm channel length case. The measured value for the G_m at a drain current of 10 A is given in Table 1. The measured ratio of G_M for the 0.3 versus 0.5 μm channel length cases is only 1.25x, which does not match the calculated value. The effective channel lengths become 0.63 and 0.83 μm for these two designs when a straggle L_{SP+} of 0.33 μm is added to the designed channel length. This changes the ratio to 1.3x, which explains the smaller measured ratio for G_m. The same rationale applies to the inversion-channel devices with designed channel lengths of 0.3 and 0.5 μm. The measured ratio of G_m given in Table 1 for the 0.3 vs 0.5 μm channel length cases is also only 1.22x. This reduced ratio can be explained by inclusion of the implant straggle in determination of the effective channel length. This analysis demonstrates the importance of including the straggle L_{SP+} for determining the transconductance of SiC power MOSFETs, an effect not recognized in previous publications.

C. ON-STATE CHARACTERISTICS

A major goal of all SiC power MOSFET designs is to achieve a low specific on-resistance in the on-state to reduce conduction losses and the die active area [24]. It has been shown by analytical modeling that the specific on-resistance has a minimum value with varying JFET width [11], [24]. This optimization was performed when designing the 1.2 kV SiC power MOSFETs for this paper before fabrication without taking straggle L_{SP+} into account, as commonly done in previously reported devices in the literature [2], [9], [15].

The on-resistance component values for the SiC power MOSFET can be computed using the equations for the linear cell design in the textbook [24]. Among the various components, the channel, accumulation layer, JFET, and drift region components are impacted by the straggle L_{SP+}.

The specific channel resistance is given by [24]:

$$R_{CH,sp} = \frac{L_{CH}W_{cell}}{2\mu_{ni}C_{OX}(V_G - V_{TH})} \tag{2}$$

where W_{cell} is the cell width (twice the cell pitch shown in Fig. 1). The channel length with inclusion of straggle L_{SP+} is increased by 0.33 μm.

The specific JFET resistance is given by [24]:

$$R_{JFET,sp} = \frac{\rho_{JFET}x_{jP}W_{cell}}{a} \tag{3}$$

where ρ_{JFET} is the resistivity of the JFET region, x_{JP} is the depth of the P^+ shielding region, and 'a' is the effective width for vertical current flow through the JFET region. For the model without accounting for straggle L_{SP+}, the value for 'a' is given by [24]:

$$a = 2(W_{JFET} - W_0) \tag{4}$$

where W_{JFET} is the JFET width in Fig. 1(a), W_0 is the JFET depletion width due to the built-in potential of the junction between the P^+ shielding region and the JFET region. When the straggle L_{SP+} is included, this changes to:

$$a_{eff} = 2(W_{JFET} - W_0 - L_{SP+}) \tag{5}$$

which produces an increase in the JFET resistance.

The specific drift region resistance is given by [24]:

$$R_{D,sp} = \frac{\rho_D t_D W_{cell}}{(W_{cell} - a)}\ln\left(\frac{W_{cell}}{a}\right) \tag{6}$$

where ρ_D is the resistivity of the drift region, t_D is the thickness of the drift region below the P^+ shielding region.

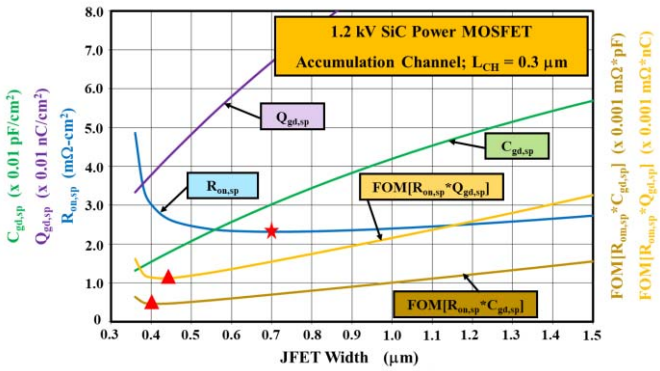

FIGURE 13. Analytically calculated specific on-resistance, gate-drain capacitance, and gate charge as a function of JFET width obtained for as-designed 1.2 kV power MOSFETs without taking ion implant straggle of the P^+ shielding region into account. The resulting FOMs are also shown.

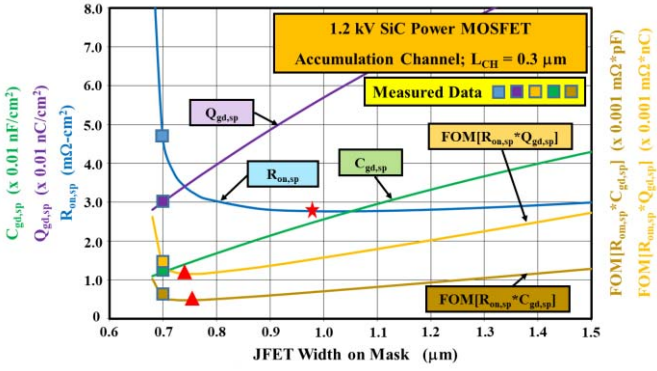

FIGURE 14. Analytically calculated specific on-resistance, gate-drain capacitance, and gate charge as a function of JFET width obtained for the 1.2 kV power MOSFETs after taking ion implant straggle of the P^+ shielding region into account. The resulting FOMs are also shown.

The value of 'a' changes to 'a_{eff}" when the straggle L_{SP+} is included, which increases the drift region resistance as well.

The electric field for the gate oxide thickness of 27 nm is 4 MV/cm at a gate bias of 11 V. This matches the electric field in the gate oxide of commonly reported SiC power MOSFETs with gate oxide thickness of 50 nm using 20 V gate bias. In contrast, a gate bias of 15 V produces an oxide electric field of 5.5 MV/cm in the on-state. The device lifetime at an electric field of 4 MV/cm exceeds 10,000 years at 175 °C while it is estimated to be over 1000 years for an electric field of 5.6 MV/cm [27]. The device lifetime for 15 V gate bias is probably sufficient from an applications perspective. However, to be conservative, a gate bias of 11 V was used for the analysis and measurements of on-resistance in this paper so that the gate oxide electric field matches that for the commonly used 50 nm gate oxide case. A channel mobility of 25 cm^2/V-s was used for the accumulation channel devices and 16 cm^2/V-s for the inversion channel devices based on the data in Fig. 2 at a gate bias of 11 V.

The specific on-resistance ($R_{on,sp}$) is plotted as a function of JFET width in Fig. 13 for case of an accumulation channel 1.2 kV SiC power MOSFET with designed channel length of 0.3 μm without taking straggle L_{SP+} into account. The minimum $R_{on,sp}$ occurs at a JFET width of 0.7 μm (indicated by the red star in the figure). This was the basis for the actual mask design used for these devices as illustrated in Fig. 1(a), as also commonly used in other published optimized devices [2], [9], [15]. However, the minimum value for $R_{on,sp}$ of 2.3 mΩ-cm^2 is much (> 2x) smaller than the measured value given in Table 1 for the fabricated devices.

The impact of the straggle L_{SP+} was analytically modeled for the accumulation-channel 1.2 kV SiC power MOSFET with mask designed channel length of 0.3 μm by increasing the channel length by 0.33 μm and shrinking the JFET width by 0.33 μm from the value on the mask. This creates the structure shown in Fig. 1(b). The resulting variation of $R_{on,sp}$ with the JFET width on the mask is shown in Fig. 14. It can be observed that the minimum $R_{on,sp}$ has shifted to a JFET width of 0.98 μm (indicated by the red star in the figure) and the minimum value has increased to 2.8 mΩ-cm^2. An important observation from this modeling is that the $R_{on,sp}$ is increased to 4.6 mΩ-cm^2 at the mask designed JFET width of 0.7 μm, which is close to the measured value for the fabricated devices as shown by the blue square symbol in Fig. 13. Consequently, the analysis in this paper demonstrates the importance of including the straggle L_{SP+} during analysis of the specific on-resistance and during the design of cells for 1.2 kV SiC power MOSFETs. This has been neglected in previous publications.

Analytical models were also applied to the accumulation channel devices for various JFET widths using a designed channel length of 0.5 μm with and without straggle L_{SP+}. The plots are not shown in the interest of space because they look similar to those shown in Fig. 13 and 14. The lowest value for $R_{on,sp}$ was observed at the same JFET width of 0.7 μm as the devices with 0.3 μm channel width but its value was larger (2.6 mΩ-cm^2) due to the increased cell pitch. This value does not match the measured value given in Table 1. However, modeling performed after including the straggle L_{SP+} gave a specific on-resistance of 5.0 mΩ-cm^2 for a designed JFET width of 0.7 μm in agreement with data in Table 1.

In addition, the analytical models were applied to the inversion channel devices with the designed channel length of 0.3 and 0.5 μm for various JFET widths with and without straggle L_{SP+}. The plots are not shown in the interest of space. The minimum $R_{on,sp}$ was observed at a JFET width of 0.7 μm for both cases with values of 2.5 and 2.9 mΩ-cm^2, respectively, when the straggle L_{SP+} was omitted. These values are much smaller than the measured values in Table 1. Modeling of the inversion-channel devices after including the straggle L_{SP+} gave a specific on-resistance of 7.7 and 9.0 mΩ-cm^2 for channel lengths of 0.3 and 0.5 μm at the designed JFET width of 0.7 μm in agreement with the measured values in Table 1.

D. DYNAMIC CHARACTERISTICS

The specific gate-drain capacitance ($C_{gd,sp}$) and specific gate-drain charge ($Q_{gd,sp}$) are dynamic parameters that serve as useful measures of the switching performance of SiC power MOSFETs [24]. For the analysis of the impact of the ion-implant straggle of the P^+ shielding region in this paper, the specific gate-drain capacitance was obtained using the equations in the textbook [24]:

$$C_{gd,sp} = \frac{a}{W_{cell}}\left(\frac{C_{OX}C_{SM}}{C_{OX}+C_{SM}}\right) \quad (7)$$

where C_{SM} is the specific capacitance of the depletion layer below the gate oxide. The specific gate-drain charge was also obtained using the equations in the textbook [24]:

$$Q_{GD,sp} = \frac{2aq\varepsilon_S N_D}{W_{cell}C_{OX}}\left[\sqrt{1+\frac{2V_{DS}C_{OX}^2}{q\varepsilon_S N_D}} - \sqrt{1+\frac{2V_{ON}C_{OX}^2}{q\varepsilon_S N_D}}\right] \quad (8)$$

where ε_S is the dielectric constant from 4H-SiC, N_D is the drift region doping concentration, and V_{DS} is the drain bias.

The $C_{gd,sp}$ and $Q_{gd,sp}$ are plotted in Fig. 13 for the device without straggle L_{SP+} to demonstrate that these parameters increase monotonically with JFET width. At the mask designed JFET width of 0.7 μm, the value for $C_{gd,sp}$ is 302 pF/cm^2 and for $Q_{gd,sp}$ is 669 nC/cm^2. These values are much larger than the measured data provided in Table 1.

The high-frequency figures-of-merit FOM[$R_{on,sp}$*$C_{gd,sp}$] and FOM[$R_{on,sp}$*$Q_{gd,sp}$] provide a measure of overall device performance inclusive of both on-state and switching losses. These FOMs calculated using the above parameters are also plotted in Fig. 13. It can be observed that these FOMs have a minimum value at a JFET width of 0.40 and 0.45 μm (indicated by the red triangles in the figure). Consequently, it may be concluded that the mask designed JFET width of 0.7 μm is too large for achieving the best overall performance according to the analysis performed without straggle L_{SP+} taken into account.

The $C_{gd,sp}$ and $Q_{gd,sp}$ values for the device after including the straggle L_{SP+} are shown in Fig. 14. By comparison of Fig. 13 and 14, it can be concluded that these dynamic parameters are significantly reduced. The reduction of the JFET width by the straggle L_{SP+} is found to reduce the magnitude of $C_{gd,sp}$ by a factor of 2.5x at the designed JFET width of 0.7 μm. In addition, the magnitude of $Q_{gd,sp}$ at the designed JFET width of 0.7 μm is reduced by a factor of 2.2x when the straggle L_{SP+} is included. The values for $C_{gd,sp}$ and $Q_{gd,sp}$ are reduced to 120 pF/cm^2 and 300 nC/cm^2, respectively, at the designed JFET width of 0.7 μm, which matches the measured values as demonstrated by the green and purple square data points in Fig. 14. This large impact of the straggle L_{SP+} on these dynamic parameters of the 1.2 kV SiC power MOSFET has not been previously recognized.

In addition, it is found that the minimum value for the FOMs occurs at a mask designed JFET width of about 0.75 μm for the accumulation-channel 1.2 kV SiC power MOSFET when straggle L_{SP+} is included. This optimum JFET width is close to the value of 0.7 μm used for the fabricated devices. Consequently, the fabricated devices are found to be optimally designed for overall high frequency performance.

Another FOM applicable to SiC power MOSFETs used in high frequency circuits is the (C_{iss}/C_{rss}) ratio. This FOM is a measure of immunity to the turn-on of the SiC power MOSFET due to a high [dV/dt] at its drain terminal, which can produce large power losses [24]. At high drain bias voltages, C_{GD} is much smaller than C_{GS} allowing a FOM[C_{GS}/C_{GD}] to be used. Using the measured values given in Table 1, the (C_{iss}/C_{rss}) ratio for the accumulation channel device with 0.3 μm channel length is 338. The value for C_{GS} can be obtained using [24]:

$$C_{gs} = \frac{2C_{OX}(L_{N+O}+L_{CH})}{W_{cell}} \quad (9)$$

where L_{N+O} is the overlap of the gate with the N^+ source region (0.5 μm in Fig. 1). The calculated value for C_{GS} using the analytical model is 40 nF/cm^2, similar to the measured values. Consequently, the calculated FOM[C_{GS}/C_{GD}] is 129, which does not match the measurements. After inclusion of the straggle L_{SP+}, the FOM[C_{GS}/C_{GD}] is 324 in agreement with the measured data - an improvement by a factor of 2.5x. This demonstrates the importance of accounting for the straggle L_{SP+} for determination of this FOM.

The results of analytical modeling of the dynamic parameters and the FOMs for the accumulation mode 0.5 μm mask designed channel length and the two cases of channel length for the inversion-mode devices were very similar to that discussed above. These results are therefore not given in the paper in the interest of space.

E. SATURATED DRAIN CURRENT

The saturated drain current ($I_{D,SAT}$) of SiC power MOSFETs at the on-state gate bias determines their short-circuit withstand time [30]. In order to demonstrate the impact of the straggle L_{SP+} on the $I_{D,SAT}$, TCAD simulations of the accumulation-channel device with designed channel length of 0.3 μm were performed to obtain the output characteristics up to large drain voltages. Device structures with and without including straggle L_{SP+} were simulated for comparison. The output characteristics obtained using the simulations for the two cases are shown in Fig. 15. The saturated drain current ($I_{D,SAT}$) is reduced by a factor of 1.17x due to the straggle L_{SP+}.

A quasi-saturation region is observed between the linear region and the saturated drain current region of operation in Fig. 15. The quasi-saturation region extends to 200 V with inclusion of lateral straggle while it extends to only 100 V without it. The stronger quasi-saturation effect occurs due the reduction of the width of the JFET region by the straggle L_{SP+}.

It has been previously shown that the short-circuit withstand time (t_{SC}) for SiC power MOSFETs is inversely proportional to the magnitude of the saturated drain current [31].

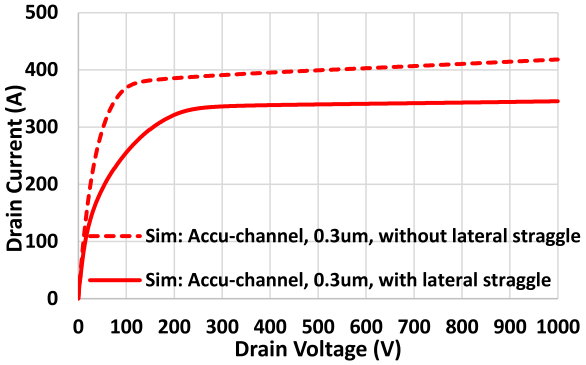

FIGURE 15. High voltage output characteristics of the accumulation-channel 1.2 kV SiC power MOSFET for a gate bias of 10 V. The cases for a designed channel length of 0.3 μm are shown with and without taking the ion-implant straggle of the P^+ shielding region into account. Device area = 0.045 cm^2.

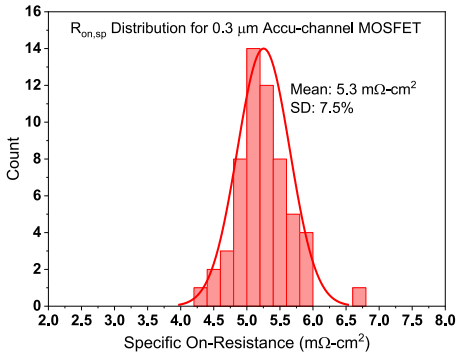

FIGURE 16. Measured statistical distribution of the specific on-resistance of 1.2 kV accumulation-channel SiC power MOSFETs with mask designed channel length of 0.3 μm at a gate bias of 10 V.

A smaller saturation current under short-circuit conditions, with the SiC MOSFET operating at the on-state gate bias, results is reducing the power dissipation. This decreases the rate of rise of die temperature during the short-circuit event, producing a longer short circuit withstand time. Consequently, the straggle L_{SP+} has a beneficial impact of improving the short-circuit time. The magnitude of the short-circuit current at a drain bias of 800 V reduces from 405 to 345 A in Fig. 15 due to the implant straggle. This will increase the short-circuit time by 17%. This a valuable attribute because the t_{SC} is less than the desired 10 μs for commercial SiC power MOSFET products.

F. DEVICE MANUFACTURING

The devices discussed in this paper were manufactured in a 6-inch commercial foundry, X-Fab, TX, using a non-self-aligned process with alignment tolerance of 0.2 μm. This may be expected to produce large parametric variations for the devices with a short mask designed channel length of 0.3 μm.

Extensive wafer-level device characterization was performed on the 1.2 kV SiC power MOSFET devices designed with 0.3 μm channel length. The statistical distribution of the specific on-resistance measured on the 76 devices on a wafer is shown in Fig. 16. The specific on-resistance has an average value of 5.3 mΩ-cm^2 at the chosen gate bias of 10 V with a standard deviation of less than 7.5%. Similarly good distributions were observed for other measured device parameters. The extension of the channel length due to the straggle L_{SP+} occurs uniformly across the wafer independently of any alignment step. The straggle L_{SP+} is therefore a beneficial effect to achieving a more uniform distribution of the device parameters, a phenomenon not recognized in previous publications.

V. CONCLUSION

There is a perception that ion-implant straggle of the P^+ shielding region (straggle L_{SP+}) does not have a significant impact on the characteristics of 1.2 kV SiC power MOSFETs [13]. The systematic analysis presented in this paper using analytical modeling and TCAD simulations demonstrates that the straggle L_{SP+} plays an important role in determining the characteristics of 1.2 kV SiC power MOSFETs. It is highlighted for the first time in this paper that the straggle L_{SP+} not only reduces the JFET width by $L_{S,P+}$ but it also increases the channel length by $L_{S,P+}$.

It is shown in this paper that the straggle L_{SP+} has the following beneficial impacts on the performance of the 1.2 kV SiC planar-gate power MOSFET: (1) The blocking characteristics are improved by reducing short-channel effects; (2) Electric field in the gate oxide is reduced in the blocking mode; (3) The gate-drain capacitance is reduced in half for the typical JFET width of 0.7 μm commonly used in devices; (4) The gate-drain charge is reduced in half for the typical JFET width of 0.7 μm commonly used in devices; (5) The FOM[$R_{on,sp}$*$C_{gd,sp}$] and FOM[$R_{on,sp}$*$Q_{gd,sp}$] are improved by a factor of 2.2x and 2.5x, respectively, for the commonly used mask designed JFET width of 0.7 μm; (6) The FOM[C_{gs}*$C_{gd,sp}$] is improved by a factor of 2.5x; (7) The saturated drain current is reduced improving the short-circuit withstand time; and (8) Device manufacturability is improved for short channel width devices made using a non-self-aligned process. On the other hand, the straggle L_{SP+} is found to have the following detrimental impacts: (1) The specific on-resistance is increased; (2) The transconductance is reduced; and (3) The quasi-saturation region is widened.

The analysis in this paper has important implications for optimizing the cell design of 1.2 kV SiC planar-gate power MOSFETs. It is shown that the JFET region width on the mask must be increased from 0.7 to 1.0 μm to achieve the lowest specific on-resistance. However, the lowest high-frequency figures-of-merit FOM [$R_{on,sp}$*$C_{gd,sp}$] and FOM [$R_{on,sp}$*$Q_{gd,sp}$] are shown to occur at a JFET width of 0.75 μm. The conclusions derived in this paper are relevant to SiC planar-gate power MOSFETs with all blocking voltage ratings because similar channel and JFET region designs are employed.

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