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SPICE Modeling and Circuit Demonstration of a SiC Power IC Technology

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ABSTRACT Silicon carbide (SiC) power integrated circuit (IC) technology allows monolithic integration of 600 V lateral SiC power MOSFETs and low-voltage SiC CMOS devices. It enables application-specific SiC ICs with high power output and work under harsh (high-temperature and radioactive) environments compared to Si power ICs. This work presents the device characteristics, SPICE modeling, and SiC CMOS circuit demonstrations of the first two lots of the proposed SiC power IC technology. Level 3 SPICE models are created for the high-voltage lateral power MOSFETs and low-voltage CMOS devices. SiC ICs, such as the SiC CMOS inverter and ring oscillator, have been designed, packaged, and characterized. Proper operations of the circuits are demonstrated. The effects of the trapped interface charges on the characteristics of SiC MOSFETs and SiC ICs are also discussed.

INDEX TERMS SiC MOSFETs, CMOS circuits, smart power IC, SPICE modeling, trapped interface charges.

I. INTRODUCTION

Currently, the main focus of the silicon carbide (SiC) technology is on discrete power devices, such as SiC vertical power metal–oxide–semiconductor field-effect transistors (MOSFETs), where the larger bandgap and higher breakdown electric field of SiC enable SiC-based power electronics to have higher output power and operate under higher temperatures compared to their silicon (Si) counterparts [1], [2]. These inherent material properties also make SiC integrated circuits (ICs) attractive in specific applications, such as subterranean and interplanetary explorations and high-temperature data acquisition [3], where the electronics need to operate under extreme-temperature and radioactive environments.

SiC IC research began in the 1990s, where the early studies were conducted on both 6H-SiC and 4H-SiC wafers with low-voltage (LV) all n-type MOSFET (NMOS) processes [4]–[6]. With material and process improvement, Raytheon Systems Limited (RSL) developed a 1.2-μm 4H-SiC complementary-MOS (CMOS) process (HiTSiC) along with its process design kit (PDK) [7]. Since then, a variety of SiC CMOS circuits have been demonstrated with the HiTSiC process [3], [8]–[13]. Recently, Murphree *et al.* demonstrated a SiC linear voltage regulator that offers competitive performance to Texas Instrument's silicon-based linear regulators [13].

SiC ICs with junction field-effect transistors (JFETs) and bipolar junction transistors (BJTs) have also been investigated for extreme-temperature (>500°C) applications. Shakir *et al.* demonstrated a SiC 555 timer and a SiC comparator that are operational under 500°C [14] with an in-house SiC bipolar junction transistor (BJT) process [15]. Hou *et al.* reported a 16x16 SiC UV image sensor array operating at 400°C with the same BJT technology [16]. Research

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groups from NASA and Ohio Aerospace Institute [17] have also demonstrated SiC JFET digital ICs that operate across a wide range of temperatures (−190°C to 812°C).

Previous SiC IC efforts focused on low-voltage and low-power applications. This work presents a SiC power IC technology that offers monolithic integration of high-voltage (HV) lateral n-type SiC power MOSFETs and LV SiC CMOS devices. The SiC power IC technology enables SiC-based application-specific integrated circuits (ASICs) where the Si-based control and driving circuits can be replaced with SiC ICs. For Si power ICs, the output current and breakdown voltage of Si lateral power MOSFETs are generally limited to 5 A∼10 A and 100 V∼200 V [18]. The breakdown voltage of Si power MOSFET can be increased to 600 V or higher with silicon-on-insulator (SOI) substrate [19]. However, the currents of such devices are limited to 1 A or less. The lateral SiC power MOSFET in the proposed SiC power IC technology is designed to obtain a blocking voltage of 600 V with a 5 A∼10 A output current and a comparable chip area as Si lateral power MOSFETs. Therefore, the overall current handling capability of the SiC power IC is increased by three to six times compared to Si power ICs. The speed of the SiC CMOS circuits is limited due to the poor surface mobility of SiC MOSFETs. However, the potential applications for such a mixed-voltage high-power SiC power IC process do not require high-frequency operations.

In this paper, an overview of the proposed SiC power IC technology is given first in Section II. Characterizations of the various types of MOSFETs are included in Section IV. Level 3 SPICE models are created based on the experimental characterizations and are demonstrated in Section V. The SPICE models are used for SiC circuit designs. Successful operations of the designed SiC CMOS circuits are shown in Section VI. Finally, the effects of the trapped interface charges on the SiC MOSFET characteristics and SiC circuits are discussed in Section VII.

II. THE PROPOSED SIC POWER IC TECHNOLOGY

Fig. 1 shows the cross-sectional views of the SiC high-voltage n-type lateral power MOSFETs (HV NMOS), low-voltage n-MOSFETs (LV NMOS), and low-voltage p-MOSFETs (LV PMOS) on the first (lot1) and the second (lot2). Both lots have been successfully fabricated on 6-inch SiC epitaxial wafers by the Analog Devices (ADI), Hillview fabrication facility. A P-top implant is implemented for the HV NMOS with the Single Reduced Surface Field (RESURF) technique to manage the surface electric field. The p-top design details and the surface electric field distributions of the HV NMOS are included in [20]. More descriptions of the fabrication processes of the two lots are included in [21] and [22], respectively.

A N-epi/N^+ substrate is used as the starting material for lot1. For lot2, the starting material is changed to a N-epi/P-epi/N^+ substrate. The thicknesses and doping concentrations of the epitaxial layers of both lots are illustrated in Fig. 1. In lot2, the p-type epitaxial layer and the P^+ isolation (designed to withstand 600 V) are used to isolate the high-voltage devices and the low-voltage blocks, allowing the various transistors to be integrated on the same substrate. As discussed in the later section, the body effect is more significant for SiC MOSFETs than Si MOSFETs. The P^+ isolation can also be applied to eliminate the body effect by allowing the bulk of any transistor to be connected to its source independently from other transistors. Three metal layers are developed in lot2 for the metal routing of complex circuits. The lot2 is also split into two batches with different oxide thicknesses (52 nm and 28 nm). Device characteristics for both lots are included in Section IV.

III. EXPERIMENTAL METHODS

The output (I_{DS}-V_{DS}), transfer (I_{DS}-V_{GS}), and blocking characteristics of the LV devices and the HV NMOS are measured at the wafer level with the Keysight B1506A semiconductor parameter analyzer. LV MOSFET arrays with different channel width (W) and channel length (L) are characterized for creating the SPICE models. SiC CMOS inverter and ring oscillators are also fabricated. The circuits in lot1 are diced, packaged, and characterized with custom-designed PCB boards and gate drivers.

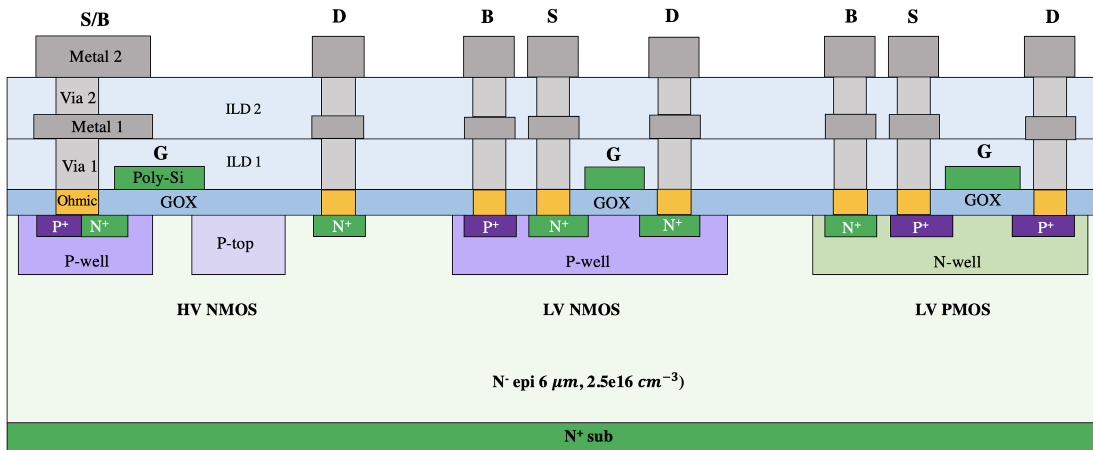
IV. DEVICE CHARACTERISTICS

A. LOW-VOLTAGE MOSFETS

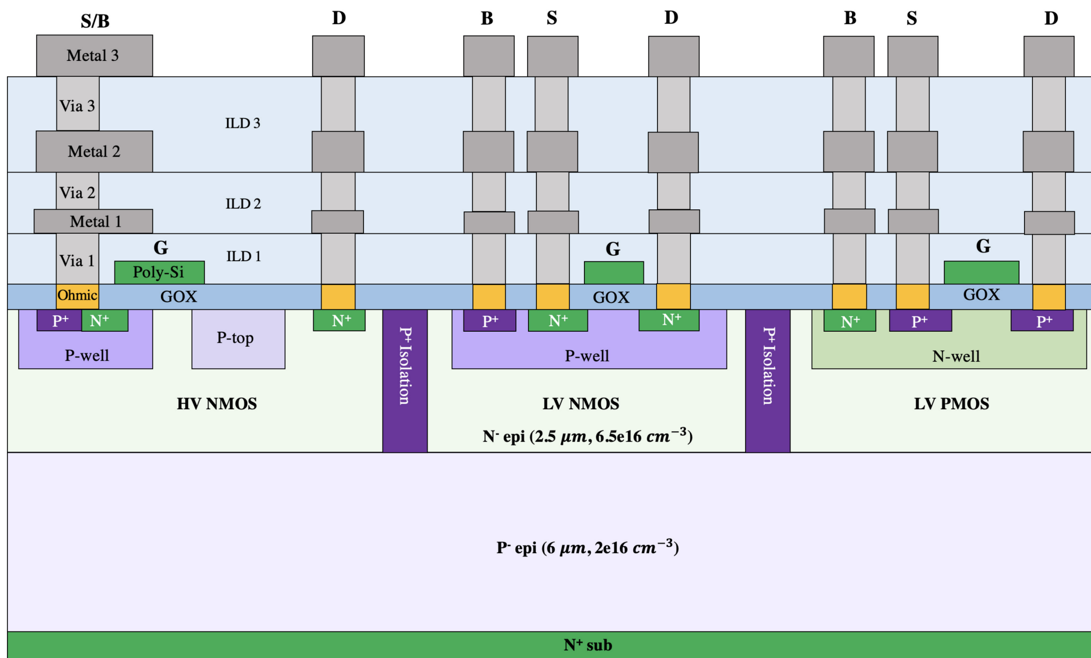
Fig. 2 shows the transfer characteristics (I_{DS}-V_{GS}) of the LV NMOS and LV PMOS in lot1 and lot2. Proper operations are obtained for the LV CMOS devices in both lots. The extracted threshold voltages (V_T) using the linear extrapolation method are marked (dots) in Fig. 2. Compared to lot1, the V_T is lowered in lot2 for the nominal design with 52 nm gate oxide. The V_T is further reduced for the split with thinner gate oxide. The output characteristics (I_{DS}-V_{DS}) of selected LV CMOS devices are included in Section V. to compare the accuracy of the SPICE models. The threshold voltages of the LV PMOS are higher than the LV NMOS in both lots. The characterizations also show that the contact resistance of the LV PMOS is much higher than the LV NMOS in both lots. As a result, the drain currents of the p-type MOSFETs at V_{DS} of −0.1 V are too low for parameter extraction. Therefore, the V_{DS} is set at −5 V for the LV PMOS. To match the current driving capability for the LV CMOS blocks, the team is optimizing the design of the LV PMOS so that the threshold voltage and the contact resistance of the LV PMOS are reduced in future lots.

B. HIGH-VOLTAGE MOSFETS

Fig. 3 shows the output and blocking characteristics of the HV NMOS in lot1 and lot2. The HV NMOS devices are the nominal designs with 52 nm gate oxide. Both the output and blocking performances of the HV NMOS in lot2 are improved when compared to the results for lot1. The blocking voltage of the lot2 HV NMOS exceeds 600 V, offering significantly higher output power comparing to the typical Si power ICs. The maximum drain current and blocking voltage



(a) Lot1



(b) Lot2

FIGURE 1. Cross-sectional views of the various types of SiC MOSFETs in (a) lot1 and (b) lot2.

of the HV NMOS in this work are significantly higher than the SiC lateral power MOSFETs reported in the recently developed SiC Bipolar-CMOS-DMOS (BCD) process [23].

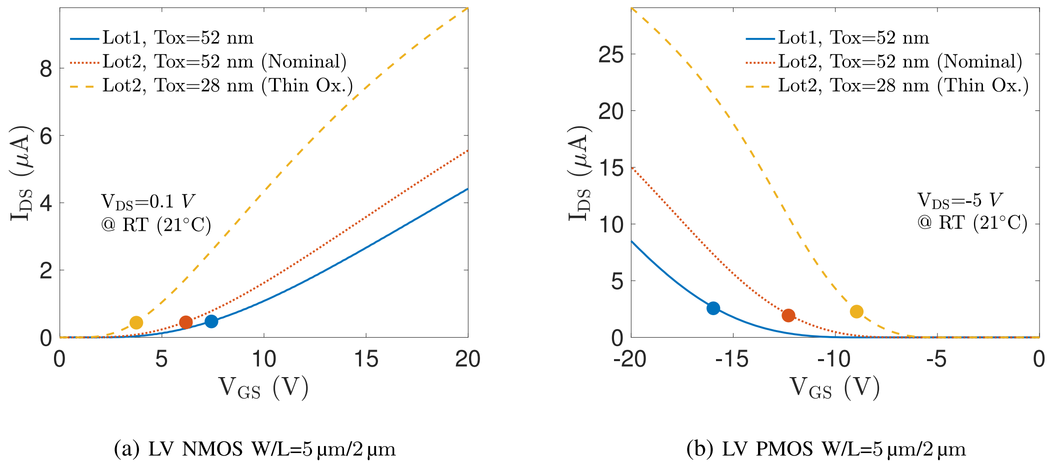
V. SPICE MODELING

This section introduces the SPICE parameter extraction sequence and demonstrates the static performances of level 3 SPICE models for selected LV CMOS devices and HV NMOS in lot2 with $T_{ox} = 52\,\text{nm}$.

A. PARAMETER EXTRACTION SEQUENCE

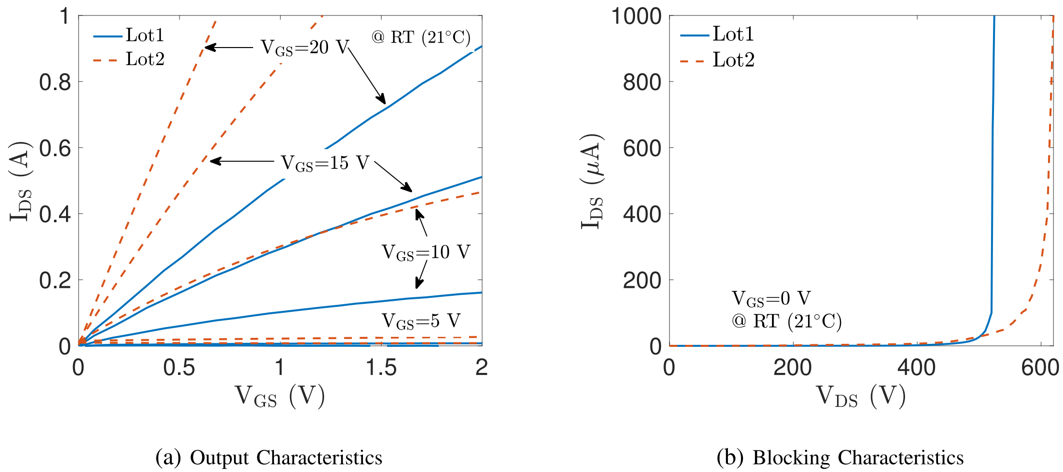
Level 3 SPICE model is selected for the initial model development for two reasons. First, its compact and physics-based model equations allow a manageable parameter extraction method. Second, the level 3 SPICE model has been successfully utilized in Si IC industry for transistors with channels longer than 1 μm [24] (also valid for the LV MOSFETs in the proposed SiC power IC technology).

The models generated for the LV MOSFETs are based on the on-wafer characterizations of the fabricated LV MOSFET arrays with different channel widths and channel lengths. The parameter extraction sequence starts with extracting the oxide thickness (TOX) from the C-V measurements. Then, the threshold at zero body bias (VTO), the bulk threshold parameter (GAMMA), the substrate doping (NSUB), and the surface bending potential (PHI) are extracted with an iterative process from the I_{DS}-V_{GS} results under different substrate biases (V_{BS}) [25]. The low-field channel mobility (UO) and surface roughness (THETA) are also extracted



(a) LV NMOS W/L=5 μm/2 μm (b) LV PMOS W/L=5 μm/2 μm

FIGURE 2. **Transfer characteristics (I_{DS}-V_{GS}) of the (a) LV NMOS and (b) LV PMOS in lot1 and lot2. The dots represent the extracted threshold voltages using the linear extrapolation method.**



(a) Output Characteristics (b) Blocking Characteristics

FIGURE 3. **(a) Output characteristics (I_{DS}-V_{DS}) and (b) blocking characteristics of the high-voltage lateral power MOSFETs in lot1 and lot2 (all nominal designs, T_{ox} = 52 nm).**

from the same data set. The number of fast interface states (NFS) is extracted from the subthreshold slopes, while the drain-induced barrier lowering (DIBL) parameter (ETA) is extracted from I_{DS}-V_{GS} curves under V_{DS}. Finally, the lateral diffusion (LD) is extracted with the Whitefield Method [26]. More details of the parameter extraction sequence and the extracted SPICE parameters are included in the Appendix.

B. STATIC PERFORMANCE OF THE SPICE MODELS

Level 3 SPICE models are constructed based on the described extraction method and incorporated into Cadence Virtuoso Analog Design Environment (ADE) for circuit simulations. Comparison between the SPICE simulations and the on-wafer characterizations for selected LV and HV MOSFETs in lot2 are shown in Fig. 4. Desirable accuracy is achieved in the triode and the saturation regions. The model created for the HV NMOS also demonstrates high accuracy for the output and blocking characteristics.

Short channel effects are observed for LV NMOS and LV PMOS with 1 μm channel length. The extracted threshold of all LV devices also show dependence on the channel lengths. Therefore, for length scaling, the SPICE models are divided into two bins (L = 1 μm and 2 μm). The SPICE models for the low-voltage MOSFETs are also binned at two channel widths (W = 5 μm and 10 μm) to increase the flexibility of the models. Eight sets of parameters are extracted and optimized to model the nominal (T_{ox} = 52 nm) LV NMOS and LV PMOS devices in lot2.

C. ON IMPROVING THE MODEL ACCURACY

Noticeable discrepancies exist at the transition between the triode and the saturation regions for the LV NMOS. The differences are caused by the trapped charges at the 4H-SiC/SiO2 interface that soften the triode-to-saturation transition [7]. The effect is not well modeled in the level 3 SPICE model since the models were originally developed for Si technology, where the interface state density is significantly lower than the state-of-the-art SiC technology.

Ahmed and his colleagues have developed BSIM4 (level 54) models with modified equations that describe the

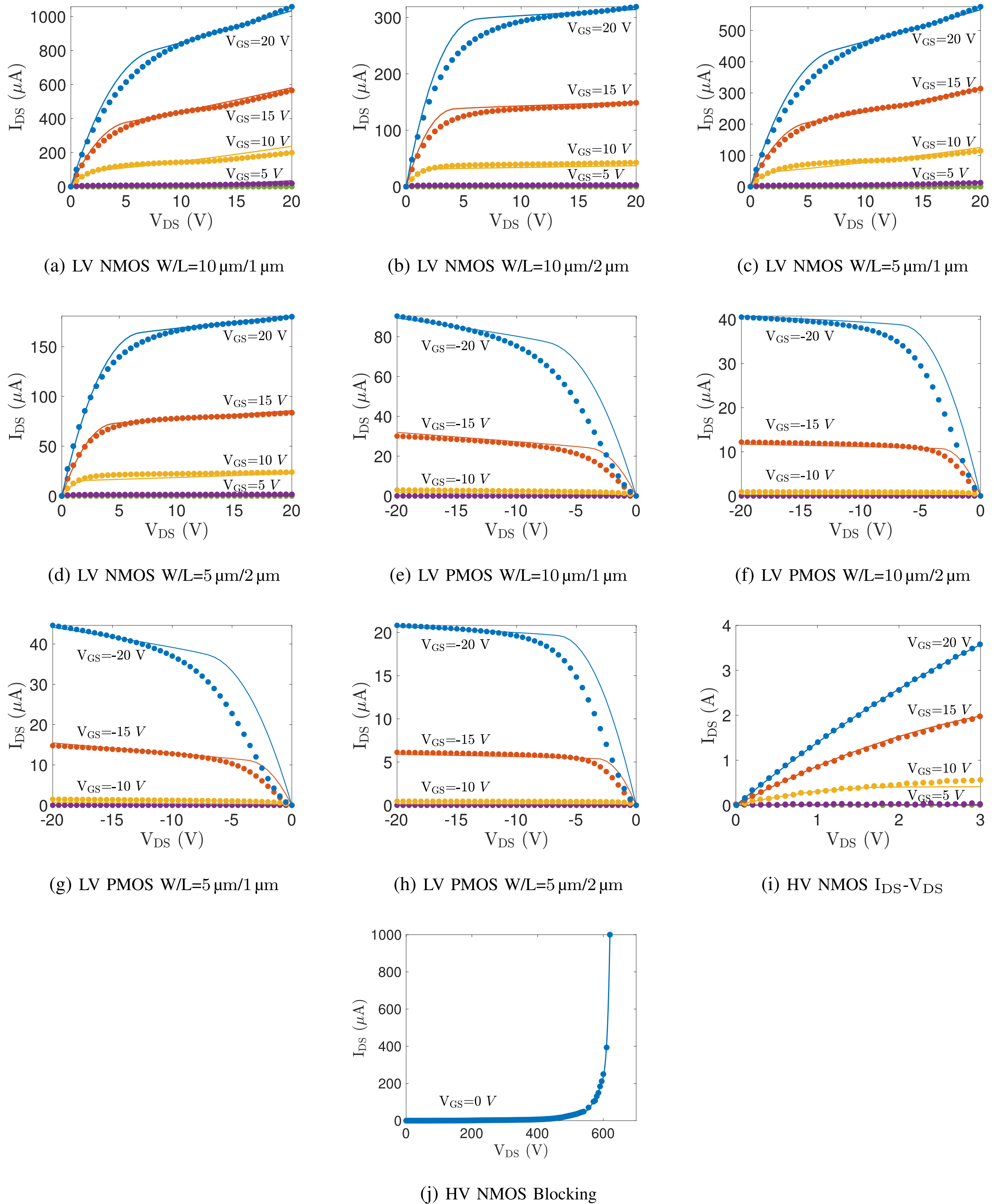


FIGURE 4. Measured (dots) and SPICE-simulated (lines) characteristics of (a)-(h) the LV MOSFETs and (i)-(j) the HV power MOSFETs in lot2.

effects of the trapped interface charges on SiC MOSFET characteristics [7]. With the added equations, the modeling accuracy of the triode-to-saturation transition and the body-bias-dependent transconductance of SiC CMOS devices are significantly improved. Although the BSIM4 models are more accurate for SiC MOSFETs and are open-source, considering the complexity of the characterization and parameter extraction process, it is more beneficial to adopt the models for a later stage of the proposed SiC power IC technology when the fabrication process is fully matured. When

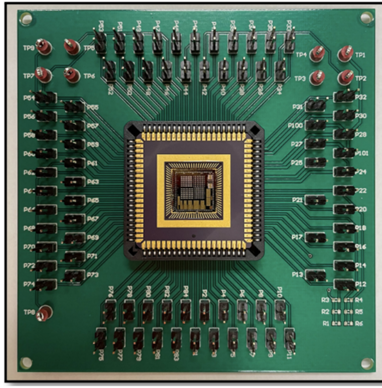


FIGURE 5. A customized PCB board designed for the testing the circuits on the 84-pin ceramic CQF J-lead package (center).

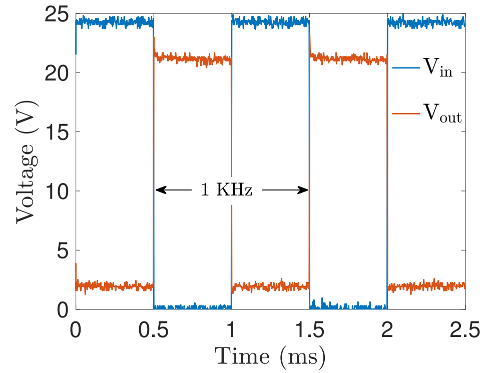
fabrications challenges such as reducing the threshold voltage and contact resistance of the LV PMOS and lowering the interface state densities are met, the BSIM4 models and their extraction methods will be adopted to improve the simulation accuracy for the future circuit designs of the proposed SiC power IC technology.

VI. CIRCUIT DEMONSTRATIONS

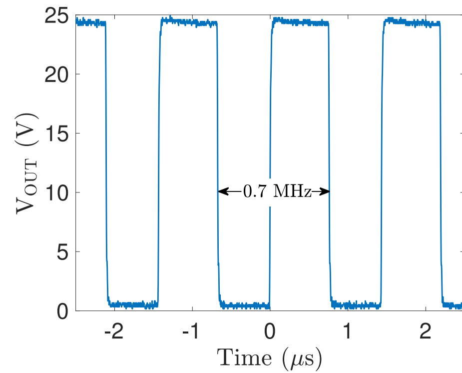
Various circuits are designed with the level 3 SPICE models [27], including a SiC CMOS inverter and a 1 MHz SiC ring oscillator. The fabricated circuits in lot1 have been diced and packaged with 84-pin ceramic CQF J-lead packages from QP Technologies and tested with the customized PCB board that is shown in Fig. 5. The dynamic operations of the SiC inverter and ring oscillator are first characterized to demonstrate the speed of operation of the digital circuits in the proposed SiC power IC technology. The circuits in lot2 are in the process of dicing and packaging. The characterization results will be included in future publications.

Fig. 6 shows the waveform of the SiC inverter and the ring oscillator. Proper operations are shown for both circuits. The target frequency of the SiC ring oscillator is 1 MHz, while the measured oscillation frequency is 0.7 MHz. The discrepancy comes from the initial SPICE models that are based on device simulations (Sentaurus TCAD device simulator) instead of actual measurement results [27]. The dynamic simulation accuracy is expected to improve with C-V characterizations of the fabricated MOSFET arrays. The output swing of the inverter is reduced compared to the oscillator. This is because the 0.5 µm channel devices used in the inverter have high drain-source leakage currents, thus reducing the output swing. Both LV NMOS and LV PMOS with channel lengths of 1 µm or longer show no drain-source leakage current issues. Therefore, 1 µm has been defined as the minimum channel length with the current capability of the fabrication process.

The oscillation frequency of the SiC ring oscillator increases at elevated temperatures, as shown in Fig. 7. This increase is due to the re-emission of the trapped electrons at



(a) SiC CMOS Inverter



(b) SiC Ring Oscillator

FIGURE 6. Output waveform of (a) the SiC CMOS inverter and (b) the 1 MHz (target frequency) SiC ring oscillator in lot1 at room temperature (21°C). The power supply voltage is 25 V.

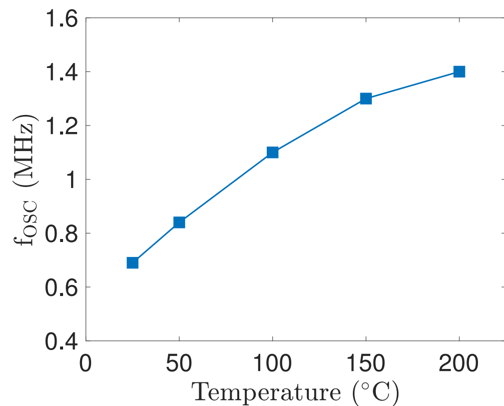


FIGURE 7. Oscillating frequency of the 1 MHz SiC ring oscillator in lot1 as a function of the ambient temperatures. The power supply voltage is 25 V.

higher temperatures, which leads to a higher drive current in SiC MOSFETs. A detailed discussion of this behavior is included in the next Section.

VII. EFFECTS OF TRAPPED INTERFACE CHARGES

A. EFFECTS ON THRESHOLD VOLTAGE

A high density of interface states forms during the oxidation process of SiC MOSFETs. During device operation, part of

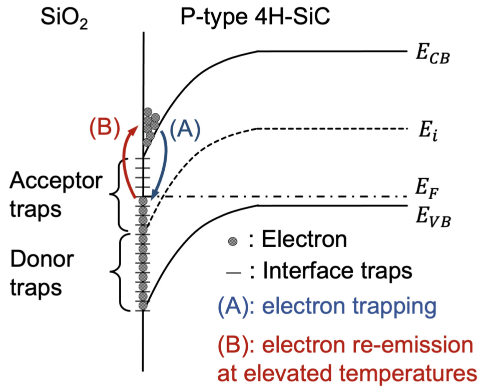


FIGURE 8. Band diagram showing the trapping and re-emission of electrons at the 4H-SiC/SiO2 interface.

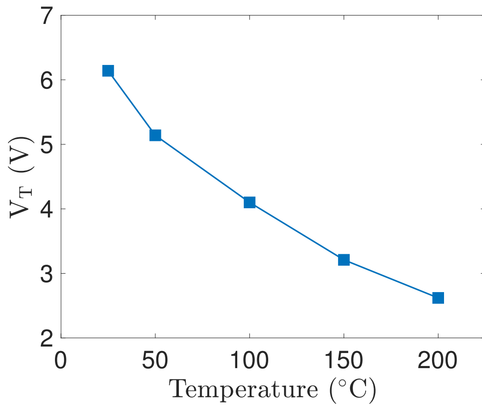


FIGURE 9. Threshold voltage vs. temperature for the 10 μm/1 μm LV NMOS in lot1.

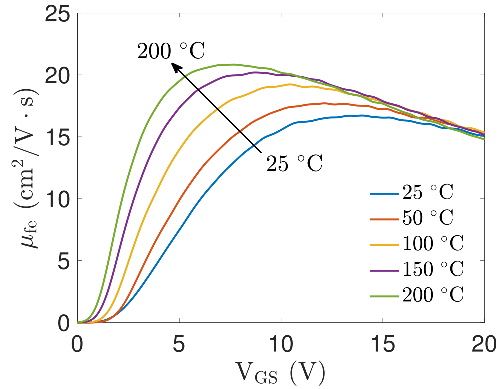


FIGURE 10. Extracted electron field-effect mobility (μ_{fe}) from 25°C to 200°C for the 10 μm/1 μm LV NMOS in lot1.

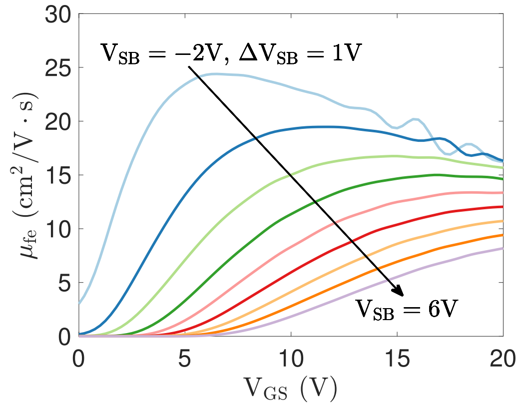


FIGURE 11. Extracted electron field-effect mobility with different substrate biases at room temperature (21°C) for the 10 μm/1 μm LV NMOS in lot1.

the electrons that flow across the channel are trapped at the interface, as illustrated by process (A) in the energy band diagram (Fig. 8). At elevated temperatures, the electrons that are trapped at the interface re-emit back to the conduction band, as illustrated by process (B). The re-mission of the electrons at high temperatures decreases the charges trapped at the interface and lowers the threshold voltages of SiC MOSFETs [28], [29]. More detailed discussion on the nature of the interface traps and the trapping mechanisms are included in [30]. Fig. 9 shows over 3 V of threshold voltage reduction from 25°C to 200°C for the 10 µm/1 µm LV NMOS in lot1.

It is worth noting that Si MOSFETs observe a similar trend, i.e., lower threshold voltages at elevated temperatures. However, the trend is much stronger in SiC MOSFETs due to the higher interface state density.

B. EFFECTS ON CHANNEL MOBILITY

For SiC MOSFETs, the field-effect electron mobility (μ_{fe}) in the channel region is much lower (20∼40 $cm^2 V^{-1} s^{-1}$) compared to the bulk mobility (∼800 $cm^2 V^{-1} s^{-1}$) due to fewer electrons in the inversion layer and a combination of different scattering mechanisms caused by the trapped interface charges. Like V_T, μ_{fe} is also temperature-dependent because of the re-emission of the trapped electrons at elevated temperatures. Fig. 10 demonstrates significant increases of the extracted μ_{fe} at higher temperatures and low V_{GS}. This behavior is similar to Si MOSFET. However, at high V_{GS}, the extracted μ_{fe} of SiC MOSFETs becomes far less dependent on temperature as shown in Fig. 10. The behavior is different than Si MOSFETs, which exhibit degraded mobility at higher temperatures and higher V_{GS}.

Depending on the substrate bias (V_{SB}), the inversion layer carriers are pushed into or pulled away from the interface, which results in enhanced or reduced scattering. This phenomenon is illustrated in Fig. 11, where the μ_{fe} is extracted at room temperature (21°C) with varying substrate biases. Over 3x change in maximum μ_{fe} is observed with V_{SB} ranging from −2 V to 6 V. Because of higher interface quality, μ_{fe} of Si MOSFETs will show less dependence on V_{SB} than the results demonstrated in Fig. 11. It is worth pointing out that in the proposed SiC Power IC technology, the body effect of the SiC MOSFETs can be eliminated by allowing the bulk of any transistor to be connected to its source independently from other transistors, as discussed in Section II.

C. EFFECTS ON CIRCUIT PERFORMANCE

The oscillation frequency of the CMOS ring oscillator depends on the delay of each inverter in the chain, which

is ultimately determined by the current driving capability of the MOSFETs at higher values of V_{GS} (i.e., higher driving current means lower delay and higher oscillation frequency). The driving current of a MOSFET is a function of the threshold voltage and the carrier mobility. For SiC MOSFETs with high V_{GS}, the carrier mobility is almost insensitive to temperature, but the threshold voltage drops significantly at higher temperatures, and thus will dominate the behavior of the drive current of the device. Consequently, the drive current of the SiC LV CMOS devices with high V_{GS} increase at higher temperatures, which results in smaller inverter delay and higher oscillation frequency in the ring oscillator. This trend is different in Si MOSFETs since the carrier mobility degrades decreases at higher temperatures with higher V_{GS}. As a result, the drive current of the devices drops at higher temperature, which typically leads to lower oscillation frequency of the ring oscillators. Therefore, circuit designers need to consider the difference between SiC and Si MOSFETs in terms of how temperature affects both the threshold voltage and channel mobility.

VIII. CONCLUSION

Level 3 SPICE models have been generated based on experimental characterizations for the proposed SiC Power IC Technology. The models are binned at different channel widths and channel lengths to maximize the model accuracy and flexibility. SiC circuits such as CMOS inverter and ring oscillators are designed using the SPICE models. Proper operations are presented for the SiC circuits. More complex circuits such as a 600 V SiC half-bridge power stage with fully integrated SiC CMOS gate drivers have also been designed and are in fabrication.

The trapped charge at the 4H-SiC/SiO_2 interface is demonstrated to soften the transition between the triode and the saturation regions. As a result, the accuracy of the SPICE models is affected in the transition region. The trapped interface charges also impact the characteristics of SiC MOSFETs under different temperature and bias conditions, affecting the operation of SiC ICs. Therefore, further efforts, such as adopting the SiC BSIM4 models, are warranted to model the effects of the trapped interface charges and improve the SPICE model accuracy when the proposed SiC power IC process is mature.

APPENDIX
SPICE PARAMETER EXTRACTIONS

This Appendix describes the parameter extraction methods for the critical SPICE model parameters.

A. EXTRACTION OF VTO, GAMMA, NSUB, AND PHI

VTO, GAMMA, NSUB, and PHI are extracted from the I_{DS}-V_{GS} results with different substrate biases (V_{SB}). The iterative process illustrated in Fig. 12. PHI is first calculated with

$$PHI = 2\phi_f = \frac{2K_BT}{q}\ln\left(\frac{NSUB}{n_i}\right), \quad (1)$$

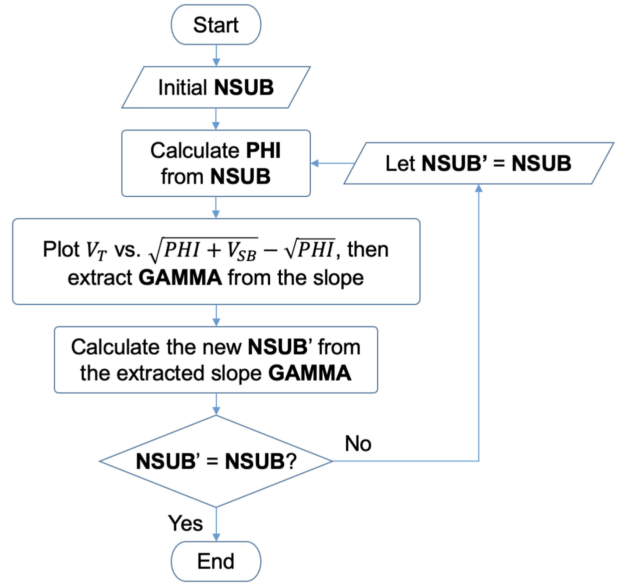


FIGURE 12. Flow chart illustrating the iterative process of extracting VTO, NSUB, PHI, and GAMMA.

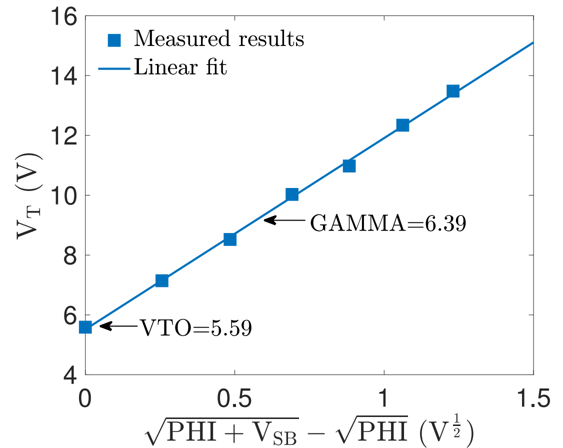


FIGURE 13. Extracting VTO and GAMMA for the 10 μm/1 μm LV NMOS in lot2.

where ϕ_f is the band bending potential and the initial value of NSUB comes from the device design. Threshold voltage of a four-terminal MOSFET under different V_{SB} is described by

$$V_T = VTO + GAMMA \times \left(\sqrt{PHI + V_{SB}} - \sqrt{PHI}\right). \quad (2)$$

Therefore, VTO and GAMMA can be extracted from the y-intercept and slope of the V_T vs. $(\sqrt{PHI + V_{SB}} - \sqrt{PHI})$ plot as shown in Fig. 13. Then, a new NSUB value is calculated from the extracted GAMMA with

$$NSUB = \frac{GAMMA^2}{2q\varepsilon_{SiC}}\left(\frac{\epsilon_{ox}}{t_{ox}}\right)^2. \quad (3)$$

The new NSUB value is used to repeat the iterative process until the process converges to a final set of parameters.

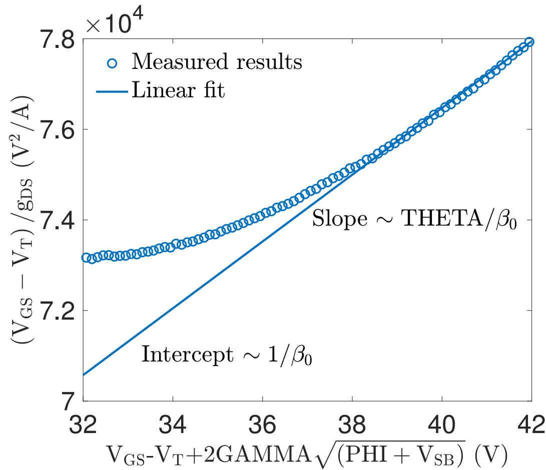


FIGURE 14. Extracting UO and THETA for the 10 μm/1 μm LV NMOS in lot2.

B. EXTRACTION OF UO AND THETA

The same set of I_{DS}-V_{GS} results are used to extract UO and THETA. The level 3 SPICE model accounts the effect of the surface roughness on the channel mobility under higher gate voltages. The simplified level 3 drain-source current equation under linear region is written as

$$I_{DS} = \frac{\beta_o(V_{GS} - V_T)V_{DS}}{1 + THETA\big(V_{GS} - V_T + 2GAMMA\sqrt{PHI + V_{SB}}\big)}, \tag{4}$$

where $\beta_o = UO \cdot C_{ox}\frac{W}{L}$. Eq. (4) can be re-written into

$$\frac{V_{DS}}{I_{DS}}(V_{GS} - V_T) = \frac{1}{\beta_o} + \frac{THETA}{\beta_o} \times \Big(V_{GS} - V_T + 2GAMMA\sqrt{PHI + V_{SB}}\Big). \tag{5}$$

Therefore, UO (from β_o) can be extracted from the y-intercept of (5), while THETA can be calculated from the slope. The method is applied to the 10 μm/1 μm LV NMOS as shown in Fig. 14.

C. EXTRACTION OF NSF

NSF is extracted from the subthreshold slope (SS) that is defined as

$$SS = \ln 10\left(\frac{\partial \ln I_{DS}}{\partial V_{GS}}\right)^{-1} = n \cdot 2.3 \cdot \frac{K_B T}{q} = n \cdot 60\text{mV/dec}, \tag{6}$$

where n is described as

$$n = 1 + \frac{C_D + qNFS}{C_{ox}}. \tag{7}$$

NFS can be calculated from n if SS is known.

The extracted and optimized level 3 SPICE model parameters for the 10 μm/1 μm LV NMOS in lot1 and lot2 are included in Table 1.

TABLE 1. Extracted SPICE parameters.

Parameter	Unit	Lot1 W/L=10/1	Lot2 W/L=10/1
VTO	(V)	6.4	5.6
GAMMA	($V^{\frac{1}{2}}$)	6.1	6.4
PHI	(V)	3.3	3.3
NSUB	(cm^{-3})	2.2×10^{18}	1.2×10^{18}
UO	($cm^2/V \cdot s$)	18.1	20.4
THETA	(V^{-1})	6.6×10^{-3}	7.4×10^{-3}
NFS	(cm^{-2})	1.2e13	7.4e12

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