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Sub-10 nm Top Width Nanowire InGaAs Gate-All-Around MOSFETs With Improved Subthreshold Characteristics and Device Reliability

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ABSTRACT In this article, sub-10 nm top width nanowire $In_{0.53}Ga_{0.47}As$ gate-all-around (GAA) MOSFETs with improved subthreshold characteristics and reliability are demonstrated. These devices exhibit a significant improvement in the subthreshold performances with subthreshold swing (SS) of 70 mV/dec, drain induced barrier lowering (DIBL) of 46 mV/V, and off-current (I_{off}) of 1.6×10^{-4} μA/μm for InGaAs GAA MOSFETs. Effective control of short channel effects (SCEs) is confirmed by the error bar of statistical variation analysis. Under gate bias stress, a low degradation of SS and threshold voltage (V_{th}) shift has been achieved due to N_2 RP treatment of the InGaAs GAA MOSFETs. The superior performance can be attributed to the strong electrostatic control and high quality of high-κ/InGaAs interface, originating from shrinking nanowire width and RP passivation effects. These results show the developed GAA MOSFET devices have good potential for future low-power high-switching speed CMOS logic applications.

INDEX TERMS Gate all around, HfO_2, SCEs, RP treatment, InGaAs, MOSFET.

I. INTRODUCTION

As the technology nodes down scaling to the sub-10 nm, suppressing short channel effects (SCEs) has become a strict challenge to overcome the serious threshold voltage (V_{th}) roll-off, stronger drain induced barrier lowering (DIBL), and drastic subthreshold swing (SS) degradation [1]. To address these issues, gate-all-around (GAA) field-effect transistor has been proposed, and has shown resistant to SCEs [2]–[7]. However, for the III-IV based transistors, severe subthreshold performance degradation is a crucial issue correlated to the strong band to band tunneling (BTBT) of the small bandgap material and a considerable number of traps generated at the high-κ and semiconductor interface which accounted for trap-assisted tunneling (TAT) and Frenkel-Poole emission in scaled gate oxide [8]–[11]. For the ultrathin thickness of hafnium oxide (HfO_2), the flat band voltage shift resulting from stress-induced interface traps is one of the key problems need to be overcome [12].

In this work, $In_{0.53}Ga_{0.47}As$ GAA MOSFETs have been fabricated with the inclination angle near 70° of channel sidewall in [10] direction with nanowire top width of 8 nm and using a simple RP treatment with one gas ambient (N_2) in order to improve not only the gate control but also the interface quality of the high-κ material and InGaAs. The

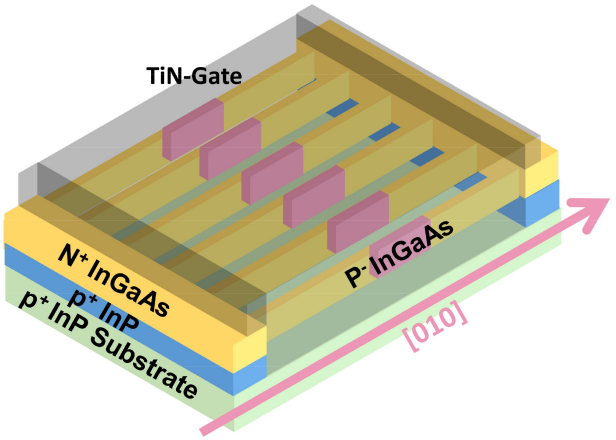

FIGURE 1. Schematic image of the typical $In_{0.53}Ga_{0.47}As$ gate-all-around (GAA) device.

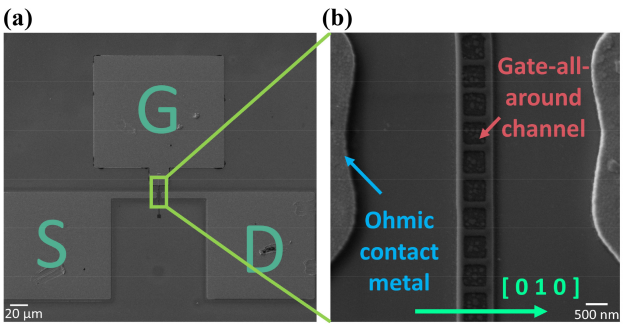

FIGURE 2. Top view SEM image of (a) typical $In_{0.53}Ga_{0.47}As$ GAA device, and (b) fabricated $In_{0.53}Ga_{0.47}As$ GAA channel followed by [10] direction.

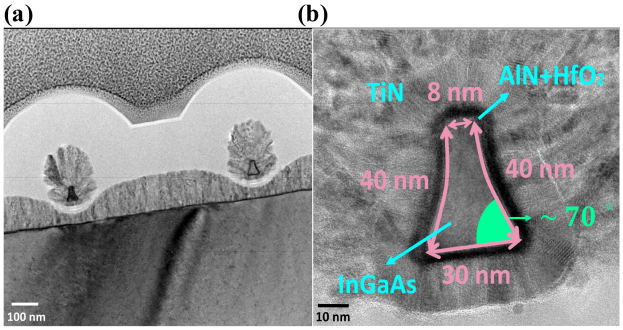

FIGURE 3. Cross-sectional HRTEM image of (a) fabricated $In_{0.53}Ga_{0.47}As$ GAA device, and (b) $W_{nw,top}$ = 8 nm, and sidewall inclination angle (θ) ~ 70° $In_{0.53}Ga_{0.47}As$ channel.

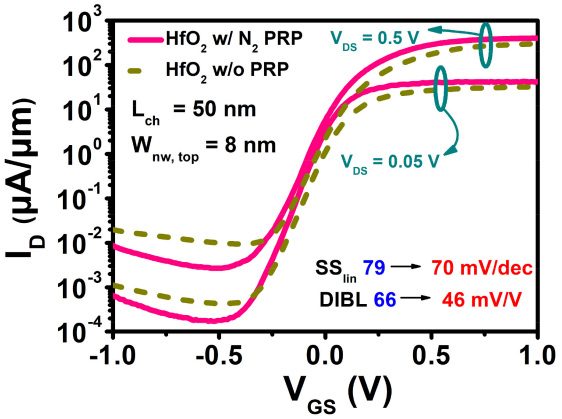

FIGURE 4. I_D-V_{GS} transfer characteristics of the HfO_2 w/N_2 and w/o N_2 RP treatment for L_{ch} = 50 nm, $W_{nw,top}$ = 8 nm $In_{0.53}Ga_{0.47}As$ GAAFETs.

effectiveness of the RP treatments with N_2 and N_2/NH_3 are quite similar in term of the interface trap density (D_{it}) value. Reduced nanowire top width can enhance the gate controllability further improve the SCEs. Additionally, comparing to device fabricated without N_2 RP passivation, N_2 RP treated $In_{0.53}Ga_{0.47}As$ GAA MOSFETs have shown a significant enhancement on SS, DIBL, leakage current, and reliability properties.

II. DEVICE FABRICATION

Fig. 1 shows the schematic image of the $In_{0.53}Ga_{0.47}As$ GAA device. Figs. 2(a) and (b) show the top view and zoom-in SEM images of a typical $In_{0.53}Ga_{0.47}As$ GAA MOSFETs fabricated. Details of the process flow can be referenced elsewhere [7]. After source/drain (S/D) regions were defined and processed, nanowire was created following the (010) orientation which has the highest aspect ratio of the $In_{0.53}Ga_{0.47}As$ material [3]. Dry etching and wet etching techniques were applied to create the bottomless structure. $In_{0.53}Ga_{0.47}As$ and InP were etched using the ICP to form the fin patterns, and citric acid was used to scale the fin width and reduce surface roughness of the $In_{0.53}Ga_{0.47}As$ channel. Subsequently, to fabricate the gate-all-around structure, $In_{0.53}Ga_{0.47}As$ channel bottom etching was achieved by diluted HCl solution to selective etch the InP layer which was underneath the $In_{0.53}Ga_{0.47}As$ layer. After the sulfur pretreatment $(NH_4)_2S$ solution treatment, the PEALD-AlN interfacial passivation layer was deposited and followed by ALD-HfO_2 layer deposition with the equivalent oxide thickness (EOT) of 0.8 nm and the surface of the dielectric layers were treated using an in-situ N_2 RP process which were performed at plasma power of 150 W for 5 minutes at 250°C in the same Fiji-G2 ALD chamber. Immediately, 10-nm PEALD-TiN was deposited to wrap the $In_{0.53}Ga_{0.47}As$ channel in the Fiji-202 ALD chamber. Control sample without N_2 RP treatment was also fabricated for comparison. Fig. 3(a) shows the cross-sectional high resolution transmission microscopy image (TEM) of the fabricated $In_{0.53}Ga_{0.47}As$ GAA device. The finished devices feature a channel length (L_{ch}) of 50 nm, top width ($W_{nw,top}$) of 8 nm, bottom width ($W_{nw,bottom}$) of 30 nm, nanowire height (H_{nw}) of 40 nm, and the sidewall inclination angle (θ) with respect to the surface of the nanowire bottom was nearly 70° (Fig. 3(b)).

III. RESULTS AND DISCUSSION

Fig. 4 presents the subthreshold characteristics of the $In_{0.53}Ga_{0.47}As$ GAA MOSFETs with and without N_2 RP treatment. The current in the figure is normalized to the

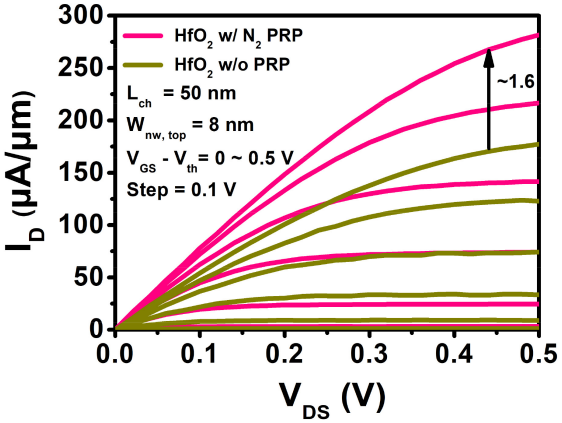

FIGURE 5. I_D-V_{DS} transfer characteristics of the HfO_2 w/N_2 and w/o N_2 RP treatment $In_{0.53}Ga_{0.47}As$ GAAFETs.

perimeter of the total effective channel width $W_{tot} = (2\times H_{nw}+W_{nw,top}+W_{nw,bottom}) \times$ (No. of wire). Comparing to the control sample, RP treated devices exhibit considerable performance improvement. Subthreshold swing (SS) decreases from 79 to 70 mV/dec, drain induced barrier lowering (DIBL) reduces from 66 to 46 mV/V, OFF-current (I_{off}) was suppressed from 4.3×10^{-4} to 1.6×10^{-4} μA/μm, ON/OFF current ratio increased from 7.6×10^4 to 2.5×10^5, a substantial improvement of ON-current was observed. Furthermore, benefiting from the nearly 70° sidewall inclination angle, the leakage current for the $In_{0.53}Ga_{0.47}As$ GAAFETs with and without N_2 RP treatment were lower than 5×10^{-4} μA/μm. This means the inclination angle of 70° sidewall can help to confine the electron density more effectively. Great improvements in the subthreshold swing were observed for the N_2 RP treated $In_{0.53}Ga_{0.47}As$ GAA MOSFETs due to the nitrogen passivation effects. Nitrogen atoms generated in the RP process can help to passivate not only the oxygen vacancies in the HfO_2 film but also the dangling bond at the interface between the high-κ materials and the III-V semiconductors, contributing to the significant reduction of the D_{it} [7], [9], [13]–[15]. This may aggressively suppress the Frenkel-Poole emission and trap-assisted tunneling [11]. In addition, the decreased D_{it} can effectively suppress the trap-assisted tunneling (TAT) leakage current from gate to drain [16]. Fig. 5 shows the output characteristics for the normalized drive current of the $In_{0.53}Ga_{0.47}As$ GAA MOSFETs with and without N_2 RP treatment. After the N_2 PRP treatment, the result shows superior improvement in the I_D at V_{GS}-V_{th} = 0.5 V and V_{DS} = 0.5 V from 176 to 282 μA/μm (increased up to 160%), mainly due to the high interface quality between the high-κ dielectric and $In_{0.53}Ga_{0.47}As$. Figs. 6(a) and (b) show the subthreshold swing in the linear regime (SS_{lin}) and DIBL error bar of statistical variation for 25 $In_{0.53}Ga_{0.47}As$ GAA MOSFET devices with and without N_2 RP treatment. These results show that the N_2 RP treated devices exhibit dramatically improvement in the average SS_{lin} which decreased from 74 to 67 mV/dec and the average DIBL

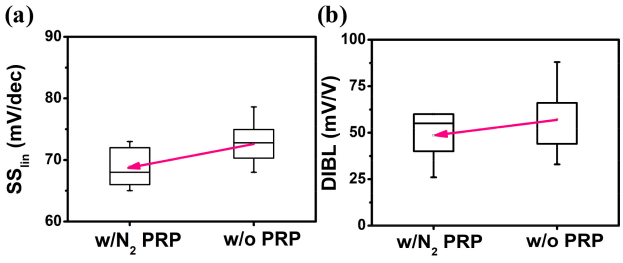

FIGURE 6. (a) Minimum SS in linear regime, and (b) DIBL versus w/N_2 and w/o N_2 RP treatment $In_{0.53}Ga_{0.47}As$ GAAFETs.

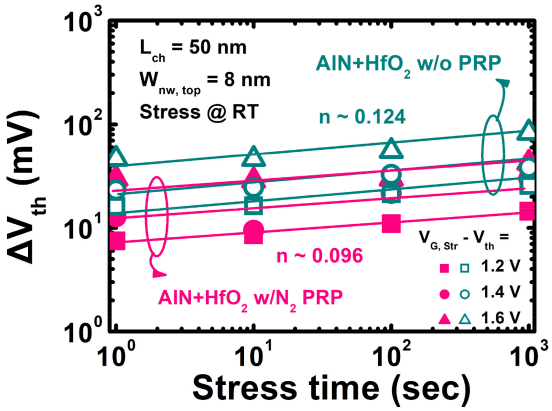

FIGURE 7. Threshold voltage shift (ΔV_{th}) as a function of the stress time w/N_2 and w/o N_2 RP treatment $In_{0.53}Ga_{0.47}As$ GAAFETs.

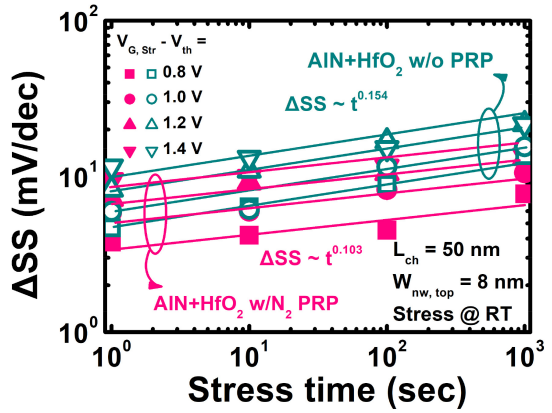

FIGURE 8. Subthreshold swing shift (ΔSS) as a function of the stress time w/N_2 and w/o N_2 RP treatment $In_{0.53}Ga_{0.47}As$ GAAFETs.

which dropped from 62 to 47 mV/V. The suppressing of the SCEs was demonstrated by the N_2 surface passivation. The positive bias temperature instability (PBTI) characteristics were carried out with positive constant voltage stress (CVS). Fig. 7 shows the threshold voltage shift (ΔV_{th}) as a function of the stress time of $In_{0.53}Ga_{0.47}As$ GAA MOSFETs with and without N_2 RP treatment under different gate voltage stress from $V_{G,Stress} - V_{th}$ = 1.2 V to 1.6 V at room temperature (RT). After N_2 RP treatment, the power law factor n value ($\Delta V_{th} \propto t^n$) changes from 0.124 to 0.096. Fig. 8 compares the N_2 RP treated $In_{0.53}Ga_{0.47}As$ GAA FETs

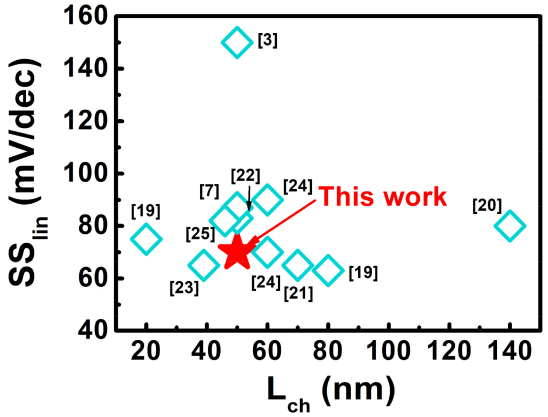

FIGURE 9. Benchmark plots of SS as a function of L_{ch} in this work. The data are compared with other state-of-the-art InGaAs GAAFETs devices.

with control sample for the time evolution of subthreshold swing shift (ΔSS) at different stress voltages of 0.8 to 1.4 V. The n value of time exponent was changed from 0.154 to 0.103. It is reasonable since less traps were generated and very rare trapping/detrapping processes occur under gate voltage stress [17], [18]. It indicates superior interface quality between the oxide and semiconductor obtained in $In_{0.53}Ga_{0.47}As$ GAA MOSFETs with N_2 RP treatment and shows surprising progress of the InGaAs GAA MOSFETs reliability with scaled oxide. Fig. 9 benchmarks the minimum SS in the linear regime versus difference channel lengths (L_{ch}) achieved in this work with the state-of-the-art InGaAs GAA MOSFETs. The N_2 RP treated $In_{0.53}Ga_{0.47}As$ GAA MOSFETs with scaled EOT showed considerable improvement in the SCEs immunity.

IV. CONCLUSION

InGaAs GAA MOSFETs with sub-10 nm top width nanowire with enhanced subthreshold performance and improved reliability were characterized. The nanowire device fabricated with sidewall inclination angle nearly 70° N_2 RP treatment showed great channel controllability for the InGaAs GAA MOSFETs. SS of 70 mV/dec, DIBL of 46 mV/V, I_{off} of 1.6×10^{-4} μA/μm, and high I_{on}/I_{off} ratio of 2.5×10^{5} were achieved. These results indicate that InGaAs GAA devices are promising for future low-power high-switching speed logic applications.

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