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A Low-Power CMOS Image Sensor With Multiple-Column-Parallel Readout Structure

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ABSTRACT This paper presents a low-power multiple-column-parallel (MCP) readout CMOS image sensor (CIS) in terms of its structural features. Because each column in an MCP unit performs analog-to-digital (A/D) conversion sequentially, the columns have their own operating periods before and after A/D conversion. Upon completion of A/D conversion in each column, a local bias control (LBC) scheme is applied using a bias circuit of a pixel source follower (SF) to minimize power consumption. In this study, the effectiveness of the proposed LBC scheme is verified for the MCP readout structure. Through simple modification of a column-biasing circuit, the prototype MCP readout CIS achieved significant power savings, which shows its applicability to low-power CIS applications. The prototype CIS was implemented using a 1P6M 0.18-μm CMOS process. A maximum frame rate of 430 fps was achieved while consuming 2.38 mW of power. Compared to a conventional column driver, the proposed LBC scheme reduces the total power consumption by 29.4%, which is an overall power savings of 15%. The prototype CIS also demonstrated figures of merit of 119.1 $\mu V \cdot nJ$ and 8 $\mu V_{rms}/kHz$.

INDEX TERMS CMOS image sensor (CIS), pixel source follower, column driver, bias voltage control technique, local bias control (LBC) scheme, multiple-column-parallel (MCP) readout.

I. INTRODUCTION

Recently, CMOS image sensors (CISs) have been used in various portable electronic devices, such as mobile phones and PCs, as well as in healthcare applications [1]–[3]. Because the mobilities of such devices are limited by their battery lives [4], minimizing their power consumption is an important design concern for CIS applications.

Various studies have been reported on low-power circuit design [5]–[7] in literature for specific operating conditions. In addition, low-power readout techniques that are optimized for the characteristics of input signals [8]–[10] and specific operations related to applications [11]–[14] have been reported. For example, Park *et al.* [7] achieved low power consumption by adopting a fully dynamic CIS structure; however, this structure is not suitable for high-speed operation because it suffers from high readout noise due to increased global supply signal and power-line fluctuations. Liu *et al.* [10] used pixel signal similarity to implement a low-power readout scheme by reusing the conversion results of previous pixels; however, this scheme is difficult to apply to a readout structure that shares a global reference for analog-to-digital (A/D) conversion. Kim *et al.* [13] proposed a multiresolution CIS adopting the subsampling method to optimize power consumption depending on the imaging conditions; however, the sizes of logic circuits for multiresolution imaging increase with pixel resolution reduction ratios. Because the CIS is a system composed of several functional blocks, while focusing on itself, further performance improvement can be derived by examining the structural role of each block and its power consumption pattern.

There are two different pixel readout mechanisms in CISs for extracting signals: global shutter [15] and rolling shutter readout [16]. Compared to global shutter, the rolling shutter readout is relatively less complex and more cost-efficient. Moreover, the limited numbers of transistors in the pixels allow integration at higher resolutions with less electronic

noise. In general, for the rolling shutter readout, a readout circuitry is used in each column, which is called a column-parallel (CP) readout structure; it sequentially extracts the pixel signals in each row of the pixel array.

However, with increasing customer demand for higher-pixel-resolution CISs, the pixel sizes have reduced to increase the pixel spatial density, thus making it difficult to integrate the column circuitry within a narrow pixel pitch. Note that the column circuitry in the CP readout structure should be laid within a specified pixel pitch. To alleviate this problem, multiple-column-parallel (MCP) readout structures, in which one readout circuitry covers several columns, have been reported [17]–[19]. Although the MCP readout structure has a spatial advantage in layout design, it consumes more power than the CP readout structure for maintaining the required frame rate and noise performance. This is because the MCP readout analog-to-digital converters (ADCs) should operate faster for the number of columns in the MCP unit than the CP structure of ADCs. Considering that pixel sizes continue to shrink (up to 0.64 μm, as recently reported by SAMSUNG [20]), the MCP readout structure is expected to become increasingly popular [21], [22]. Thus, the effort to find an optimal operation method suitable for its structural features will be worthwhile, resulting in further performance improvement. In this study, we examined the potential to further reduce power consumption by modifying the readout scheme using MCP readout structural properties. The operating period that can minimize the current consumption of the CIS was determined by closely examining the structural conditions and operation timing of the MCP readout structure. In contrast with the CP readout structure, where a row is selected for pixel signal readout, the MCP readout structure sequentially reads multiple columns in the MCP unit. In other words, the columns of each MCP unit have their own operating periods before and after A/D conversion. This study focuses on the operating states of each column in the MCP unit. Immediately after completion of A/D conversion in each column, the bias voltage of the pixel source follower (pixel SF) changes to minimize power consumption (hereafter referred to as the local bias control or LBC scheme). This study demonstrates the effectiveness of the LBC scheme in the low-power MCP readout structure with a conventional 10-bit successive approximate register (SAR) ADC.

The remainder of this paper is organized as follows. Section II discusses the low-power MCP readout structure with the pixel bias control scheme. Section III presents an analysis of the power savings effect of the proposed LBC scheme. Section IV describes a prototype CIS and its detailed circuit implementation. Section V presents the experimental results for the prototype chip, and Section VI presents the conclusions of this study.

II. LOW-POWER MCP READOUT STRUCTURE

Fig. 1 illustrates a simplified block diagram of the conventional CIS, which is composed of a pixel array, a vertical scanner (V-scanner), global circuits, and column drivers. To perform A/D conversion on pixel signals, the ramp generator provides global A/D references to the readout circuitry. Here, depending on the ADC type, A/D references can be supplied in the form of the CP or MCP readout structures. The A/D conversion results are then sequentially extracted through the horizontal scanner (H-scanner) from the CIS chip.

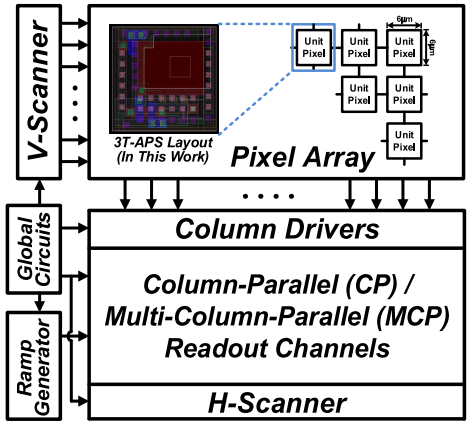

FIGURE 1. Simplified block diagram of a conventional CIS.

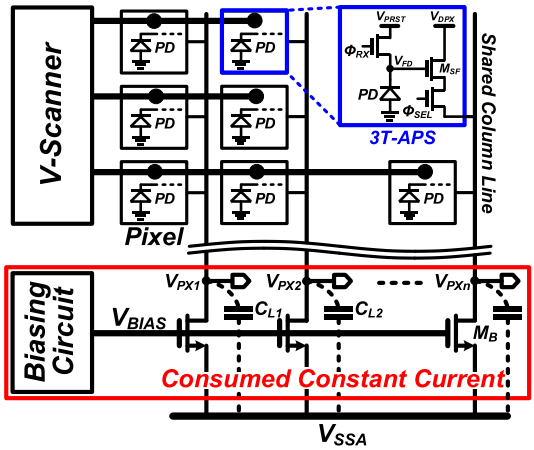

FIGURE 2. Simplified schematic of the column drivers with a pixel array.

Fig. 2 shows a simplified schematic of the column drivers with the pixel array and V-scanner. The pixels in the row are selected by the V-scanner with the control signal of $\emptyset_{SEL}$, and the M_{SF} in the pixel and M_B of the column driver are configured as the pixel SF. Typical current mirror circuits are used to define the bias current of the entire pixel SF. In general, while buffering accumulated electrons of the photodiode (PD) as voltage signals (V_{PX}) in the pixel, the pixel SF constantly consumes power during the entire CIS operation. Therefore, it is one of the main power-consuming blocks in the CIS. Hence, for low-power design, it is necessary to set an appropriate bias current of the pixel SF (I_{BPX}). With a fixed pixel supply voltage (V_{DDPX}), I_{BPX} is related to the bandwidth (BW_{SF}) and output swing range of the pixel SF (ΔV_{PX}). Given that V_{PX} changes continuously according to the pixel control signal, the pixel readout speed could be

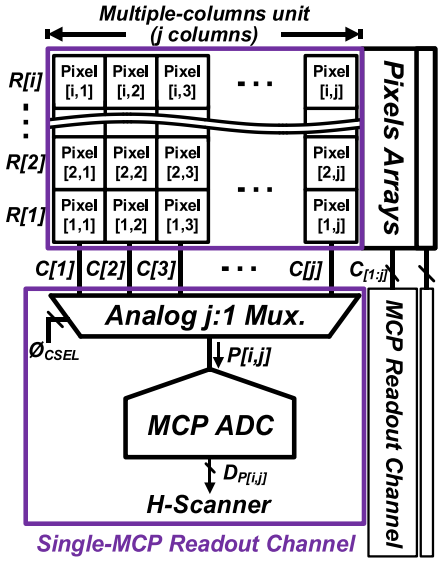

FIGURE 3. Simplified block diagram of the MCP readout structure.

limited by the transconductance of the pixel SF (G_{M_PX}) and load capacitors (C_L) as

$$BW_{SF} \propto \frac{G_{M\_PX}}{C_L}. \tag{1}$$

Because the pixel size is limited, G_{M_PX} depends on I_{BPX}. However, V_{PX} also changes according to I_{BPX} as follows:

$$V_{PX} = A_{SF} \cdot V_{FD} - \left(V_T + \sqrt{\frac{2I_{BPX}}{\beta}}\right) \tag{2}$$

where A_{SF} is the pixel SF gain and V_{FD} is the voltage of the floating diffusion node. In terms of body effect, A_{SF} can be expressed as follows:

$$A_{SF} = \frac{G_{M\_PX}}{G_{M\_PX} + G_{MB\_PX}} \tag{3}$$

$$= \frac{1}{1 + G_{MB\_PX}/G_{M\_PX}} \tag{4}$$

$$\frac{G_{MB\_PX}}{G_{M\_PX}} = \frac{\gamma}{2\sqrt{|2\emptyset_F + (V_{PX} - V_B)|}}. \tag{5}$$

where G_{MB_PX} is the transconductance of the pixel SF with body effect, $\emptyset_F$ is the work function, γ is the body effect coefficient, and V_B is the substrate voltage. According to (2) and (3), V_{PX} decreases as I_{BPX} increases, which in turn decreases A_{SF}. Owing to such performance trade-off relationships, in the CP readout structure, changing I_{BPX} to reduce power consumption during CIS operation could cause severe image quality degradation. In terms of reducing V_{DDPX}, with the scaling-down of CMOS technology, the maximum ΔV_{PX} is limited to secure the operating condition of the pixel SF.Fig. 3 shows the simplified block diagram of the MCP readout structure [8], [16]. In a selected row (R[i]), the input pixel signals (P[i, j]) from columns C[1] to C[j] are inserted sequentially to each MCP readout ADC through the analog

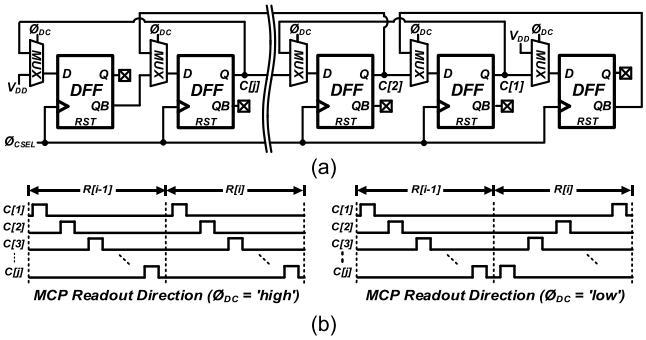

FIGURE 4. (a) Simplified schematic of the analog MUX controller and (b) column readout direction with $\emptyset_{DC}$.

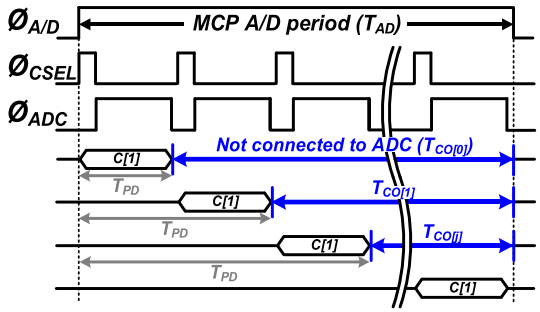

FIGURE 5. Simplified operational timing diagram during the MCP A/D period.

multiplexer (MUX) in the MCP unit. Here, i represents the i-th row, and j represents the j-th column. The simplified schematic of the controller of the analog MUX is shown in Fig. 4(a). It is based on a conventional shift register with additional MUXs to change the logical shifting direction, depending on the control signal of $\emptyset_{DC}$. With the direction control signal $\emptyset_{DC}$, two column selecting sequences to readout in the MCP unit are shown in Fig. 4(b). Because all control logic signals are synchronized and globally fed into all MCP readout channels, there is no performance degradation caused by their operation.

Fig. 5 illustrates the simplified operational timing diagram during the MCP A/D period (T_{AD}). In the MCP unit, each column is selected sequentially along with the control signal $\emptyset_{CSEL}$, and the MCP readout ADCs convert V_{PX} of their corresponding columns during the period of $\emptyset_{ADC}$. Considering the sequential readout operation in the MCP unit, there is an inherent waiting period (T_{CO}) after completion of A/D conversion in each column. Because each column does not perform any function during the T_{CO} period, the performance could be improved for various aspects with additional circuits optimized for utilizing T_{CO}.

III. PROPOSED READOUT SCHEME

Fig. 6 shows the bias current source for the pixel SF in each column, which is a typical cascode structure (M_{CC} and M_B) for improving A_{SF}. As an operational option, ΔV_{PX} can be maximized by changing the biasing voltage of M_{CC} from

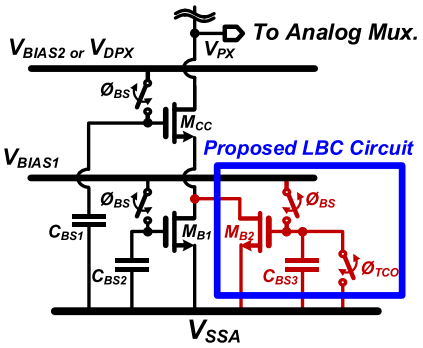

FIGURE 6. Simplified schematic of the bias current source for the pixel SF in each column.

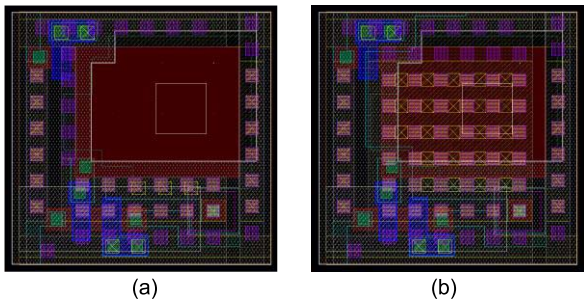

FIGURE 7. Layout design of the (a) 3T active pixel sensor and (b) optical black pixel.

V_{BIAS2} to V_{DDPX}. When the pixel signal decreases according to its own light intensity, it causes fluctuations through the globally shared biasing lines V_{BIAS1} and V_{rBIAS2} in the adjacent columns (i.e., coupling noise). Thus, the column bias sampling (CBS) technique [23], [24] is adopted to alleviate the effects of coupling noise. In this study, the LBC scheme is proposed to minimize the power consumption of each column during the T_{CO} period while reducing the bias currents of the pixel SFs. Compared to the conventional case, the bias transistor of M_B is composed of two transistors M_{B1} and M_{B2}; before the MCP A/D conversion, the own bias voltages are sampled in additional sampling capacitors C_{BS1} and C_{BS2}, respectively. Next, during T_{CO}, the sampled bias voltage of C_{BS2} is reset to the circuit ground voltage V_{SSA} through an additional switch of $Ø_{TCO}$, which turns off M_{B2}. Under this bias condition, since the pixel SF is driven only by M_{B1}, its current consumption is reduced by the ratio $M_{B2}/(M_{B1} + M_{B2})$ (i.e., reduction ratio of I_{BPX}). The reduction ratio of I_{BPX} was designed to be 50%. Moreover, the LBC scheme is more efficient than fully turning on and off the bias current sources of the pixel SFs for reducing the settling time for continuous row readout and coupling noise. $Ø_{TCO[j]}$ and $Ø_{CSEL[j+1]}$ are synchronized and applied sequentially in each column. The last column in the MCP unit is reserved for driving the pixel signal of successive rows, which minimizes the settling errors. In addition, MOS capacitors are used as C_{BS}s for the CBS technique to increase design precision. They are placed near the bias transistors of the comparator for area efficiency. The power savings effect (PSE) of the proposed LBC scheme can be verified with the averaged bias current consumption (I_{BPX_AVG}) of the pixel SFs. Referring to Fig. 4, the total MCP A/D conversion time, T_{AD}, is composed of two operating periods: T_{PD} (driving V_{PX}) and T_{CO} (applying the LBC scheme). Therefore, I_{BPX_AVG} during $T_{A/D}$ can be expressed as follows:

$$I_{BPX\_AVG} \approx \sum \frac{(T_{PD} \cdot I_{PD}) + (T_{CO} \cdot I_{CO})}{T_{AD}} \tag{6}$$

where I_{PD} and I_{CO} represent the bias currents of the pixel SF during T_{PD} and T_{CO}, respectively. As all columns in the MCP unit are selected sequentially, that is, $T_{PD} = T_{AD} - T_{CO}$, (6) can be written as follows:

$$I_{BPX\_AVG} = \frac{1}{T_{AD}}\left(\sum_{n=1}^{j}\left(\left(T_{AD} - \frac{T_{AD}}{j}(j-n)\right) \cdot I_{PD} + \left(\frac{T_{AD}}{j}(j-n) \cdot I_{CO}\right)\right)\right) \tag{7}$$

$$= \sum_{n=1}^{j}\left(\left(I_{PD} - \frac{(j-n)}{j} \cdot (I_{PD} - I_{co})\right)\right) \tag{8}$$

$$= \sum_{n=1}^{j} I_{PD} - \sum_{n=1}^{j}\left(\frac{j-n}{j}\right) \cdot \Delta I_{LBC} \tag{9}$$

where j and n represent the total number of columns and corresponding column number in the MCP unit, respectively. Equation (9) implies that the power savings from the LBC scheme is related to the difference (ΔI_{LBC}) between I_{PD} and I_{CO} and the duration of T_{CO} for each column. Moreover, since the LBC scheme is applied only to T_{AD} of the entire row readout (T_{ROW}), its *PSE* (%) can be defined in terms of the total power consumption as follows:

$$PSE(\%) = \sum_{n=1}^{j}\left(\frac{j-n}{j}\right) \cdot \frac{\Delta I_{LBC}}{I_{PD}} \cdot \frac{T_{AD}}{T_{ROW}} \cdot 100. \tag{10}$$

Considering that the proportion of $T_{A/D}$ increases as the ADC resolution increases, the proposed LBC scheme can be used more effectively for high-resolution ADCs in the MCP readout structure, as observed from (10). In particular, its efficiency would be greater in a low-power CIS, where the power consumption of the pixel SF is comparatively higher.

IV. CIRCUIT IMPLEMENTATION

Fig. 7 shows the layout design of the 3T active pixel sensor (APS) used in this work. It is based on the typical 3T-APS structure using PN junction diodes [25], as shown in Fig. 7(a). To alleviate pixel fixed-pattern noise (FPN), optical black pixels (OBPs) [24] are designed and placed on each side of the pixel array, as shown in Fig. 7(b). The output range of the 3T-APS is approximately from 1.4 V to 0.5 V ($\Delta V_{PX} = 0.9$ V). When applying the biasing voltage V_{DDPX} to M_{CC}, ΔV_{PX} is maximized to approximately 1.2 V with a bias current of approximately 3 μA. From this

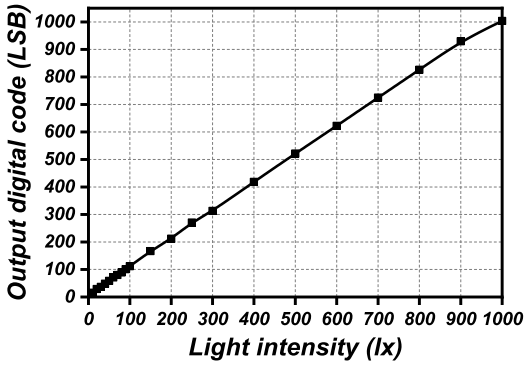

FIGURE 8. Optoelectrical response to light intensity.

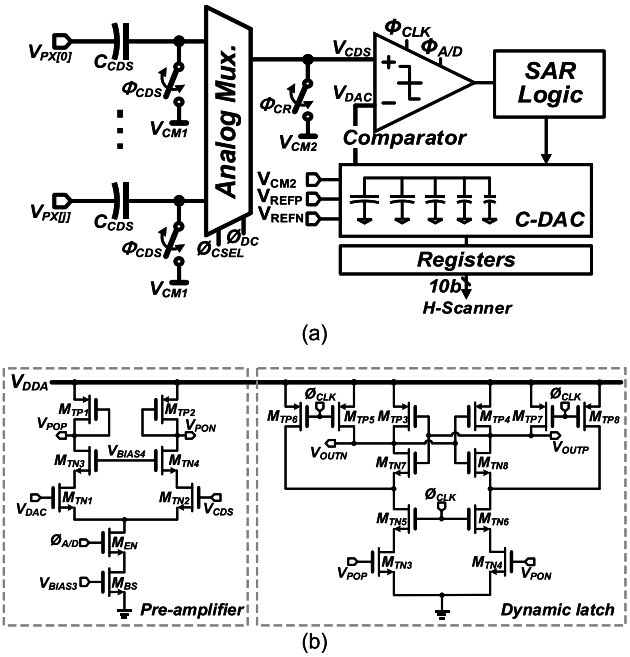

FIGURE 9. (a) Simplified schematic of the 10-bit SAR ADC in the MCP unit and (b) its comparator.

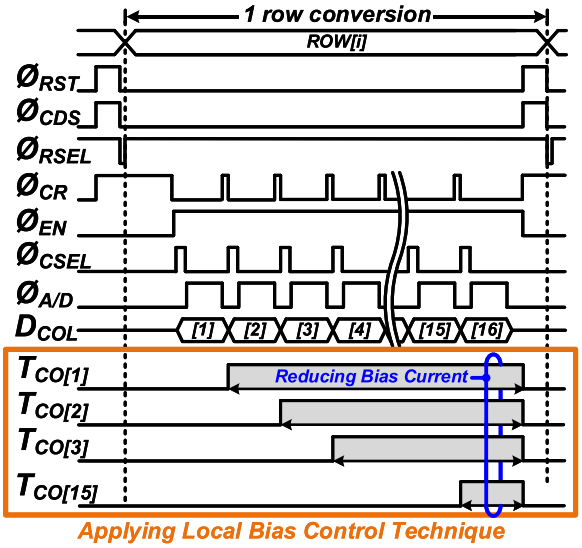

FIGURE 10. Operational timing diagram of the prototype MCS readout CIS with the proposed LBC scheme.

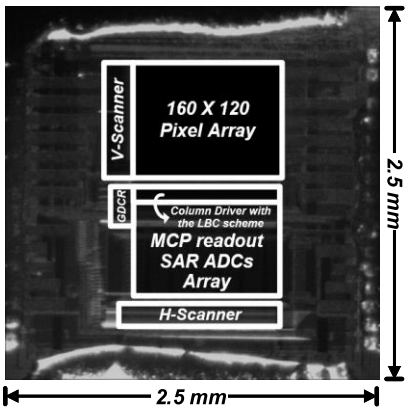

FIGURE 11. Microphotograph of the prototype chip.

result, 1-LSB corresponds to approximately 880 μV at a resolution of 10 bits. Fig. 8 shows the optoelectric response to light intensity while operating at 60 fps. A sensitivity of 54 mV/lx·s was obtained from the slope of the output signal in the prototype CIS.

Fig. 9(a) shows the simplified schematic of the conventional 10-bit SAR ADC in the MCP unit [8]. The capacitive digital-to-analog converter (C-DAC) is binary weighted with a trilevel switching scheme [27], and its total capacitance is 3.58 pF. The comparator of the SAR ADC was designed with a typical two-stage topology of a preamplifier and dynamic latch comparator, as shown in Fig. 9(b). The preamplifier leads to high power consumption because of the constant bias current of 2.35 μA. To reduce current dissipation, the preamplifier is turned on only during T_{AD} with the enabling switch M_{EN} ($\emptyset_{A/D}$).

Fig. 10 illustrates the operational timing diagram of the prototype MCS readout CIS with the proposed LBC scheme. Referring to Fig. 9(a), when the pixel is reset with the control signal of $\emptyset_{RST}$, analog correlated double sampling (CDS) is conducted in C_{CDS} with the control signal of $\emptyset_{CDS}$. Next, all columns in each MCP unit are sequentially selected through the analog MUXs by the control signal of $\emptyset_{CSEL}$, and A/D conversion is performed during the period of $\emptyset_{A/D}$. Before A/D conversion of each column, the comparator inputs of V_{CDS} and V_{DAC} are reset to V_{CM2} with the control signal of $\emptyset_{CR}$. The proposed LBC scheme is applied at the end of each column readout sequentially (T_{CO}), thus minimizing power consumption. Note that the proposed scheme is not applied to the last column to drive the successive row effectively.

V. MEASUREMENT RESULTS AND DISCUSSION

The prototype CIS was fabricated using 0.18-μm 1-poly 6-metal (1P6M) CMOS technology. Fig. 11 shows a microphotograph of the prototype chip. The chip size is 2.5 mm × 2.5 mm, and an effective pixel array of 160 × 120 was implemented with 6 μm pitch of the 3T-APS. Then,

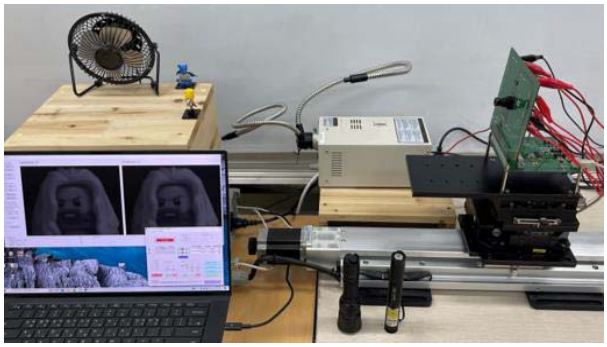

FIGURE 12. Measurement environment for the prototype CIS.

FIGURE 13. Sample image acquired by the prototype CIS.

five additional OBPs were placed on each side of the pixel array. In this design, ten MCP readout units with one 10-bit SAR ADC, which cover 16 columns, are implemented. Fig. 12 shows the measurement environment to verify the performance of the prototype CIS. Various control signals are generated by the external field-programmable gate array (FPGA) board to the chip board. The output codes of the chip board are transmitted to a PC through the USB interface and is displayed using an imaging software program in real time. The sample image acquired by the prototype CIS is shown in Fig. 13. The prototype CIS demonstrates 430 fps, corresponding to a pixel rate of 8.23 Mp/s. The readout time for a single row is approximately 19.4 μs, with 3 μs for the analog CDS operation and 16.4 μs for the MCP readout operation. With the OBP information, FPN from the MCP readout structure was removed via off-chip digital calibration [29].

To confirm the noise influence of the proposed LBC scheme, the histogram of random noise (RN) is shown in Fig. 14 as an image quality indicator [30]. Under dark illumination conditions as in [14], the sample images of 100 frames were captured to obtain the standard deviation of the RN. Compared to the conventional case, when the proposed LBC scheme was applied, the RN increased slightly from 0.47 to 0.55 LSB_{rms} at 620 fps. Moreover, by lowering the operating speed from 620 to 430 fps, the RN was further alleviated by 0.47 LSB_{rms}. Here, we changed T_{AD} from 16.4 to 11.4 μs (thus reducing MCP readout speed by 30%). This result implies that the RN increased owing to the column drivers when adopting the LBC scheme without adequate settling time. Hence, power savings would limit the maximum operating speed, which is a disadvantage of the

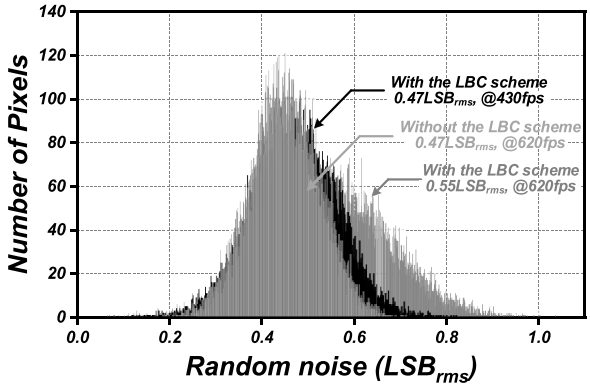

FIGURE 14. Histogram of random noise as image quality indicator.

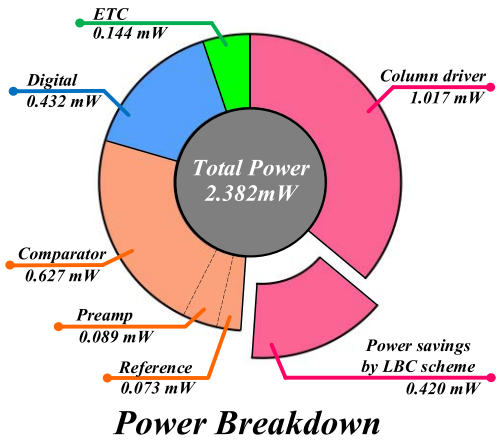

FIGURE 15. Power breakdown of the prototype CIS.

LBC scheme. Note that in the CBS technique, column fixed-pattern noise (CFPN) can be caused by switching noise but is mitigated by the CDS operation. Considering the various CIS applications, it is useful as a low-power technique in applications that do not require high-speed operation.

Fig. 15 shows the power breakdown of the prototype CIS. In this work, because the low-power-consuming SAR ADC is used for MCP readout, the column driver is the block that consumes the most power. Before applying the proposed LBC scheme, the column driver consumes 1.44 mW, corresponding to 51% of the total power consumption of 2.81 mW. With the proposed LBC scheme, the power consumption of the column driver is 1.02 mW, which is reduced by 29.4%. This results in a total power consumption of 2.38 mW, with an overall power savings of 15%.

As the pixel resolution of the CIS increases, the number of columns increases. Since the proposed LBC scheme reduces the power consumption of the column driver, the power reduction effect increases proportionally as the number of columns increases. In addition, since the number of rows increases as the pixel resolution increases, the column driver consumes more power to satisfy a given frame rate. This means that when the proposed LBC scheme is applied in high-resolution CISs, the PSE would be greater because the power consumed by the pixel SF is comparatively higher.

TABLE 1. Performance summary.

Parameter	Value
Technology	0.18 μm CMOS Process
Chip area	2.5 × 2.5 mm
Supply voltages	3 V (Pixel), 1.8 V (Circuit)
Number of pixels	160 (H) × 120 (V)
Pixel size	6 μm × 6 μm
Random noise	0.47 LSB_{rms}
ADC resolution	10 bits
ADC input range	0.9 V
Dynamic range	57.4 dB
Power consumption	2.81 mW (w/o PBC) 2.38 mW (w/ PBC)
Frame rate (fps)	430
FoM (μV·nJ)	119.1

TABLE 2. Performance comparison.

	[9]	[31]	[32]	This work
Process technology	0.35 μm CMOS	0.13 μm CMOS	0.18 μm CMOS	0.18 μm CMOS
Photodiode	PN	PN	PN	PN
Pixel pitch (μm)	3.5	11.2	4.4	4.4
Transistors per pixel	3	3	3	3
Pixel resolution	384 x 256	644 x 488	256 x 128	160 x 120
ADC type	SAR	SAR	SAR	SAR
ADC resolution (bits)	10	14	12	10
Random noise (μV_{rms})	2770	83	96.5	413
Frame rate (fps)	381	120	90	430
Power (mW)	*11.65	78	4.4	2.38
**FoM_1 [μV_{rms}·nJ]	861	171	145	119.1
***FoM_2 [μV_{rms}/kHz]	28.4	1.42	8.38	8.0

*Power consumption is calculated by 1-column power consumption x 256 columns
**FoM_1 = [Noise] x [Power consumption] / [The number of pixels] / [Frame rate]
***FoM_2 = [Noise] / [The number of vertical pixels] / [Frame rate]

Referring to (10), when the proportion of $T_{A/D}$ increases as the ADC resolution increases, the proposed LBC scheme can be used more effectively for high-resolution ADCs. Considering these, although the proposed LBC scheme was verified in this study for the prototype CIS with low pixel resolution, it is worth noting that the PSE of the LBC scheme is expected to increase further when applied for high pixel resolution in high-resolution ADCs.

The measured performance of the prototype CIS is summarized in Table 1. We note that as one of the layout concerns in this design, the input line of the test ADC was routed to the output pad across the global digital control logic (GDCR) without any shielding. Thus, it is difficult to evaluate the static performance, such as differential nonlinearity (DNL), integral nonlinearity (INL), and ADC readout circuit noise, of the SAR ADC alone. This layout problem is expected to be effectively solved by modifying the layout pattern and further adding a layout shielding pattern. Nevertheless, based on the primary characteristics, the proposed scheme is suitable for implementing a low-power MCP readout structure. Table 2 shows the performance comparison of the proposed scheme with other works [9], [31], [32]. The figures of merit (FoMs) in terms of power efficiency and noise performance [33] are calculated as

$$FoM_1 = \frac{Noise \times Power\ consumption}{Number\ of\ pixels \times frame\ rate} \tag{11}$$

$$FoM_2 = \frac{Noise}{Number\ of\ \text{vertical}\ pixels \times frame\ rate}. \tag{12}$$

Although this work has a small-resolution pixel array format, the two FoMs reflect the performance changes as the pixel rate increases. For the two FoMs, the prototype CIS demonstrates better performance for FoM_1 (119.1 μV_{rms}· nJ) compared to other works. For FoM_2, considering that the pixel pitch size of the proposed image sensor is similar to that of a commercial image sensor, the results of this work are comparable from the commercial perspective. This study demonstrates the effectiveness of the LBC scheme in the MCP readout structure. Although the MCP readout ADCs are disadvantageous in terms of their power consumption compared to the CP readout ADCs, the proposed LBC scheme can be used via structural connection to the MCP readout ADC operation. In addition, the proposed LBC scheme is well suited to the column driver based on its MCP structural feature. However, the proposed scheme may also be applied to CP structures that are based on single-slope or two-step single-slope ADCs because these structures can change the bias currents of the comparators upon completion of A/D conversion.

VI. CONCLUSION

This study introduced a low-power MCP readout CIS based on structural features. When performing A/D conversion for each column sequentially, the proposed LBC scheme changes the bias voltage of the pixel SF to minimize power consumption. Based on the power savings analysis of the proposed LBC scheme proposed herein, we estimated that a PSE equivalent to approximately 16% of the total power can be achieved. In the actual measurements, the PSE of 29.4% for the column drivers was demonstrated with the prototype CIS, which corresponds to an overall power savings of 15% in the CIS. The predicted and measured PSEs of the proposed scheme show similar results, which proves that the LBC scheme reduces the power consumed by the column driver effectively. As the pixel sizes in CISs continue to diminish, the MCP readout structure with the proposed scheme can be used for low-power CIS applications.

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