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A Novel Multi-Scale Method for Thermo-Mechanical Simulation of Power Integrated Circuits

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ABSTRACT During development of power Integrated Circuits (IC), several iterations between the design and test/ measurement steps are performed. Computer-aided engineering significantly shortens the product development process because the numerical simulations can identify and remediate most deficiencies during the design stage. The recent IC manufacturing technologies lead to ca. 10^4-order scale separation between transistor cell details and the device active area, resulting in very complex IC models. For the IC complexity to be overcome, advanced multi-scale analysis methods are required to perform accurate simulations in a decent time (order of hours). This paper proposes an advanced and enhanced multi-scale simulation method for the thermo-mechanical analysis of power ICs. The computational IC structure is automatically generated from a Cadence layout and partitioned into far-field and homogenized regions - the macro-model. Detailed localized micro-scale sub-models are assigned to limited portions of the homogenized region. The two-way simulated data transfer between the homogenized macro-model and the micro sub-models is one multi-scale approach novelty proposed in this paper. The method is validated on a real test chip structure presented in literature. The proposed multi-scale approach in conjunction with the two-way macro-micro data transfer lead to similar accuracy in the prediction of defect location, yet with significant simulation time - and computational resource reduction (CPU time and RAM usage reduced by almost 80% and 60% respectively) compared to the method used as reference.

INDEX TERMS Reliability simulation, DMOS structure, multi-level simulation method, sub modeling, fast thermal cycling, power cycling.

I. INTRODUCTION

Power ICs are used in a wide range of applications, e.g., in the automotive industry, to control different electrical loads [1].

Regardless of the manufacturing technology, whether it is bipolar, Double-diffused Metal-Oxide Semiconductor (DMOS) or high integration Bipolar-CMOS-DMOS (BCD), the power ICs metallization is subjected to Fast Thermal Cycling (FTC) [2]. During switching, the power dissipated by the device generates high junction temperatures in short time intervals, causing the plastic deformation of the metallization layers. Thermal Induced Plastic Metal Deformation (TIPMD) accumulates in metallization leading to device failure after a number of switching cycles ranging between 10^4 and 10^9 [3]. Some of the most frequent failure mechanisms caused by FTC are the cracking of metal lines [4], the delamination of power metal from the SiO_2 substrate [5] and the cracking of dielectric between two adjacent metal lines, widely known as Inter-Metal or Inter-Layer Dielectric (IMD or

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ILD) cracking [6], [7]. The metal extruded inside the cracks causes short-circuits, which in some cases means device critical failure, as demonstrated in [2] and [3].

The complex nature of multi-physical phenomena that take place in power ICs makes reliability prediction difficult to achieve by purely theoretical models, while reliability measurements are very time-consuming and require multiple iterations, increasing the cost of design. Therefore, the reliability analysis of power ICs, based on numerical simulation employed in early design stages, is essential for designing more robust and cost-effective devices. The Finite Element Method (FEM) is the most popular for numerical simulation of IC models, because it allows for the analysis of complex multi-physical phenomena on structures with complex geometries and highly heterogeneous material properties.

Although a power ICs model is built-up of subdomains of simple 3D shapes (often regular hexahedral regions with different material properties), the resulting computational models are very complex [8]. Due to material inhomogeneities and high aspect ratios between the repetitive transistor cells (hundreds of nanometer order [7]) and the entire switching stage (millimeter order [7]), significant computational resources (CPU time and RAM) are required when standard FEM is used to solve such 3D models [9]. In order to increase the efficiency of the simulation process, computational domain simplification and homogenization [10], combined with advanced conforming or non-conforming mesh generation [9] and [11], are applied in the direct FEM analysis. These approaches lead to less "heavy" computational models, at the expense of decreased result accuracy. For example, manual time-consuming model simplifications have been carried out in [12] in order to assess by direct FEM simulations, the chip failure during Active Power Cycling (APC) tests and to correlate the numerical simulation results with the spot of emerging failure.

For efficient numerical analysis (minimized CPU time and RAM requirements) of thermo-mechanical processes in power ICs, multi-scale FEM was recently used [13]–[17]. The main advantage of multi-scale FEM is the progressive reduction of the computational domain towards the presumed failure region. The multi-scale FEM is based on the cut-boundary method, which assumes that displacement results from the macro-scale model are used to constrain the lower-scale models [15]. Although the multi-scale FEM is widely used in the thermo-mechanical analysis of power IC, strong limitations can occur because the simulation results are transferred only in one-way - from the macro to micro-scale sub-models [13]–[17]. Hence, in case of time-dependent problems, such as the local plasticity of the IC metallization system, because the micro sub-models contributions (e.g., in plastic strain and stress) on the macro-model time iteration step are ignored (not being interpolated back on the macro-model at the subsequent iteration step), the prediction of the accumulated plasticity-related phenomena is less conservative. To overcome the one-way method drawbacks, some papers [18]–[21] propose to add a macro-model correction step in order to obtain a full iterative procedure. It was shown that the two-way method efficiently solves the generic structural mechanic problem [18], large assemblies [19], fuels [20], and nuclear reactors in [21]. However, insufficient or no interest whatsoever has so far been given to the implementation of the two-way method in multi-scale modeling of power IC, for assessing the thermo-mechanical local plasticity.

A typical one-way multi-scale numerical thermo-mechanical analysis requires the homogenization of highly heterogenous regions of power IC model. During two stages, the homogenization of heterogenous regions is solved, [22] and [23]. The first stage solves the problem of inclusions (representative volume element – RVE) encapsulated in a very large homogenous domain, similar to the Eshelby problem [24]. In the second stage, the equivalent computed fields are assigned to the homogenized region of the macro-model. Several semi-analytical approaches such as affine [25]–[27], self-consistent [28]–[30] or Mori-Tanaka methods [31]–[33] can be applied to determine the evolution law of homogenized material properties. The affine and the self-consistent methods mainly homogenize thermo-elastic material properties [26] and [29]. One drawback of these methods is the high computational time required by the Laplace-Carson domain transformation. In addition, Mori-Tanaka formulation can homogenize the heterogenous computational domains with thermo-elasto-viscoplastic material properties [27] and [28]. However, the linearization procedure required by this method lacks in comprehensiveness and limits the accuracy. The direct numerical simulation homogenization method [34] is preferable to the above-mentioned methods, because it can compute the equivalent material properties, regardless of the structure inhomogeneity and elasto-viscoplastic material behaviors. The method is based on numerical estimation (e.g., FEM) of homogenized material properties.

In order to accelerate the simulation process, reduce computational resource, avoid any excessive and time-consuming simplification procedures and improve the accuracy of one-way multiscale analysis, a novel multi-scale numerical simulation approach is proposed. A complex (all geometrical details) 3D IC model is generated. The model is composed of far-field and interest regions. The interest region (e.g., power stage) is highly heterogeneous and is replaced by a homogenized region (computed based on direct numerical simulation homogenization method) to obtain a computationally efficient simulation model - macro-model. Localization regions (regions susceptible to important plastic deformations) are pointed out on the macro-model from a preliminary thermo-mechanical simulation during one temperature cycle. Micro sub-models (which capture all geometrical details of power stage components) are defined and linked to the macro-model localization regions. The macro and micro-model are simulated together during the same time loop and simulations results are interpolated from macro to micro and from micro

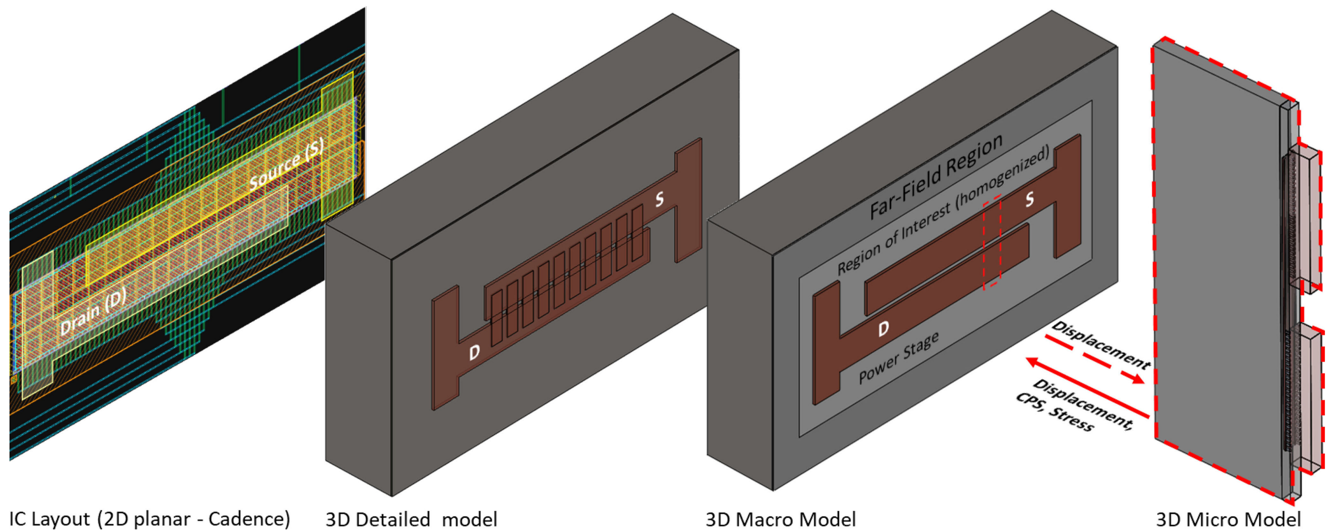

FIGURE 1. Implementation workflow of the two-simulation level multi-scale approach.

to macro. Although a similar simulation procedure can be found in the literature [13]–[17], the advantage of the multi-scale method proposed in this paper is the iterative updating of the macro-scale model with the field values calculated in the micro-scale sub-models. The two-way multi-scale updating solution ensures a correction of the macro-region wherefrom the micro-model for the next time-point simulation is localized. Comparisons are performed between the proposed two-way multi-scale method and the one-way multi-scale method on the same power IC test chip (designed in a BCD technology model) presented in [2] - reference computational model. The results obtained by multi-scale methods are qualitatively compared with those obtained on the reference computational model (not multiscale). The reference computational model in this paper has been built similarly to the model specifications in [2] and recomputed (for benchmarking purposes) using direct FEM method. The failure mechanism predicted with the multiscale analysis developed in this paper is caused by the metal creep that leads to high stresses in the insulator leading to generation of cracks in the encapsulating IMD.

Finally, the computational resources required by the multi-scale approach (two-ways) are compared with those required by the direct FEM method on the reference model.

II. POWER IC SIMULATION BY TWO-WAY MULTI-SCALE COUPLING METHOD

The two-way multi-scale coupling technique has already demonstrated its potential in structural mechanics with local plasticity [18] and material damage analysis [35]. As already mentioned, the method is applied in two stages. In the first stage, equivalent homogenous material properties of a macro model (very simple), related to heterogeneous regions model (very complex) are extracted. This is referred as bottom-up formulation. In the second stage, the unknown variables of microscale models are computed, starting from the known macroscopic variables. This is referred as top-down formulation.

In Fig. 1, the implementation of the two-way coupling multi-scale method is presented. The method starts with the definition of the 3D computational model. The computational model can be automatically generated from the 2D IC layout (e.g., designed in Cadence). The 3D computational model construction procedure is implemented in Python and run in Salome preprocessing software [36]. The computational model consists of planar geometry features extruded along a perpendicular direction, so that a fast 3D detailed model is obtained.

The 3D computational model is divided in far field and interest regions. The far-field region consists of homogenous blocks (Si bulk and SiO_2 layer). The interest regions from the 3D computational model include the highly heterogenous region of power stages (metallization system). The highly heterogenous region is homogenized and equivalent material properties are assigned to the homogenized regions (e.g., signal metallization system). FEM numerical homogenization, as described in [34] and [37] is applied (bottom-up formulation). To the homogenized region, equivalent material properties computed on the RVE are assigned. Thus, a reduced complexity macro-model, suitable for a FEM analysis with moderate computational resources, is obtained.

The micro sub-model will localize the interest region where the failure is most probable to occur on the studied IC structure (Fig. 1). The localization is performed based on the Cumulative Plastic Strain (CPS) results (metal creep) according to [38]. The CPS is computed at the first temperature cycle on the macro-model. Thus, a limited macro-region, wherein the maximum values occur, is pointed out to be linked with the localization micro sub-model. A typical micro sub-model is reduced in size (10^2-10^3 smaller) but consists of all geometrical details encompassed by the localized region of the studied power IC. However, because of its reduced

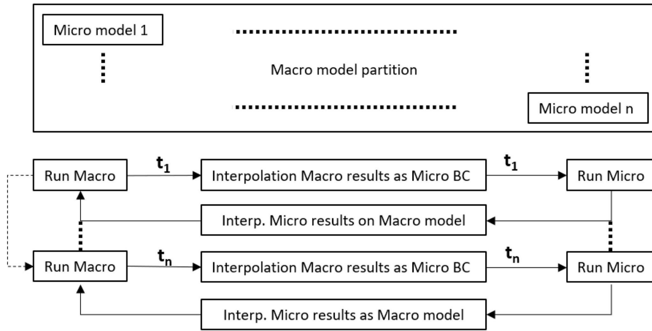

FIGURE 2. Schematic representation of two-scale simulation algorithm.

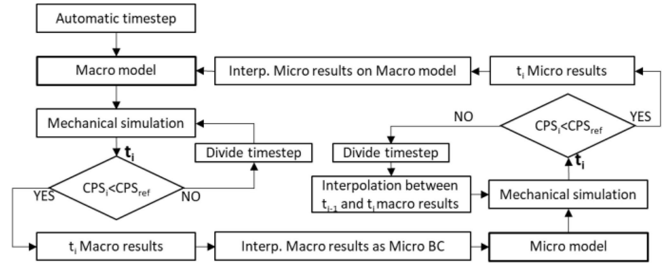

FIGURE 3. Adaptive time-step computation.

dimensions, the micro sub-model requires less CPU time and memory during simulations, compared to the reference complex model.

The thermo-mechanical localization procedure (top-down formulation) considers the large-scale model results as mechanical constrain for the micro-scale sub-model based on the Saint Venant's principle [39], stipulating that at a given moment, a state of forces inside the model can be replaced by an equivalent static system (the state of displacement on the boundary). Hence, the mechanical stress and strain fields inside the localized model are distorted only near the model boundaries. The number of stimulation levels (scales) depends on the complexity of the studied IC structure and the resolution requirements. In this work, the multi-level approach for two simulation scales is defined.

The iterative actualization of macro-scale results is presented in Fig. 2. The user can partition the complete or several regions of macro-model in boxes that define the localized micro-regions (micro sub-models), function of simulated CPS during one temperature cycle. The localized micro sub-models do not necessarily need to completely cover the macro-model. For the initial tests, a single micro sub-model is usually defined.

The macro-scale model is firstly simulated at the t_1 time-step to determine the displacement and stress. Further, the nodal displacement results are interpolated to the computational nodes of micro-model(s) boundary, using the linear interpolation method detailed in [9]. They are used as initial or boundary conditions (BC) in the micro-model. Simulation of each micro-model leads to detailed results (nodal displacement and computed stress at Gauss integration points). The micro-model simulation results are further interpolated back on the macro-model volume mesh elements, thus enriching the macro-model results.

The viscoplastic behavior specific to the metal regions is time-dependent, hence a time integration scheme is required. The time step discretization is a function of the CPS results, see Fig. 3.

An initial time step is set for the mechanical simulation. The simulation advances to the next time step only if the CPS results (the difference between the current time-step plastic strain and the previous one) is under the imposed threshold (CPS_{ref}). If the CPS_{ref} is exceeded, the time step interval $t_{i+1} - t_i$ is divided. The microscale model shall be computed on the same time steps as the macroscale model. When the CPS results exceed the CPS_{ref}, the time step is further divided.

The next time-step of the macro-scale simulation is defined according to an automatic adaptive time step. The next time step is predicted using the following equation:

$$\Delta t_{i+1} = c \cdot \Delta t_i, \ \ where\ c = \min_{i \in N} \frac{CPS_{ref}}{|\Delta CPS_i|}, \tag{1}$$

where t_i is the current time step, CPS_{ref} is the imposed threshold, and the ΔCPS_i represents the CPS field variation at Gauss points between the previous and the actual time step.

III. CASE STUDY ON A PHYSICAL TEST STRUCTURE

A. COMPUTATIONAL MODEL

The geometrical model used in this work is extracted from the layout of a test chip on which FTC measurements were performed; experimental results were presented in [2]. The test chip is a lateral DMOS transistor designed in a BCD technology.

Starting from the device's layout designed in Cadence, the computational model is automatically generated. First, the 2D footprint of each geometrical feature is generated. Further, each footprint is extruded into the 3D feature and translated to the final position according to the device manufacturing technology details. The resulted geometry represents the complex reference computational model, containing most of the geometrical details (such as all signal metal lines in Fig. 4). The metallization system is built from two power metal plates (PMet) and four layers of signal metal lines. The PMet plates are twice as thick as the signal metallization (ratio 2:1 on Z-axis). Along the Z axis, for the computational model, the real thickness of Si die is considered. The device's Active Area (AA) has a rectangular shape (ratio 5 to 1 on the X-axis), of approximately $0.15mm^2$, as described in [2]. The AA is considered in Si die under the signal metallization system, being highlighted with a red dotted rectangle in Fig. 4.

Due to the model symmetry (e.g., distribution of power metal and the signal metallization system), only a quarter of IC test structure is required for the thermo-mechanical numerical analysis, see Fig. 5.

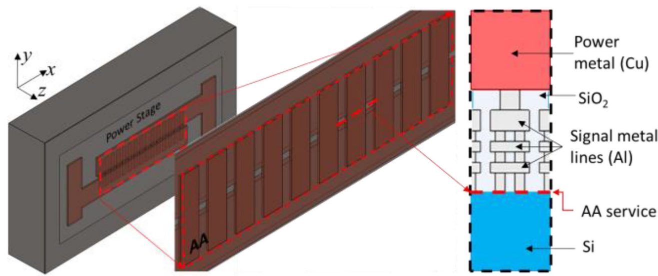

FIGURE 4. 3D computational model with geometrical details of metallization system - (---) Active Area (AA).

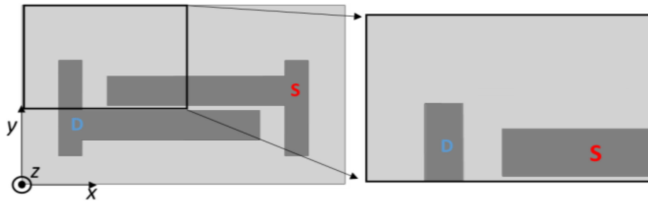

FIGURE 5. Top view of practical simulation model - a quarter of IC test structure.

TABLE 1. Elastic material properties extracted at the reference temperature (293.15 K).

Material Properties	Al	Cu	Si	SiO_2
Young Modulus (GPa)	70.4	140	168	54.5
Poisson ratio	0.33	0.34	0.36	0.2
Shear Modulus (GPa)	26.5	52.23	79.5	22.33
CTE (1/K)	$2.32e^{-5}$	$1.65e^{-5}$	$2.5e^{-6}$	$2.5e^{-7}$

The multilayer routing metallization system made of Al metal stripes is embedded in the dielectric region (e.g., SiO_2) and the power metal plates made of Cu are placed on top of the routing system, Fig. 6 left. The elastic material properties assigned to each different material region of the computational model are presented in Table 1. Temperature-dependent material properties are used for each material, except for SiO_2, which is defined according to [40]–[42].

Time-dependent evolutionary elasto-viscoplastic laws characterize the material properties of metal regions (Al and Cu) according to Chaboche [43]. Thus, plasticity and ratcheting effects are computed during mechanical simulation.

The resulted computational model considers all constitutive features, with specific material properties, of IC test structure. This model is simulated using the direct FEM analysis and is further referred as the reference model.

B. MULTI-SCALE MACRO-MODEL DEFINITION

In power ICs subjected to fast thermal cycling, the accumulated plastic strain in the topmost layer of the signal metallization (see M1 in Fig. 6 left) is found to be far more pronounced than in the lower signal metal layers, which are thinner, [2] and [3]. Consequently, to generate the macro-model, the complex reference model is simplified (see Fig. 6 right). Thereby, the geometrical model will be finally composed only of the signal metal layer (M1) right underneath the PMet, while the other signal layers will be replaced by one homogenized region.

TABLE 2. Equivalent linear elastic material properties extracted at the reference temperature (293.15 K).

Material Properties		
Young Modulus (GPa)	E_x	57.6
	E_y	57.7
	E_z	56.5
Poisson ratio	ν_{xy}	0.24
	ν_{xz}	0.25
	ν_{yz}	0.251
Shear Modulus (GPa)	G_{XY}	23.17
	G_{XZ}	23.17
	G_{YZ}	23.24
CTE (1/K)	α_{xy}	$1.36e^{-5}$
	α_{xz}	$1.04e^{-5}$
	α_{yz}	$1.11e^{-5}$

The extraction of equivalent material properties for the homogenized region starts with the right choice of the RVE, similar to the fiber-reinforced composite material pattern [37]. The RVE should incorporate all the constitutive phases from homogenized region represented by the metal lines, and the matrix represented by the dielectric (equivalent of encapsulating material). The RVE dimensions should be chosen to reproduce the periodicity of the structure. It should be small enough so that any stress and strain state of the macro-structure is constant across RVE, [34]. Since the metallization of such devices exhibits geometrical periodicity, the general practice is to select the smallest domain which comprises all the geometrical details (Fig. 6 center bottom). Further, stress and strain from a static study on the RVE subjected to traction and shear loads are obtained. The stiffness tensor is then calculated based on the computed stress and strain, followed by the homogenized linear-elastic material properties of inverse stiffness tensor, [34].

The homogenization process applied to the RVE, extracted from the studied IC structure includes only Al and SiO_2 materials. The resulted material properties are isotropic due to the alternate direction of metal lines (x and y direction) from one metal layer to another. Table 2 presents the computed equivalent material properties at the reference temperature (293.15K). The equivalent homogenized material properties are computed for a temperature interval ranging from 293K to 600K, with a 30K step, [6].

C. MESH

Meshing studies [9], [44], and [45] demonstrated that elastic and plastic behavior regions require specific mesh elements and densities in order to accurately capture the undergoing processes. An unstructured mesh of linear tetrahedral elements was generated for the domains of elastic material properties (Si or SiO_2). For the domains with nonlinear material properties (i.e., Al or Cu), characterized by nonlinear kinematic hardening Chaboche model, to avoid any blockage (e.g., generated by the linear tetrahedral mesh

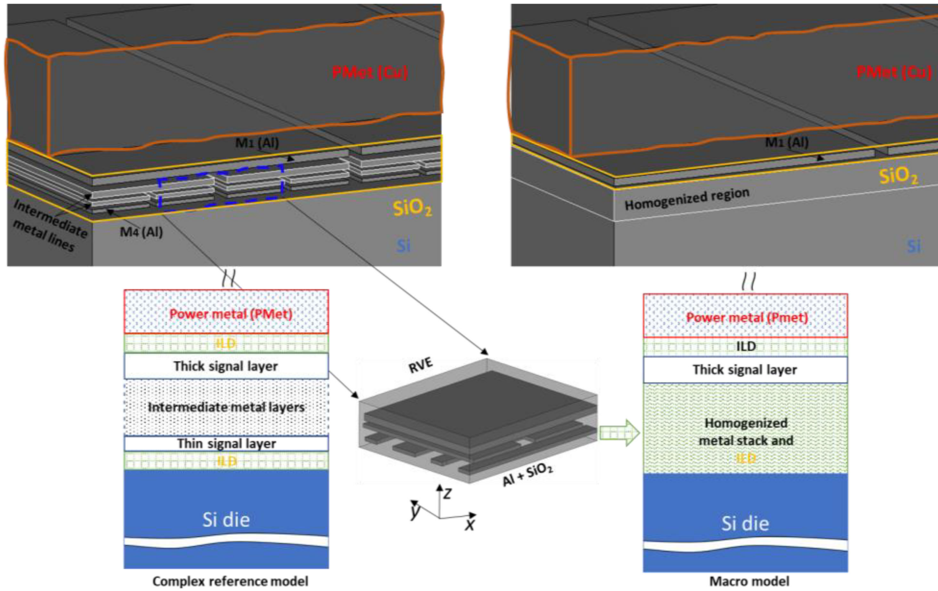

FIGURE 6. **Multi-scale macro-model definition.**

elements [44]), a structured mesh of lower-order hexahedral elements was generated. In addition, a high-density mesh is required for the interest region to accurately capture the thermally induced deformations [45]. For example, an adaptive structured hexahedral mesh, varying in size from 0.25 to 0.05 μm, in metallic regions with nonlinear material properties, was generated.

A non-conformal mesh alongside the multi-domain interfaces is used to simplify the meshing procedure, mainly on the macro (simplified model) [9]. The advantage of this method is that the domains of complex topology can be independently meshed and meshing failure is highly minimized. The meshing generation process is parallelized and is faster, compared to conformal meshing methods. The disadvantage consists in higher complexity of the mathematical model that will overcome the nonconformity at the interface between non-matching domains.

The mesh generated on the analyzed computational models finally consists of: $3.98 \cdot 10^6$ nodes and $19.67 \cdot 10^6$ mesh elements - reference complex model; $1.48 \cdot 10^6$ nodes and $7.05 \cdot 10^6$ mesh elements - macro (simplified) model; $0.41 \cdot 10^6$ nodes and $2.16 \cdot 10^6$ elements - micro (detailed) sub-model.

D. BOUNDARY CONDITIONS - THERMAL LOADS

The temperature distribution is computed on the reference model starting from a uniform power distribution on AA surface, for reproducing the same behavior of the IC under the test conditions in [2]. The amplitude of the power pulse is 15W with $t_{on} = 3.5$ms and $t_{off} = 46.5$ms (see Fig. 7 a). The pulse has a 50ms period. During t_{off}, the model cools down to the reference temperature of 125°C (398K), as measured during tests in [2]. On the bottom face of the Si die (e.g., at the interface with the Leadframe), a constant temperature $T_{ref} = 125$°C condition is set. The maximum

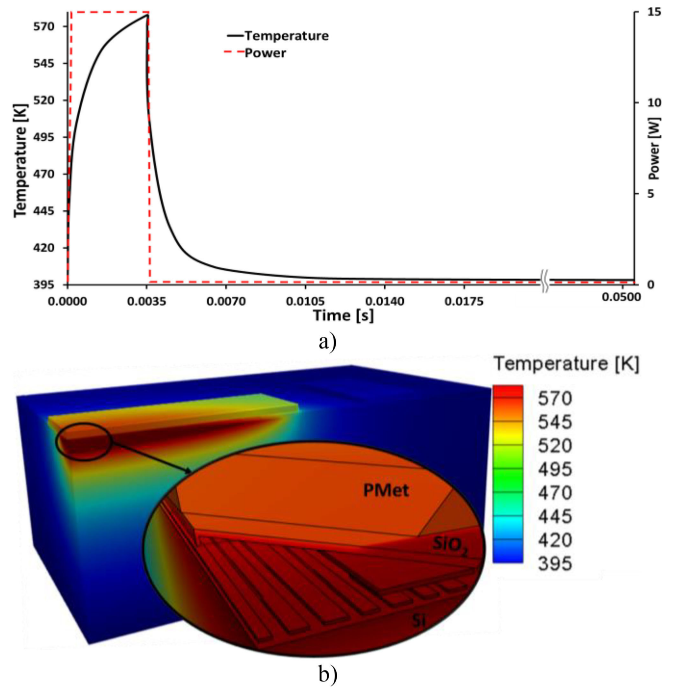

FIGURE 7. **a) Power stimulus pulse and temperature response; b) temperature distribution on the reference computational model at 3.5ms.**

temperature, ca 300°C (580K), is reached at the AA surface at the end of the power pulse. The temperature color plot on the reference computational model is presented in Fig. 7 b. The signal metallization system reaches the maximum temperature (ca. 575K). The PMet plate acts as a thermal capacitance. Because it has larger dimensions compared to signal metal lines, it cools down the SiO_2 below PMet. The simulated temperature profile extracted from AA,

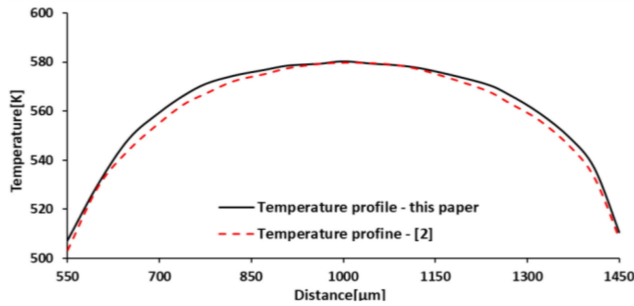

FIGURE 8. Comparison between temperature profile obtained in [2] and the one obtained on the reference model in this paper.

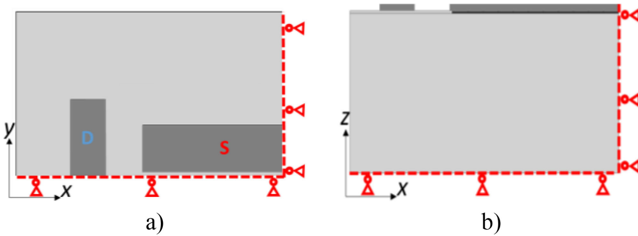

FIGURE 9. Mechanical boundary conditions: a) top view and b) lateral view.

along a line coinciding with x axis in Fig. 5, is similar with the one simulated in [2], see Fig. 8.

The coupling between the thermal and the mechanical problems is one-way only (thermal to mechanical). Thus, each study (reference, macro, and micro) uses the same thermal load.

E. BOUNDARY CONDITIONS - MECHANICAL CONSTRAINTS

Symmetry boundary conditions are imposed on the multi-scale macro-model, see Fig. 9. As the bottom face of the model corresponds to the interface between the die attach and leadframe, the displacement is constrained on the Z-axis.

F. MULTISCALE RESULTS TRANSFER

The mechanical displacement states simulated in the macro-model are transferred at each time point (linear interpolation using the finite element shape functions [9]), on the cut-out boundaries of localized study (micro-model), see Fig. 10.

The cut-out boundary of the localized model could be any shape (e.g., planes, sphere, irregular shapes). The fundamental condition for choosing the shape of the cut-boundaries is given by the geometrical particularities of the detailed model. For example, the localization performed in this study requires planar surfaces for extracting the cut-out micro model due to the longitudinal recurrence of signal metal lines (M1, see Fig. 10).

The next simulation time point starts after the interpolation of micro-model results back on the macro-model. The micro-model displacement results computed at the mesh nodes, and CPS and stress results computed at the Gauss points

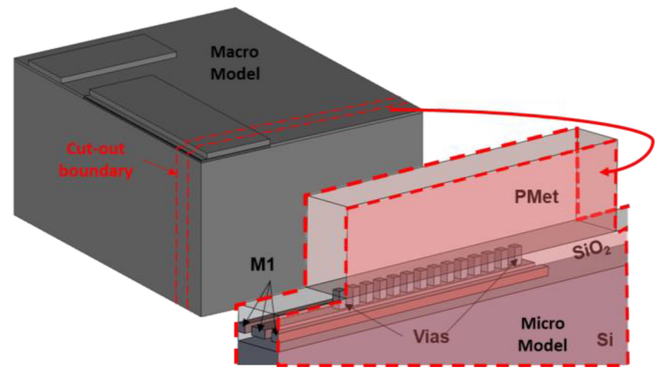

FIGURE 10. Example of micro sub-model extraction for macroscale results interpolation on the cut-out boundary.

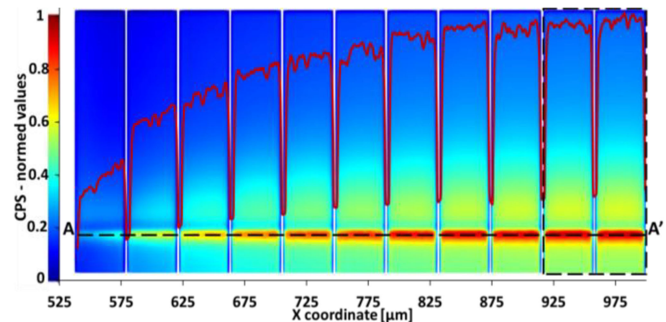

FIGURE 11. Normed CPS distribution at the level of M1 metal layer and extracted CPS values along the AA' line at the end of the first power pulse (3.5ms).

are linearly interpolated back on the macro-model (at the computational nodes and Gauss points respectively).

IV. RESULT DISCUSSIONS

The thermo-mechanical study is scripted and performed in the small deformation domain, in Code_Aster [46], thermo-mechanical FEA open-source software. PETSc solver [47] was used to solve the mechanical problem. The thermo-mechanical study was performed on two processors HP Z620, 128Gb RAM workstation.

A. MACROSCALE STUDY ON 1ST STUDIED CYCLE

To determine the localization region of reliability study, the macroscale model is studied during the first temperature cycle. The CPS variation across the M1 metal lines is analyzed to find the most affected metal line(s) of the studied structure. Fig. 11 shows the normed CPS values at the end of the first power pulse (3.5ms) inside the M1 layer. The AA' line is placed under the edge of the PMet. The color plot is superposed with the extracted values along the AA' line. The largest CPS values are found at the center of device (see two M1 lines, right of Fig. 11). The failure is most likely to appear inside the IMD SiO_2 region and is usually caused by the high aspect ratio between the width of an M1 metal line and the dielectric gap between two adjacent metal lines [2]. The localization must place the cut-out

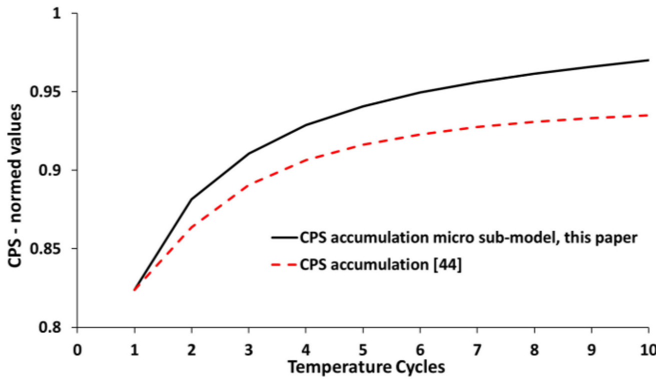

FIGURE 12. Accumulated plastic strain function of temperature cycle along one signal metal line: micro sub-model in this paper and structure studied in [44].

boundary inside the regions with minor stress variations, according to Saint Venant's principle [39], represented by the IMD. Hence, the study will be localized at the first two metal lines, closest to the device center, see the black dotted rectangle in Fig. 11.

B. MULTI-SCALE METHOD ACCURACY ASSESSMENT

It is well-known that APC is a high-cycle fatigue phenomenon that leads to stress-strain redistribution, by relaxation, plastic-shakedown or cyclic plasticity, and that over time it impacts on the final stress-strain distribution. Although, theoretically, several thousand load cycles would be required to correctly capture by numerical simulation the fatigue phenomenon, practically, CPS highly accumulates after the first temperature cycles. Furthermore, the CPS accumulation linearizes and makes easier the prediction of failure zone. A numerical study made over 10 temperature cycles, on the micro sub-model described in this paper, and on the computational structure presented in [44], shows that CPS linearizes after 5 temperature cycles, see Fig. 12. Smorodin *et al.* demonstrated by numerical simulation in [3], the CPS linear accumulation behavior over 2000 temperature cycles. Bari and Hassan investigated by numerical simulations and experiments in [48], the Chaboche model [43], and demonstrated that "*simulations exhibit desired nonlinear ratcheting for lower cycles and constant ratcheting rate for higher cycles*." Therefore, one can assume that the CPS prediction based on 10 power cycles, as shown in this paper, can accurately indicate the critical zone of emerging defect.

The simulation results on the multi-scale model are compared with the reference model results, based on the method described in [2]. The CPS results are averaged along the extraction line (AA') inside the micro-region for both the multi-scale and the reference model.

The relative error between the averaged CPS (simulated with the multi-scale method) and the averaged CPS (simulated with the reference model), is evaluated during several temperature cycles. After ten cycles, both relative errors - between the averaged CPS (simulated with the one-way multi-scale method) and the averaged CPS (simulated with the reference model), as well as between the averaged CPS (simulated with the two-way multi-scale method) and the averaged CPS (simulated with the reference model) - converge to 2.25% and 1.75%, respectively, see Fig. 13.

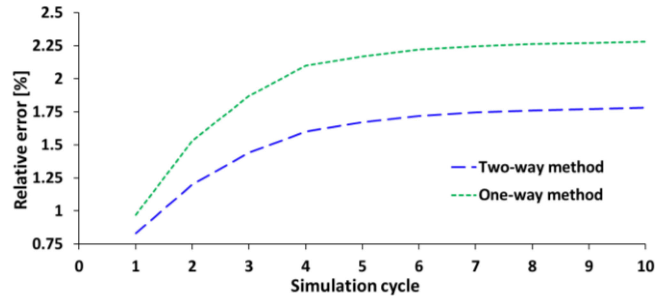

FIGURE 13. Evolution of the averaged CPS relative error between multi-scale methods and reference model during ten cycles.

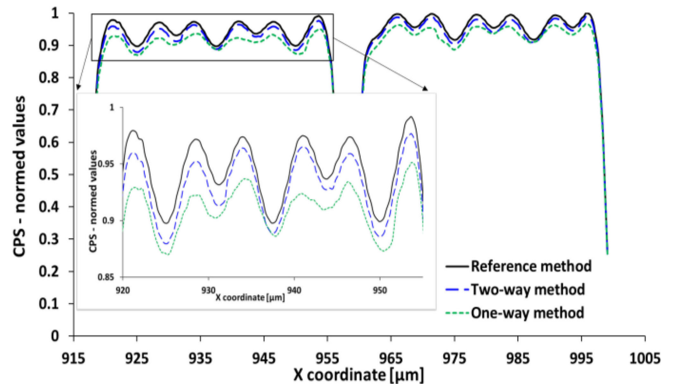

FIGURE 14. Comparison between the CPS normed values computed with the multi-scale methods, and reference model at 10th temperature cycle.

Henceforth, the results simulated after ten cycles will be used to foster a better accuracy of the multi-scale method.

The CPS simulated, on the one hand with the one-way multi-scale method and, on the other hand, with the two-way multi-scale method, are compared with the CPS simulated on the reference model, see Fig. 14. It can be clearly seen that after ten temperature cycles, the latter CPS results get closer to those simulated on the reference model. Hence, the former method can underestimate the CPS results in the critical regions, because it does not update the macro-scale model with the results simulated in the micro sub-model.

The multi-scale model results follow the same behavior as the reference model, but they are slightly influenced (mitigated) by the material homogenizations in the macro-model simulation stage. Fig. 15 presents the normed values of CPS along AA' line during ten temperature cycles.

C. VALIDATION OF THE MULTI-SCALE METHOD WITH MEASUREMENT RESULTS

Calibrations and validations versus detailed geometrical models are useful, but they do not always prove the concept. The multi-scale simulation method needs being further validated by laboratory measurements performed on the test

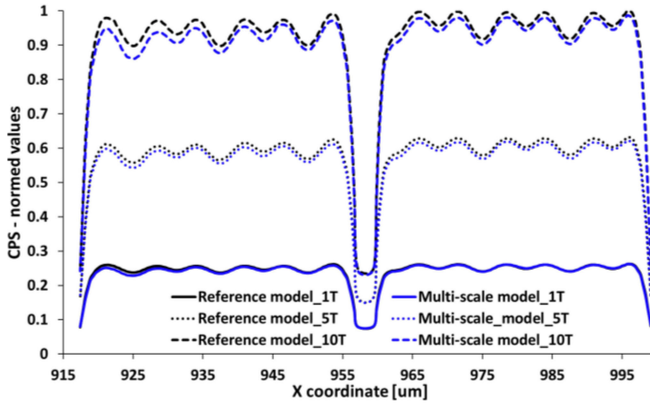

FIGURE 15. Normed values of CPS along AA' line during ten temperature cycles: reference model and multi-scale model.

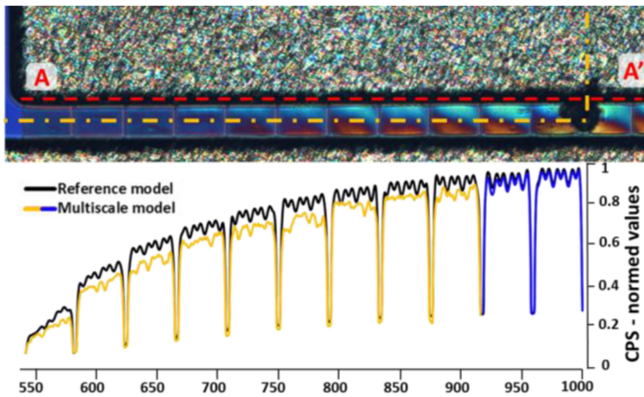

FIGURE 16. Image of differential interference contrast (Nomarski) from a failed device [2] correlated with CPS normed results obtained with reference model (—), multi-scale macro model (—), and multi-scale micro model (—); the underlined macro-model borders (–·–); AA' data extraction line (– –).

structure described in [2], subject to the same operating conditions. Finally, this allows the region with the highest probability of defect occurrence, determined by the simulations, to be compared to the fault location determined by laboratory tests.

Fig. 16 shows a differential interference contrast microscopy (DIC) of the tested device [2] with overlapped simulated accumulated plastic strains after the tenth temperature cycle. The highest buckling occurs in the center of the device (between the PMet plates), as shown by the DIC's light red and blue color tones. The computed plastic strains from Fig. 16 are extracted from the M1 metal layer, along the AA' line, as shown in Fig. 11. The multi-scale model and the reference model lead to the same predicted failure spot with almost the same precision. The blue line represents the region where the multi-scale model is localized. The interpolated micro-model results back on the macro-model (between x = 925μm and x = 1000μm) are similar to reference model results.

Fig. 16 reveals in the failure spot region that defect appears between two adjacent metal lines that accumulate the highest plastic strain values.

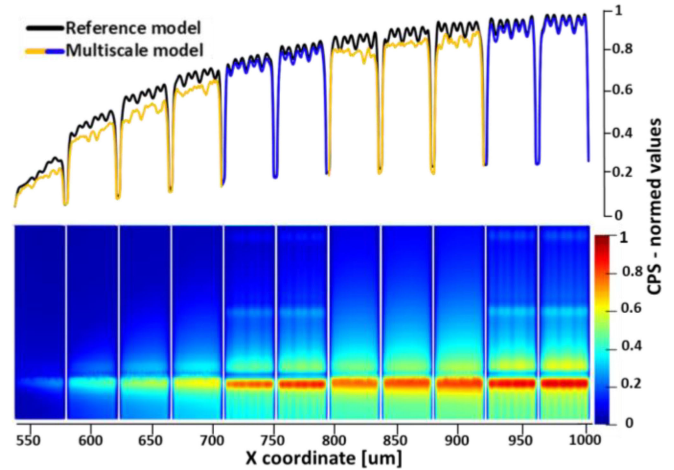

FIGURE 17. CPS normed values at the end of 10th cycle simulated on two localized regions (—) (top), slice through 1st metallization layer (bottom).

Analyzing another region, where no localization study was defined, a larger deviation between the reference and multi-scale (only macro) model results is observed, for example, between x = 700 μm and x = 850μm in Fig. 16. In order to check the accuracy and reliability of the multi-scale simulation method, the localization study is extended with one more region on the macro-model (between x = 700μm and x = 800μm). Hence, on the second localization region, the new resulted CPS gets very close to CPS computed on the reference model, Fig. 17 top.

The 2D color plot of the plastic strain extracted through the M1 layer at the end of the 10th simulated cycle is presented in Fig. 17 bottom. The localization of the micro-model in the two regions (1st between x = 1000μm and x = 925μm and 2nd between x = 700μm and 800μm) highlights how the macro-model results are enriched by all micro-model geometrical details.

The localization procedure can be easily extended if the partition of the macro-model into multiple (or entirely) micro sub-models is necessary.

D. MULTI-SCALE METHOD EFFICIENCY

The efficiency of the proposed multi-scale method is assessed by comparing the computational resources (CPU time and RAM usage) with the resources taken by the reference simulation model.

The CPU time used to solve the reference model during one temperature cycle is 25h and 22min. The average RAM usage was 99.2Gb, while periodic peak memory consumption reached all RAM available (128Gb) to complete the study.

The CPU time of the multi-scale model, when only one localization is considered, is 4h 54min for an average RAM usage of 42.2Gb. This means that the efficiency is 80.7% concerning the CPU time and 57.5% concerning the RAM usage.

When the multi-scale model is localized on two regions, the CPU time slightly increases to 6h and 37min, due to the

distributed computation and additional interpolated results, but the RAM usage remains at the same level as in the case of one region localization. Thereby, the CPU time efficiency is 73.9%.

V. CONCLUSION

A novel multi-scale method, based on sub-modeling techniques for IC reliability analysis by numerical simulation, has been presented. For efficient and accurate thermo-mechanical simulations, a two-way multi-scale localization method is proposed.

The multi-scale method combines two models: macro (full geometry, but few details) and micro (limited or localized geometry, but full details). The macro-model with equivalent homogenous material properties, related to heterogeneous regions of the real reference model (very complex) is defined and computed during the bottom-up stage. Localization transfers the computed plastic strain macro-model results onto a smaller region, micro sub-model in the top-down analysis step. The iterative enrichment (based on the two-way multi-scale method) of the macro-scale with the micro-scale simulation results, combined with the macro-model localization regions, links to multiple micro sub-models and allows obtaining detailed results over larger regions of the computational model. The comparison between the one-way multi-scale method, and the proposed two-way multi-scale method, shows a better accuracy of the latter one, compared to the reference model.

The multi-scale simulation method is implemented and validated on a real test chip structure, defined according to [2]. The results are compared to a reference study and measurements presented in [2]. The CPS-based localization method shows that the micro-scale model localization accurately predicts the failure spot recorded during laboratory tests [2]. The method leads to a considerable decrease in computational costs, while the results accuracy matches those simulated using the conventional direct FEM. Comparisons between the multi-scale method and reference results (based on the methodology presented in [2]) show an average relative error under 2%. The CPU time is reduced by 80.7% and the required RAM is reduced by 57.5%.

The proposed method facilitates the partitioning of the macro-model into multiple micro-models, which can be solved independently via distributed parallel computation. Hence, the entire IC structure can be solved in detail, providing an accurate overview allowing the analysis of the possible interaction between different regions or between detailed features of the studied device.

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