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TCAD Evaluation of the Active Substrate Bias Effect on the Charge Transport of Ω-Gate Nanowire MOS Transistors With Ultra-Thin BOX

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ABSTRACT This work presents an analysis of the application of active substrate bias (or back bias) on the charge transport properties of n-type Ω-gate SOI nanowire MOS transistors with thin buried oxide (BOX) and variable fin width. Additionally, the influence of back bias on the electrical parameters of these devices is also investigated through DC parameters such as on-to-off-state current ratio and DIBL. The evaluation is conducted by 3D TCAD simulations calibrated with experimental data. The application of negative back bias on nMOS transistors not only shifts the threshold voltage, but also causes mobility degradation due to the negative potential on the channel pushing the charges against the gate oxide interface. On the other hand, when positive back bias is applied, despite the mobility improvement allowed by the back channel's superior mobility and the front channel's less compacted inversion layer, at higher substrate bias levels, a strong mobility degradation is observed in the back channel due to the substrate's high electric field, resulting in reduction of the channel's overall effective mobility. The application of positive substrate bias degrades the subthreshold slope, leading to smaller on-to-off-state current ratio, as well as the reduced control of channel charges by the gate electrode worsens the DIBL.

INDEX TERMS Mobility, nanowire MOS transistors, substrate bias, thin BOX.

I. INTRODUCTION

In search of solutions for the performance and fabrication limits imposed by the scaling of the planar MOS technology, the interest for three-dimensional devices has, since their conception, been high as the semiconductor industry and the scientific community work together to keep up with the predictions made by Moore [1]. The use of multiple-gate transistors such as the FinFET in modern applications is nothing new as foundries recognize its potential and have since been taking advantage of the improved electrical performance allowed by the reduced cross-section dimensions and increased current drive of these devices.

The strong immunity to short-channel effects achieved by the electrostatic coupling of double and triple-gate FinFETs with smaller cross-section dimensions, especially in association with the SOI (Silicon-On-Insulator) technology, propitiates the reduction of fin width (W_{FIN}) and fin height (H_{FIN}) down to a decade of nanometers. Such devices have since been classified as nanowire MOS transistors [2], [3]. The enhanced electrical performance of nanowires is evidenced by the improved threshold voltage (V_{TH}) and subthreshold slope (S), as well as lower off-state current (I_{OFF}) and higher on-state current (I_{ON}) [4].

Another technological improvement that has been thriving in nanoelectronics applications recently is achieved by the reduction of the buried oxide (BOX) layer's thickness, with devices such as the UTBB (Ultra-Thin Body and BOX) receiving more attention and the use of thin BOX layers, in the order of 25nm, becoming a suitable option for ultra-scaled planar SOI transistors [5], [6]. This feature is convenient for the application of the active substrate biasing (or back biasing) technique, generally used for threshold voltage control [7]. In addition, other parameters can be affected when a device is under back biasing conditions,

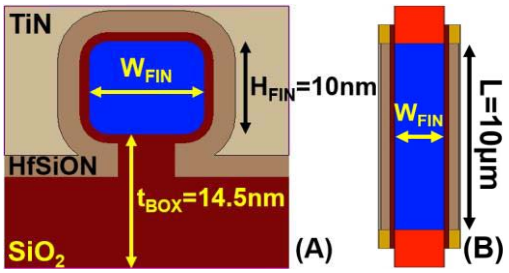

FIGURE 1. Cross-sectional (A) and top view (B) two-dimensional cuts of the simulated Ω-gate SOI nanowire MOSFET structure with fin width of 12nm.

being verified in analog aspects such as voltage gain and output conductance [8], but also in the carrier mobility of FDSOI devices [9]–[12] and Ω-gate nanowires [13], [14], with both favorable and unfavorable results to the mobility.

By combining the benefits of the nanowire geometry and the UTBB properties, the purpose of this paper is to investigate through a simulated environment the impact of substrate biasing in the effective mobility and in the performance of n-type Ω-gate nanowire MOS transistors with ultra-thin BOX layer for a wide range of negative and positive back bias (V_B). The study is carried over through calibrated 3D TCAD simulations [15] with experimental data.

II. DEVICE CHARACTERISTICS AND SIMULATION SETUP

The simulated structure of Ω-gate SOI nanowires were based on equivalent devices fabricated at CEA-Leti from 300mm (100) SOI wafers with buried oxide thickness (t_{BOX}) of 145nm [4], presenting similar architecture and geometrical characteristics, with exception of the t_{BOX} which was reduced by a factor of 10 to perform simulations with thin BOX. The geometrical aspects of the devices are 10nm fin height and a gate stack composed of 2.3nm HfSiON and 5nm TiN, with an effective oxide thickness (EOT) of 1.2nm. For the mobility analysis devices with long channel ($L = 10\mu m$) were simulated. For the performance evaluation channel length was reduced to 40nm. The devices present W_{FIN} of 12, 17 and 22nm and BOX thickness of 14.5nm. Fig. 1 shows cross-sectional and top view cuts of the simulated structure for the nanowire with W_{FIN} of 12nm.

To improve the accuracy of the simulations, adjustment of the physical model parameters was performed by comparing the results to experimental data from the devices with thick BOX, using an equivalent simulation structure with the same t_{BOX} of 145nm. Fig. 2 shows the experimental and simulated I_{DS}-V_{GS} curves for the nanowires with t_{BOX} of 145nm and W_{FIN} of 12nm with V_B varying from 0 to 100V while Fig. 3 presents the results comparing the experimental and simulated effective mobility variation with back bias in relation to mobility at $V_B = 0$ ($\Delta\mu_{eff}$) after the parameter adjustment. In order to extract the mobility using the Split-CV method [16], simulations of drain current (I_{DS}) vs. gate voltage (V_{GS}) and gate-to-channel capacitance (C_{GC}) vs. V_{GS} curves at low drain bias ($V_{DS} = 40mV$) were

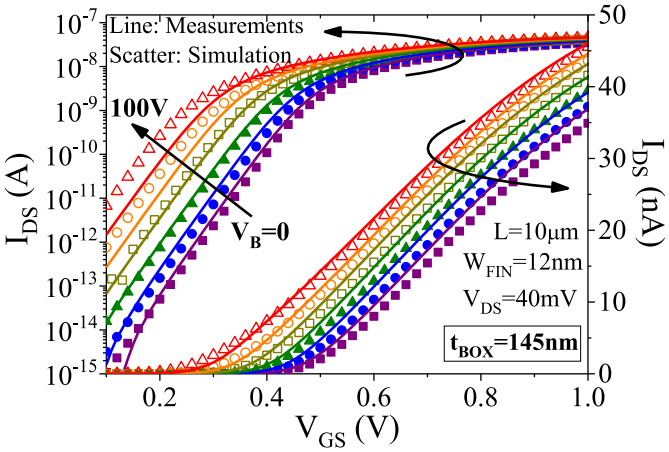

FIGURE 2. Measured and simulated drain current as a function of V_{GS} for n-type Ω-gate SOI nanowires with t_{BOX} of 145nm and W_{FIN} of 12nm.

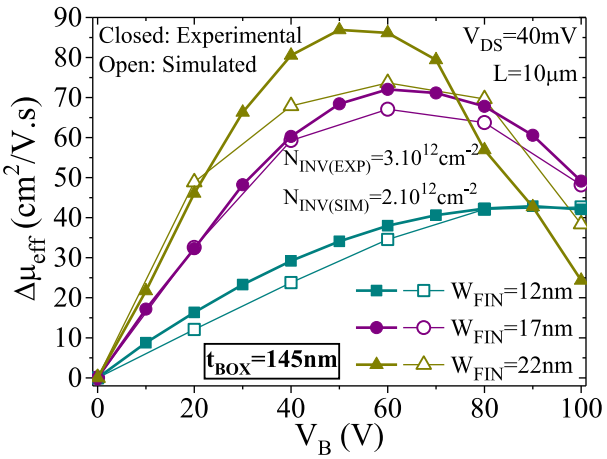

FIGURE 3. Experimental and simulated effective mobility variation as a function of V_B for n-type Ω-gate SOI nanowires with t_{BOX} of 145nm and W_{FIN} of 12, 17 and 22nm.

performed, with substrate bias (V_B) ranging from −10 to 10V with a 2V step. The physical models included in the simulations account for the mobility degradation with perpendicular and parallel electric fields, differentiation of the crystalline orientation, saturation velocity, carrier generation and recombination with doping dependent lifetime and bandgap narrowing. Since the devices present highly scaled dimensions, quantum confinement is accounted for by the Density Gradient Quantization model. The results of Figs. 2 and 3 show good agreement between experimental and simulated data. From the results of extracted mobility as a function of V_B (Fig. 3) one can see that the simulated data undermines the substrate bias influence on $\Delta\mu_{eff}$ for the wider W_{FIN} device, which does not affect the analysis carried-out in this work.

III. RESULTS AND DISCUSSION

Initial evaluation of the devices' electrical properties in terms of transfer characteristics was performed by extracting the threshold voltage (V_{TH}) and subthreshold slope (S) for

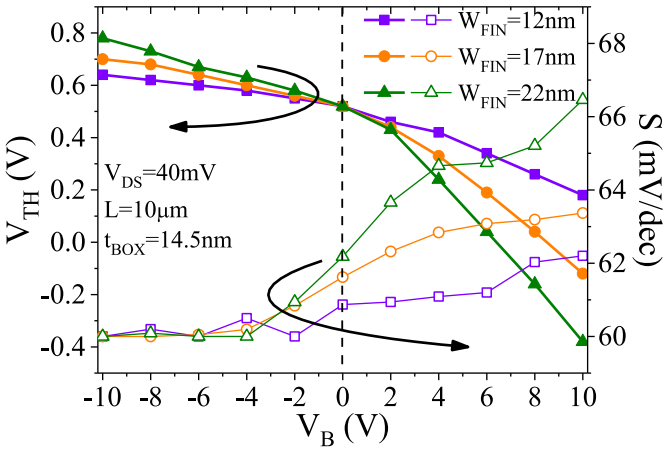

FIGURE 4. Threshold voltage and subthreshold slope as a function of substrate bias for simulated n-type Ω-gate SOI nanowires with thin BOX and fin width of 12, 17 and 22nm.

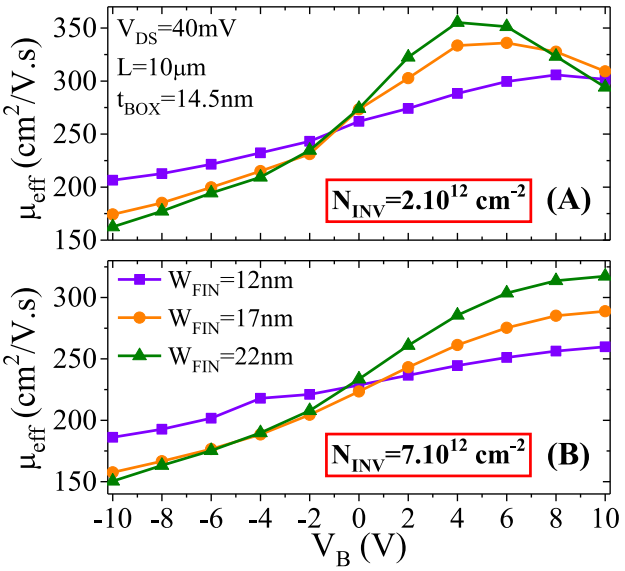

FIGURE 5. Effective electron mobility as a function of substrate bias for simulated n-type Ω-gate SOI nanowires with thin BOX and fin width of 12, 17 and 22nm at inversion charge density values of 2.10^{12} (A) and 7.10^{12} cm^{-2} (B).

the range of applied substrate bias, with the results being presented in Fig. 4. The V_{TH} was extracted using the second-derivative method [17]. The curves show a linear variation of V_{TH} with V_B, where the slope depends both on the device's fin width and on the back bias polarity. Widening the fin leads to an increased area of the Si-BOX interface, whereas it reduces the electrostatic coupling between the top and side-wall gates, which leads to higher V_{TH} variation with V_B: the $\delta V_{TH}/\delta V_B$ for positive V_B range increases from 34mV/V to 100mV/V as W_{FIN} increases from 12 to 22nm, agreeing with the results of [18] for tri-gate nanowires with ultra-thin BOX. The positive V_B application induces the formation of a channel in the Si-BOX interface, referred to in this work as the back channel (BC). With the application of negative back bias one can see that the $|\delta V_{TH}/\delta V_B|$ clearly reduces with respect to the positive V_B side of the curve regardless of W_{FIN}. On the other hand, the $|\delta V_{TH}/\delta V_B|$ increase with smaller V_B is higher for wider devices.

For the subthreshold slope, negative back bias can reduce S down to the theoretical limit for T = 300K (60mV/dec), due to the improved control of channel charges by the gate electrode, while the opposite effect is seen for positive V_B. Narrow transistors present higher immunity to S degradation, but for wider transistors the initial conduction on the BC prior to the front channel (FC) causes the subthreshold slope to slightly increase. Nevertheless, the devices present good electrostatic integrity, since the worst scenario shows an S of 66.4mV/dec, at $V_B = 10V$ and $W_{FIN} = 22nm$.

The extracted effective electron mobility was plotted against inversion charge density (N_{INV}), which was calculated using the C_{GC}-V_{GS} curves as per usual in Split-CV method. Two regions of inversion charge density were selected to obtain the mobility from: at weak inversion ($N_{INV} = 2.10^{12}$ cm^{-2}), which is closer to the maximum mobility, and at the higher inversion level ($N_{INV} = 7.10^{12}$ cm^{-2}) where carriers are more affected by the front gate's electric field. The effective electron mobility is presented in Fig. 5 as a function of V_B for fin widths of 12, 17 and 22nm at both N_{INV} values. In n-type devices, negative back bias causes the inversion charges to be pushed against the Si-gate oxide interface, leading to degradation of the electron mobility due to surface roughness scattering. The opposite effect is expected for positive back bias, with charges in the front channel being less affected by the surface roughness of the gate oxide-silicon channel interfaces, at $N_{INV} = 2.10^{12}$ cm^{-2}, in Fig. 5(A). However, for sufficiently high V_B a reduction in the mobility is observed. This reduction is higher for the wider devices. It can be observed for $V_B = 10V$ for $W_{FIN} = 12nm$, $V_B \geq 8V$ for $W_{FIN} = 17nm$ and $V_B \geq 6V$ for $W_{FIN} = 22nm$. At higher N_{INV}, in Fig. 5(B), the effect is minimized, and the mobility presents a monotonic variation with back bias, since at high V_{GS} the inversion charges are controlled predominantly by the front gate. The effects of both negative and positive V_B in mobility are enhanced as W_{FIN} increases due to the stronger control of charges by the substrate electrode and weaker control of charges by the gate electrode. Also, despite the mobility reduction at weak inversion charge density, the use of positive substrate biasing in the n-type nanowires resulted in mobility enhancement compared to the scenario where the substrate is grounded.

To investigate the causes for the mobility reduction for positive V_B, the gate-to-channel capacitance curves were used to examine conduction in the back and front channels at different V_B levels. Since a sudden capacitance rise is noticed when conduction begins in either the top or bottom interfaces, the $\delta C_{GC}/\delta V_{GS}$ curve can be used indicate the activation of the BC and of the FC [19]. The inset in Fig. 6(A) shows $\delta C_{GC}/\delta V_{GS}$ as a function of V_{GS} for

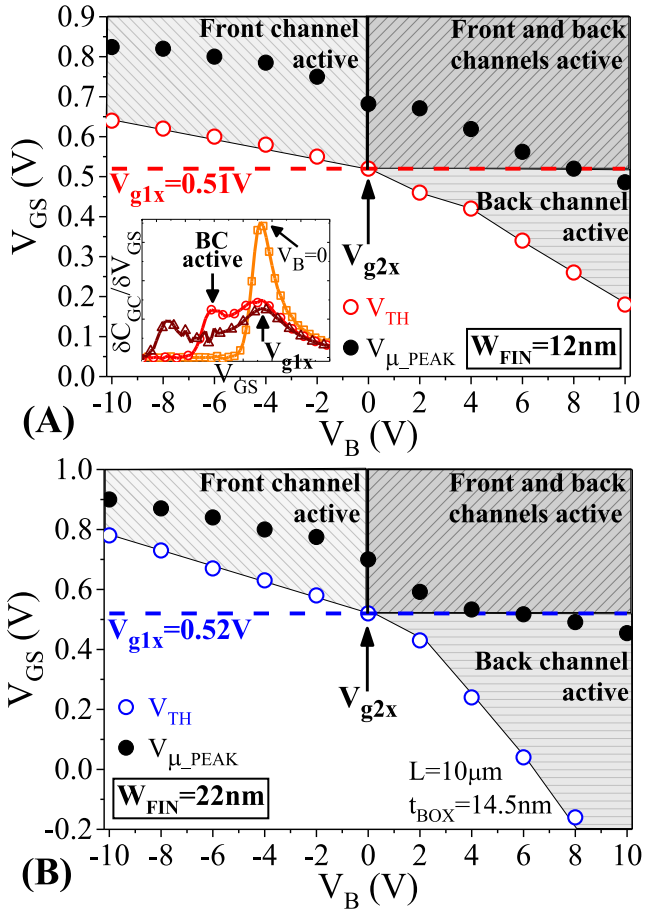

FIGURE 6. V_{TH}, V_{μ_PEAK}, V_{g1x} and V_{g2x} as a function of V_B for simulated n-type Ω-gate SOI nanowires with thin BOX and W_{FIN} of 12nm (A) and 22nm (B). Inset displays $\delta C_{GC}/\delta V_{GS}$ vs. V_{GS} for V_B of 0, 6 and 10V and W_{FIN} = 17nm. The patterned areas show the regions of gate and substrate bias for which front and/or back channels are activated.

W_{FIN} = 17nm at V_B = 0, 6 and 10V. When two peaks are observed in the curves, it means that the BC is being activated prior to the FC activation. The parameter V_{g1x} is obtained at the second peak of the curve and represents the activation of the FC. From this point onward ($V_{GS} > V_{g1x}$) the conduction occurs in both the BC and FC simultaneously. Then, the procedure described in [19] was performed to obtain the conduction profile of the nanowires. Fig. 6 presents V_{TH}, V_{μ_PEAK}, V_{g1x} and V_{g2x} as a function of back bias for the devices with W_{FIN} of 12nm and 22nm, where V_{μ_PEAK} is the gate bias at which the extracted mobility curve has its peak value and V_{g2x} is the intercept of V_{TH} and V_{g1x}, at which point FC and BC are simultaneously active. For negative V_B, since the back channel is not active when $V_B < V_{g2x}$, the μ_{eff} values in this region correspond to mobility in the FC. For positive V_B, the mobility peak is mostly found in the region where both FC and BC are active or at weak inversion ($V_{GS} \approx V_{g1x}$). For the cases where V_{μ_PEAK} is smaller than V_{g1x}, since the FC is not active for $V_{GS} < V_{g1x}$, the mobility can be attributed to the region where only the BC is active.

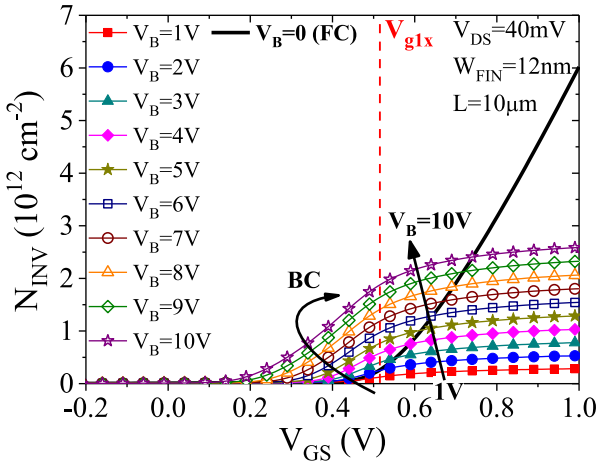

FIGURE 7. Inversion charge density in the front (line) and back (symbols) channels as a function of V_{GS} for different substrate bias for simulated n-type Ω-gate SOI nanowires with thin BOX and fin width of 12nm.

Additionally, it is possible to isolate the mobility contribution of the back channel to verify the origin of the mobility. This is achieved by subtracting from the drain current at different back bias levels the curves that contain only the front channel component, which is the one at $V_B = 0$. Since it was demonstrated that for $V_B > 0$ both the BC and FC are active, after this subtraction only the BC component remains. By doing this for the drain current and the capacitance curves, and then performing the Split-CV technique, the μ_{eff} and the N_{INV} of the back channel are obtained. Fig. 7 shows the inversion charge density in the front channel ($V_B = 0$) and in the back channel (symbols) as a function of V_{GS} for the nanowire with $W_{FIN} = 12$nm, for a back bias range of $0 \leq V_B \leq 10$V. The curve for N_{INV} in the front channel shows an expected behavior, with the charge density increasing as the device move into the strong inversion region. However, for N_{INV} in the back channel, a noticeable plateauing of the curves is observed, starting roughly after the threshold voltage of the front channel (V_{g1x}), when the charges start populating front gate interface. After a certain gate bias, the inversion charge density in the FC overcomes the one in the BC. The V_{GS} at which this occurs increases as V_B is increased, due to the higher control of charges by the substrate electrode at higher back bias.

Fig. 8 shows the mobility in the front channel ($V_B = 0$) and in the back channel (symbols) as a function of V_{GS} at different V_B values for the simulated nanowires with W_{FIN} of 12nm and 22nm. The curves show a higher μ_{eff} in the BC than in the FC for most of the V_{GS} range when V_B is applied, leading to mobility increase, but μ_{eff} reduction is noticed as back bias increases from 1 to 10V, which at strong V_B is responsible for suppressing the initial mobility enhancement. Thus, although the contribution of the higher mobility in the BC leads to an increased mobility when compared to the curve for $V_B = 0$, the degradation in the BC may cause a decrease in μ_{eff} as the back bias increases. At high V_{GS} the charges are controlled mostly by the front

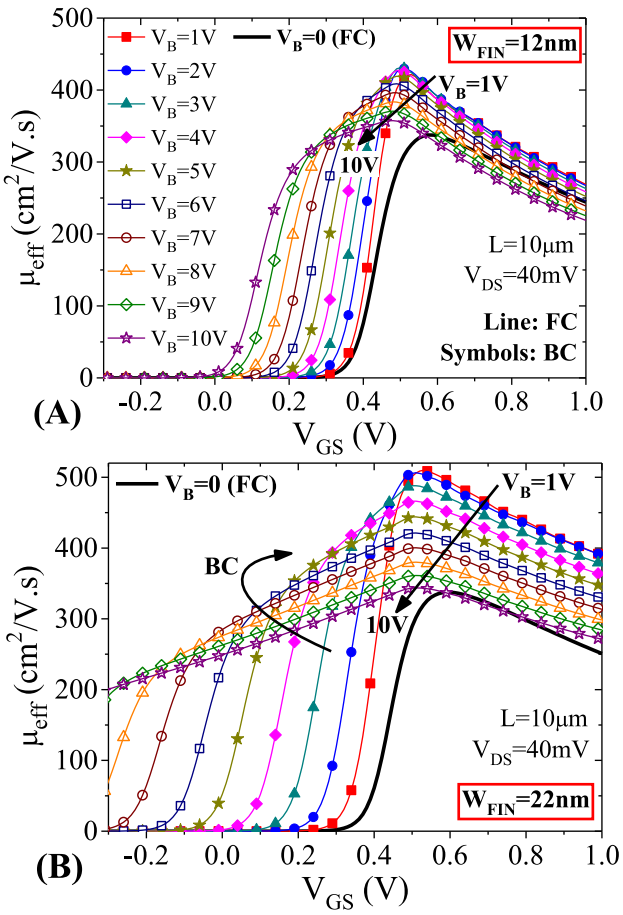

FIGURE 8. Effective electron mobility in the front (line) and back (symbols) channels as a function of V_{GS} for different substrate bias for simulated n-type Ω-gate SOI nanowires with thin BOX and fin width of 12nm (A) and 22nm (B).

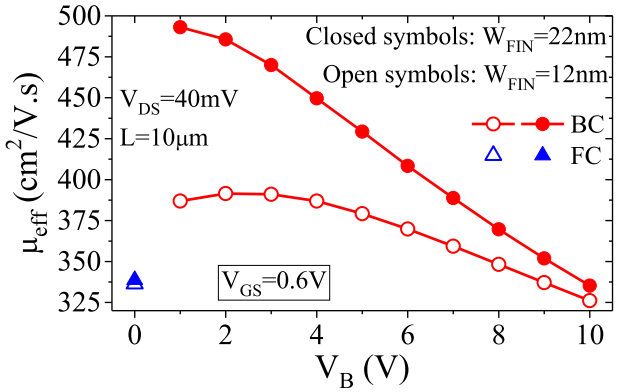

FIGURE 9. Effective electron mobility in the front and back channels as a function of back bias at V_{GS} = 0.6V for simulated n-type Ω-gate SOI nanowires with thin BOX and W_{FIN} of 12nm and 22nm.

gate, since they are mostly gathered in the FC, according to Fig. 7, so the contribution of the BC mobility is reduced in the strong V_{GS} region.

In Fig. 9, the mobility of each curve was extracted at a fixed V_{GS} value of 0.6V. While the variation in μ_{eff} between

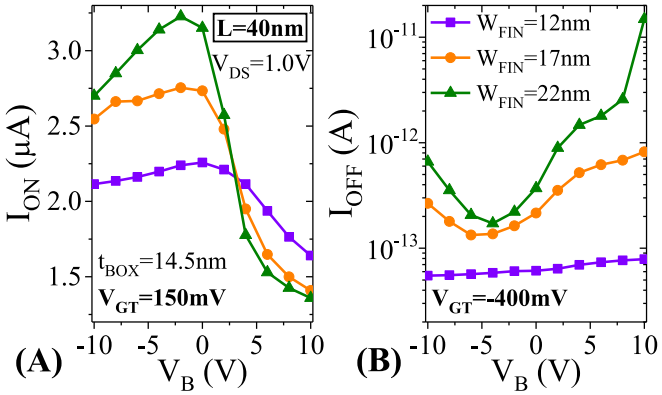

FIGURE 10. I_{ON} (A) and I_{OFF} (B) as a function of V_B for simulated n-type Ω-gate SOI nanowires with thin BOX, L of 40nm and W_{FIN} of 12, 17 and 22nm.

the FC and the BC can be as high as ~150 cm^2/V.s, depending on W_{FIN} and V_B, the back channel mobility presents a decreasing tendency with V_B. Even though its contribution to the overall mobility is smaller, since the charge density in the BC is lower than in the FC, as seen in Fig. 7, it still causes the effective mobility to reduce at higher V_B values. As V_B increases, the mobility in the BC suffers degradation due to the strong electric field of the substrate, thus, in transistors with larger W_{FIN}, this effect is even more pronounced. Finally, the decreasing pattern of μ_{eff} in the BC as V_B is raised reveals that the degradation is associated to the stronger electric field from the substrate leading to stronger Si-BOX surface roughness mobility degradation.

The mobility variation with back bias will also have an impact on the other device figures-of-merit, some of which are required to present suitable values, especially for short-channel transistors. To verify how the impact of active back biasing in the performance of short-channel nanowires, a structure with L = 40nm was simulated. This channel length has been selected as it is the shortest one to present drain induced barrier lowering (DIBL) smaller than 100 mV/V and S smaller than 80 mV/dec in the whole range of V_B and W_{FIN}. The first parameters to be examined were the on-state (I_{ON}) and off-state (I_{OFF}) currents, as well as the ratio (I_{ON}/I_{OFF}), extracted at V_{DS} = 1V and gate voltage overdrive ($V_{GT} = V_{GS}$-V_{TH}) of 150mV for I_{ON} and −400mV for I_{OFF}. These results are presented as a function of V_B in Figs. 10 and 11. The I_{ON} curves show a decreasing tendency with positive V_B, while the increase in I_{OFF} is caused by the subthreshold slope degradation. Additionally, the I_{OFF} increase for positive V_B is stronger than the I_{ON} reduction, thus, the degradation of I_{ON}/I_{OFF} in the positive back bias range can be attributed mostly to the increase of the off-state current, rather than the decrease of the on-state current. Similarly, for $V_B < -5$V, the slight reduction in I_{ON}/I_{OFF} for the wider transistors is related primarily to the I_{OFF} degradation.

Another analyzed parameter was the DIBL, presented in Fig. 12 as a function of substrate bias for the simulated

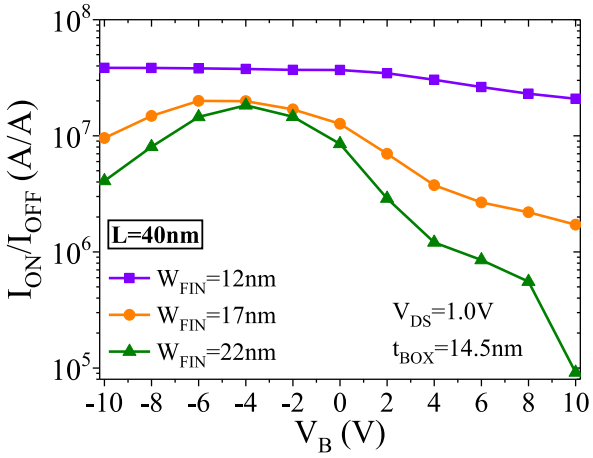

FIGURE 11. I_{ON}/I_{OFF} as a function of back bias for simulated n-type Ω-gate SOI nanowires with thin BOX, L of 40nm and W_{FIN} of 12, 17 and 22nm.

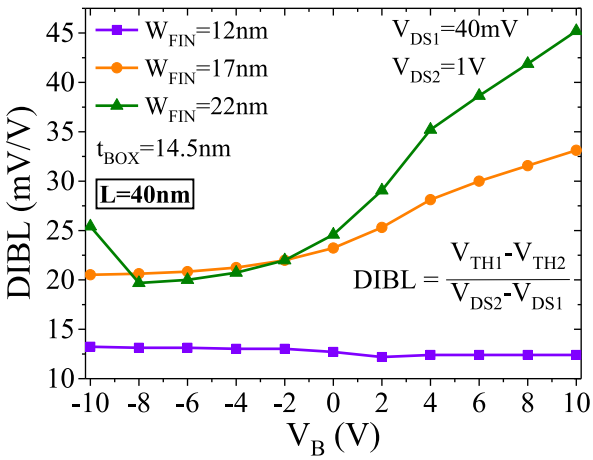

FIGURE 12. DIBL as a function of back bias for simulated n-type Ω-gate SOI nanowires with thin BOX, L of 40nm and W_{FIN} of 12, 17 and 22nm.

nanowires with fin width of 12, 17 and 22nm. Due to the initial control of the back channel by the substrate at weak inversion, the front gate's control over the charges is reduced when positive V_B is applied, leading to an increase in DIBL [20]. As the device's fin width is increased, the gate's electrostatic coupling is reduced, while the Si-BOX interface's area increases, which causes this effect to get stronger. For wider devices, where the inversion charges can spread along the back channel, another effect can also cause DIBL degradation with the increase of V_B, prompted by the high V_{DS}. The drain-induced fringing field can increase the surface potential of the Si-BOX interface, reducing the back channel's threshold voltage, which leads to increase in the DIBL [20]. However, for nanowires with such W_{FIN}, the results for a channel of L = 40nm demonstrated good immunity to this short-channel effect, presenting a DIBL of 45mV/V in the worst scenario, for W_{FIN} = 22nm and V_B = 10V.

IV. CONCLUSION

An evaluation on the charge transport properties of n-type Ω-gate SOI nanowires under active substrate biasing was performed through calibrated 3D TCAD simulation with experimental data. The impact of back bias on DC parameters related to short-channel effects was also examined. In long channel devices, mobility degradation is observed at negative substrate bias, induced by increased surface roughness scattering in the front channel's inversion layer. Under positive substrate bias, a conduction channel is formed in the Si-BOX interface, activated prior to the formation of the front channel. Although presenting higher mobility, the back channel is strongly affected by the substrate's electric field, causing mobility degradation in the back channel due to surface roughness scattering. At low inversion charge densities, where the back channel's contribution to the device's mobility is still significant, this degradation can lead to reduction of the mobility for high back bias, especially in wider devices. The analysis of short-channel devices demonstrates that the positive substrate bias has also caused significant increase of the off-state current, due to the worsened subthreshold slope, degrading the on-to-off-state current ratio. Also, degradation of the DIBL is observed for positive back bias due to loss in the control of charges in the channel by the gate electrode and to surface potential variation in the Si-BOX interface caused by drain induced fringing field. Overall, the performed analysis indicated that no clear advantage on the application of positive substrate bias on any nanowire regardless of the fin width for short-channel devices. Although the carrier mobility is increased with any positive substrate bias in comparison to its value at grounded substrate, a degradation has been observed in all devices' figures-of-merit. This degradation worsens as fin width is increased.

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