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Efficient Erase Operation by GIDL Current for 3D Structure FeFETs With Gate Stack Engineering and Compact Long-Term Retention Model

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ABSTRACT We have fabricated junctionless N-type silicon-on-insulator (SOI) ferroelectric-HfO_2 field effect transistors (FeFETs) with overlap and underlap structures between gate and drain/source regions to investigate the role of gate-induced-drain-leakage (GIDL) current in erase operation of FeFETs with a floating body. We also introduced a novel gate stack process for low voltage operation by inserting a Ti layer in the metal gate. The Ti layer insertion can suppress the growth of an interfacial layer (IL) by controlling oxygen intrusion into the IL during the rapid thermal anneal (RTA) process. We demonstrated an efficient erase operation at shorter and lower pulse voltage with GIDL current in the overlap structure than in the underlap structure. A compact FeFET retention model is developed based on the surface-potential based FET model, the nucleation-limited-switching (NLS) model, and the retention model of ferroelectric (FE) capacitor. Faster degradation of the program state observed in the experiment can be explained by electron detrapping according to the modeling and simulation.

INDEX TERMS Junctionless, FeFET, ferroelectric, HfO_2, GIDL, retention.

I. INTRODUCTION

The Recent advancement of Internet-of-Things (IoT) technologies with big data makes the data traffic between IoT edge devices and cloud servers heavier than ever seen. To store and process the large amount of data at edge devices, low-power and high-density non-volatile memories (NVMs) are required for IoT edge devices.

Since the discovery of ferroelec-HfO_2 (FE-HfO_2) [1], FeFET has attracted more attentions due to its small cell size, low-power and high-speed operation, and CMOS process compatibility. As NAND flash memories migrate from planar to 3D vertical structure, it is natural to consider the same structure for FeFET to achieve high density (Fig. 1). A 3D vertical FeFET has been previously proposed and demonstrated [2]. For the 3D vertical structure, N-type junctionless transistors with a floating body are arrayed serially as memory cells. Majority carriers (electrons) can be generated and supplied relatively fast, while minority carriers (holes) generation is relatively slow due to its N-type junctionless structure (Fig. 2). The generation of minority-carrier holes is important to fix the body potential, apply large voltage in the gate oxide, and balance with large ferroelectric polarization charge. 3D vertical NAND flash memories utilize GIDL current generated by the access transistor to supply minority-carrier holes for the efficient erase operation [3]–[5]. Therefore, it is useful to consider utilizing GIDL current for the erase operation in FeFET as well. Although there are relevant reports for

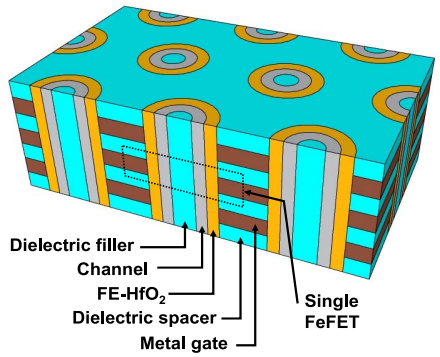

FIGURE 1. Schematic of a 3D vertical stack FeFET with FE-HfO_2 and deposited channel material.

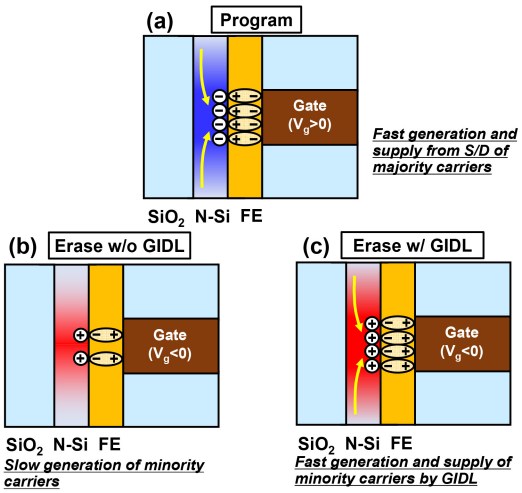

FIGURE 2. (a) Schematic of a program state of a 3D FeFET. (b) Schematic of an erase state of a 3D FeFET without GIDL. (c) Schematic of an erase state of a 3D FeFET with GIDL.

inversion-mode FeFETs [6], [7], however, it has not been fully studied for junctionless FeFET, yet. Another challenge of HfO_2-based FeFET is the low-k interfacial layer (IL) growth during rapid thermal annealing (RTA) process, which causes large voltage drop on the IL, divides gate voltage, prevents low-voltage operation, and leads to reliability problems. One possible solution is to insert oxygen scavenging material such as Ti to suppress the growth of the IL in the metal/HfO_2/Si gate stack during high temperature RTA process as reported [8]. However, it is not clear whether it also works for metal/FE-HfO_2/Si gate stack in the relatively lower temperature process. Moreover, a compact retention model for FeFET with FE-HfO_2 is needed based on the previous understanding of polarization switching for reliability estimation and device engineering toward storage memory applications.

In this work, first, we design SOI junctionless FeFETs with overlap and underlap source/drain structures to study the impact of GIDL-induced hole carriers. Next, we develop a process of Ti layer insertion in the gate stack of the

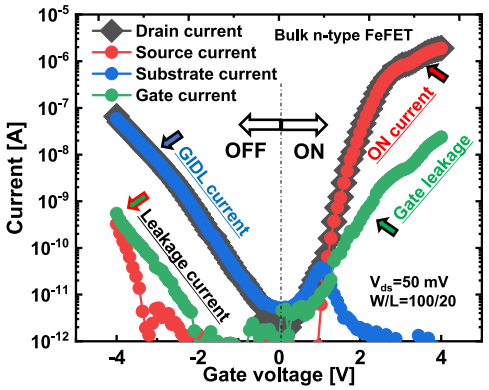

FIGURE 3. Measured I_d, I_s, I_g, I_{sub} of a bulk FeFET with overlap in the gate-last process. Only forward sweep data is shown for clarity.

FeFETs to suppress the IL growth and reduce the operation voltage. Then, we study the erase operation of the SOI junctionless FeFETs with overlap (large GIDL current) and underlap (small GIDL current) structures [9]. Finally, a compact long-term retention model for FeFETs with FE-HfO_2 is developed by considering the FE model, the NLS model [10]–[14] and the charge-trap model in gate oxide [15]–[17]. This paper is an extended version of the previous conference proceedings [18] by adding detail descriptions of the technical contents, physical analysis, and electrical characterization.

II. EFFECT OF GIDL CURRENT IN ERASE OPERATION

A HfO_2-based FeFET has a gate oxide with large dielectric constant and polarization charge, which can induce the large surface electric field at the gate-drain overlap region in negative gate voltage (V_g). Even with small drain voltage (V_d), GIDL current can be induced at the gate-drain overlap region. To observe the GIDL current, we fabricated and measured a bulk n-type FeFET with 10nm $HfZrO_2$ (HZO) by gate last process. Fig. 3 shows the measured I_d, I_s, I_{sub} and I_g versus V_g curves at $V_d = 50$mV in forward V_g sweep. In negative V_g, I_{sub} is equal to I_d, while I_s and I_g are very low, which indicates that large GIDL current is induced in the bulk FeFET at low V_d.

Before conducting our experiment, we explored the role of GIDL current in SOI junctionless FeFETs for erase operation by TCAD simulation with a GIDL current model [19]. The carrier transport was modeled by drift-diffusion. The default parameters in the TCAD was used for Si. The Schenk model was used for band-to-band tunneling (BTBT) current in GIDL. Although the Schenk model is based on local BTBT and not as accurate as non-local model, however, it is useful for qualitative discussion and for less computation load. The Preisach model was used for ferroelectric. The remanent polarization (P_r) was 3.5μC/cm^2 and the coercive field (E_c) was 1.16MV/cm based on the parameter extraction in our previous work [20]. Transient simulations were performed in the bidirectional V_g sweep with DC (slow) sweep for 0.1s (12.5ms/V) and fast sweep for 100ns (12.5ns/V).

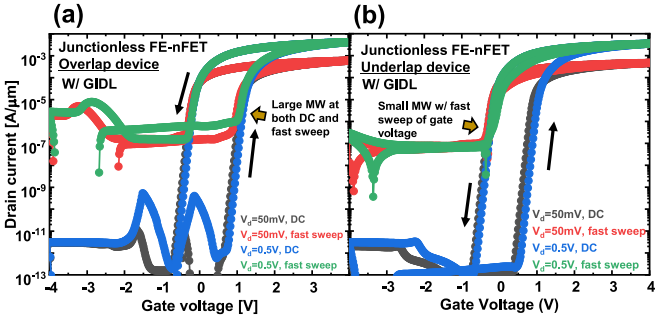

FIGURE 4. Simulated I_d-V_g of junctionless FeFETs with gate-drain overlap (a) and underlap (b) in DC/fast sweep at V_d = 50mV and 0.5V.

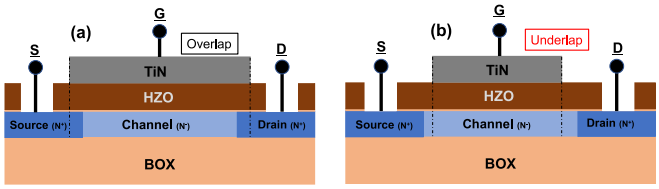

FIGURE 5. Schematic illustration of SOI N-type FeFETs with overlap (a) and underlap (b) structures.

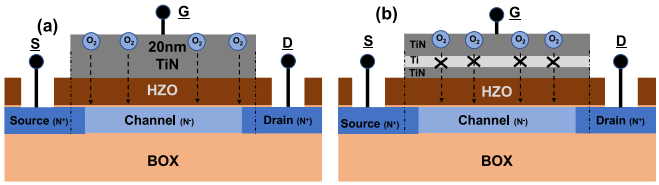

FIGURE 6. Schematic illustration of SOI N-type FeFETs with (a) single 20nm TiN gate and (b) 5nm TiN/5nm Ti/10nm TiN gate.

Fig. 4 shows the simulated I_d-V_g curves of FeFETs with gate-drain (a) overlap and (b) underlap at low and high V_d with different V_g sweep speed. The V_g sweep begins from positive voltage to negative voltage, then return to positive voltage. For DC sweep, the overlap device has higher GIDL current than the underlap device at negative V_g, since band-to-band tunneling occurs easily at the high-doped region (drain) but hardly at the low-doped region (channel). However, they have almost the same memory window (MW), this is because, even though GIDL current is small, minority carrier holes can be thermally generated in the body in the nearly infinite time of each negative V_g step in DC sweep. In contrast, for the fast sweep, the MW does not exist in the underlap device, because minority carrier holes are not generated in the limited time of each negative V_g step. As V_d increases, GIDL current of the overlap device increases. But GIDL current of the underlap device increases little and the threshold voltage (V_{th}) does not increase by erase operation, thus MW does not exist. Note that the constant current in the off-state is due to the displacement current thought the capacitors of the simulated transistors, and proportional to the sweep rate.

III. DEVICE FABRICATION

Junctionless N-type FeFETs were fabricated on SOI substrate to emulate the floating-body structure of 3D vertical FeFETs in the university lab. To study the role of GIDL current for erase operation, gate-drain overlap and underlap structures were designed corresponding to high and low GIDL current as shown in Fig. 5. Moreover, to study low-voltage operation of FeFETs, a gate stack process with Ti layer insertion was also developed as shown in Fig. 6. The IL growth is mainly due to the growth by the residual oxygen in the films and the ambient oxygen. The thickness of the bottom TiN layer, the Ti layer, and the top TiN layer are 5nm, 5nm and 10nm, respectively. This stack was optimized so that Ti does not induce excess oxygen vacancy in HZO but sufficiently scavenges oxygen.

Three devices with different gate stacks were fabricated by the gate-last process: Device A, 20nm TiN and 15nm HZO; Device B, 20nm TiN and 10nm HZO; Device C, 10nm TiN/5nm Ti/5nm TiN and 10nm HZO. After RCA cleaning, first, a SOI substrate was thinned down to 20nm by thermal oxidation and HF etching. Then, the SOI received ion-implantation and thermal activation for lightly-doped channel formation, followed by ion-implantation and thermal activation for the source and drain regions. Before depositing gate oxide, RCA cleaning was done and then chemical oxide was grown on SOI by diluted SC1 solution (NH_4OH : H_2O_2 : H_2O = 2 : 5 : 200). Next, 15nm HZO (Device A) and 10nm HZO (Device B, C) were deposited by Atomic Layer Deposition (ALD) at 250°C. 20nm TiN (Device A, B) and 10nm TiN/5nm Ti/5nm TiN were deposited as metal gate by RF sputtering. After gate patterning and soure/drain contact opening, 20nm TiN / 2nm Ti were deposited by RF sputtering and patterned. Finally, RTA was done for 10sec at 500°C for HZO crystallization and Ti silicide formation.

Metal/FE-HfO_2/Insulator/Semiconductor (MFIS) capacitors were also fabricated on N^+ Si substrate to compare the ferroelectricity without and with Ti layer insertion in the metal gate stacks: Capacitor D, 20nm TiN/10nm HZO/N^+-Si substrate; Capacitor E, 10nm TiN/5nm Ti/5nm TiN/10nm HZO/N^+-Si substrate; corresponding to Device B and Device C, respectively.

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

A. PHYSICAL ANALYSIS AND THE FE-CAPACITORS

Fig. 7 (a) and (b) show the cross sectional TEM images of Device B and C, respectively. HZO is fully crystallized after RTA for both TiN and TiN/Ti/TiN gate metal. To distinctly compare the thickness of IL, HAADF-STEM images with high Z-contract were also taken as shown in Fig. 7 (c) and (d). The thickness of the IL with TiN/Ti/TiN gate metal is thinner than with TiN gate metal and almost the same as that of the chemical oxide after diluted SC1. This result indicates that the growth of the IL during RTA is effectively suppressed by preventing oxygen intrusion by the Ti layer.

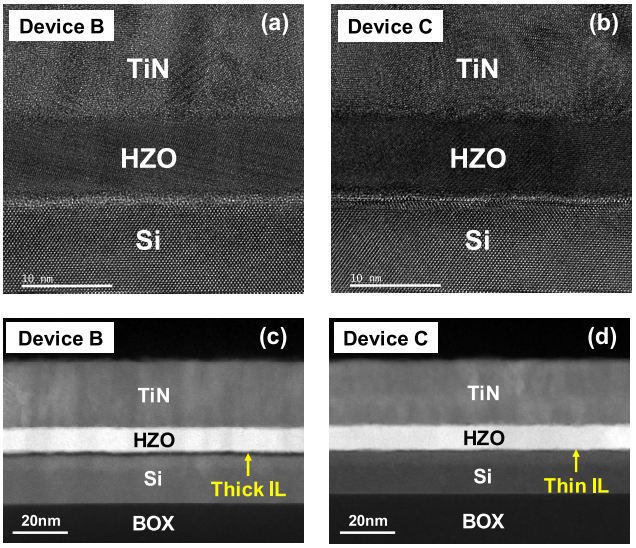

FIGURE 7. Cross sectional TEM (a, b) and HAADF-STEM (c, d) images of the gate and channel region of Device B and Device C.

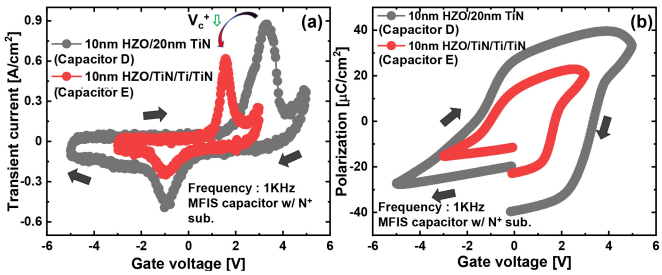

FIGURE 8. Measured (a) I-V and (b) P-V curves of the MFIS capacitors on N^+-Si without Ti layer insertion (Capacitor D) and with Ti layer insertion (Capacitor E).

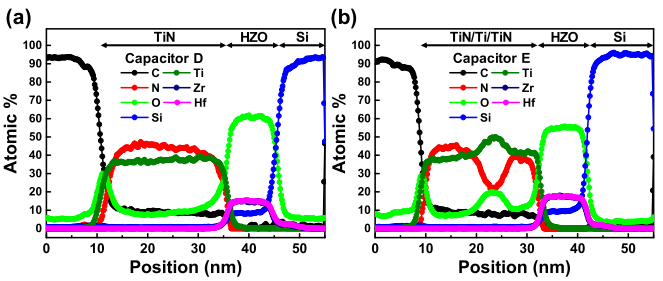

FIGURE 9. Measured EDX line-scan profiles of (a) Capacitor D and (b) Capacitor E. The Si signal in the HZO layer is an artifact and not taken into account for analysis. The O signal is partly from FIB sample preparation by O_2 plasma.

Measured I-V and P-V curves of the MFIS capacitors with and without Ti layer insertion are shown in Fig. 8, which correspond to Capacitor D and E, respectively. 1 kHz triangle voltage was applied for the measurement. The positive switching voltage of Capacitor E is lower than that of Capacitor D, however, the negative switching voltages of the capacitors are nearly the same. The polarization charge is smaller in Capacitor E than in Capacitor D. To understand the ferroelectric characteristics in the capacitors, we conducted EDX line-scan analysis as shown in Fig. 9. The Ti layer

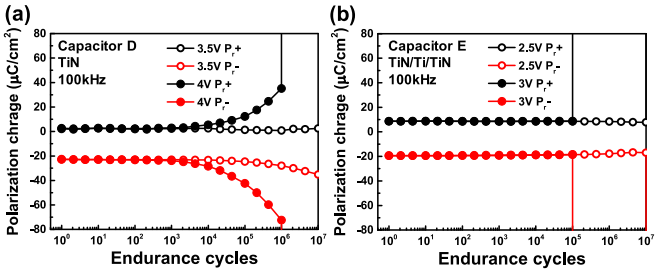

FIGURE 10. Measured endurance characteristics of (a) Capacitor D and (b) Capacitor E. The stress voltages are 3.5V and 4.V for Capacitor D, and 2.5V and 3V for Capacitor E. The stress frequency is 100kHz.

contains oxygen absorbed through the TiN layers. Although the line-scan analysis is not perfectly qualitative, the oxygen content is relatively smaller in Capacitor E than in Capacitor D. More oxygen vacancies can exist in Capacitor E than in Capacitor D and they form positive fixed charges. Thus, the fixed charges shift the switching voltages in the negative V_g direction. The difference of the polarization charge can be also made by the difference in the ferroelectricity with oxygen vacancy, which influences the stability of the ferroelectric phase [21], [22].

We studied endurance characteristics of Capacitor D and E by applying bipolar voltage pulses. It is not straight forward to estimate the electric field across the HZO layer. To make fair comparison, amplitudes of the pulse voltage are set to the polarization switching voltage +0.5V and +1.0V: 3.5V/4.0V for Capacitor D, and 2.5V/3.0V for Capacitor E. Fig. 10 shows endurance characteristics measured by the stress conditions. Capacitor E shows relatively lower endurance than Capacitor D. Capacitor D shows a gradual increase in leakage current then a breakdown because the IL is thick and prevents immediate dielectric breakdown after the percolation path formation by oxygen vacancy in the HZO layer. On the other hand, Capacitor E shows sudden breakdown because the IL is thin and the percolation path formation immediately causes dielectric breakdown.

B. DC CHARACTERISTICS OF THE FABRICATED FEFETS

We designed the gate stack for low voltage operation of FeFETs. We compared DC I_d-V_g characteristics of Device A-C in Fig. 11 (a, b, d) measured by a semiconductor parameter analyzer. In this work, memory window (MW) was defined as the difference between high V_{th} after erase and low V_{th} after program. V_{th} was defined by the constant current method at the current level of 10^{-9}A/μm. Device A shows the largest MW but requires large sweep voltage, because of its thick HZO film and thus the large coercive voltage of the HZO film. By thinning down the HZO film, Device B shows the smaller MW but with lower sweep voltage which is, however, still larger than 2V. Note that Device A and Device B with overlap show hysteresis in I_d in the negative V_g region because of hole carrier generation and hole trapping near the interface. Hole trapping lowers the electric potential and field and thus reduces GIDL. Whereas

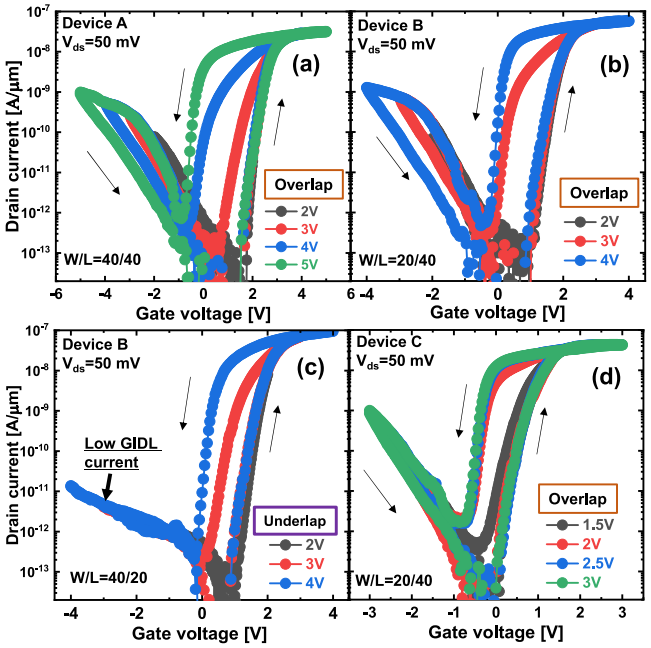

FIGURE 11. Measured I_d-V_g curves with different gate sweep voltage. (a) Device A with the overlap structure with 15nm HZO/20nm TiN, Device B with (b) the overlap structure and (c) the underlap structure, with 10nm HZO/20nm TiN, (d) Device C with the overlap structure with 10nm HZO/TiN/Ti/TiN.

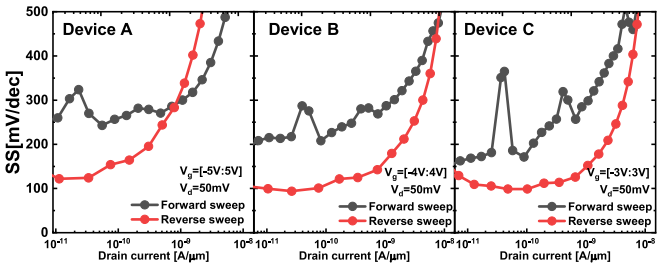

FIGURE 12. Extracted SS of Device A-C for forward and reverse sweep.

Device B with underlap does not show hysteresis because of less hole carrier generation. Device C introduces the 5nm Ti layer inside the TiN gate metal. This thin Ti layer works as oxygen scavenger [8] to block oxygen intrusion to the interface of HZO and Si, and avoids the IL growth. Note that the Ti layer does not induce remote scavenge [23] due to the low thermal budget process used in this work (500°C RTA). Device C shows the moderate MW even with the lowest sweep voltage less than 2V. The polarization switching voltages of Device B and C correspond to the coercive voltages of the MFIS capacitors in Fig. 8 (a). Fig. 12 shows the extracted subthreshold slope (SS) of Device A-C. SS is not degraded in Device C though HZO thickness is the same for all devices. This indicates that there is no significant increase in the interface density with the Ti layer insertion process. Note that SS is smaller in the reverse sweep than in the forward sweep [24]. In the forward sweep, the channel state changes from depletion to inversion. In the

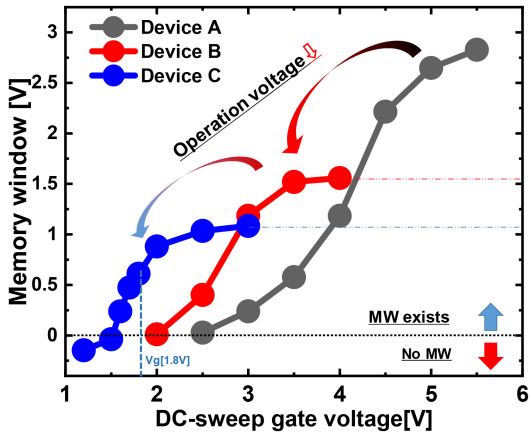

FIGURE 13. Extracted MW versus write gate voltage. MW decreases from Device A to Device C. Device C shows low voltage < 2V operation.

subthreshold region, V_g is largely dropped in the depletion layer and polarization switching does not occur till the channel state becomes inversion. In the reverse sweep, on the other hand, the channel state changes from inversion to depletion. In the subthreshold region, polarization switching large occurs when the channel state becomes depletion, the channel potential swings a lot, and thus SS becomes steep.

Fig. 13 summarizes the MW versus DC sweep voltage of Device A-C. From Device A to Device B, the write operation voltage decreases by thinning the ferroelectric gate oxide thickness, but the MW is still more than 1V. From Device B to Device C, the write operation voltage further decreases by thinning the IL. Particularly, Device C still has 0.7 V MW at 1.8V, which is promising for low voltage memory operation.

C. ERASE CHARACTERISTICS OF THE SOI JUNCTIONLESS FEFETS WITH OVERLAP AND UNDERLAP

The overlap and underlap devices have almost the same ON current, which indicates parasitic resistance in the underlap region is not severe. While large GIDL current flows in the overlap device, GIDL is suppressed in the underlap device, as shown in Fig. 11 (b) and (c). We characterized program and erase operations with variable pulse width and amplitude by using the measurement scheme in Fig. 14 (a) for Device B. First, initial V_{th} is obtained by using fast-IV measurement after set and reset pulse of initialization. Then, V_{th} shift (ΔV_{th}) is measured for variable program and erase pulses. V_d is 50mV for read operation. I_d-V_g curves of fast I-V measurement after program and erase pulses are shown in Fig. 14 (b).

Fig. 15 shows the contour plots of ΔV_{th} from the set or reset state after program/erase operation for the overlap (a) (b) and underlap (c) (d) devices at $V_d = 0$V. Program characteristics are almost the same for the overlap and underlap devices due to the junctionless structure. Note that $\Delta V_{th}|$ is relatively larger after erase than after program. This can be due to the asymmetric write voltage amplitude for program and erase from the flat band condition of the HZO

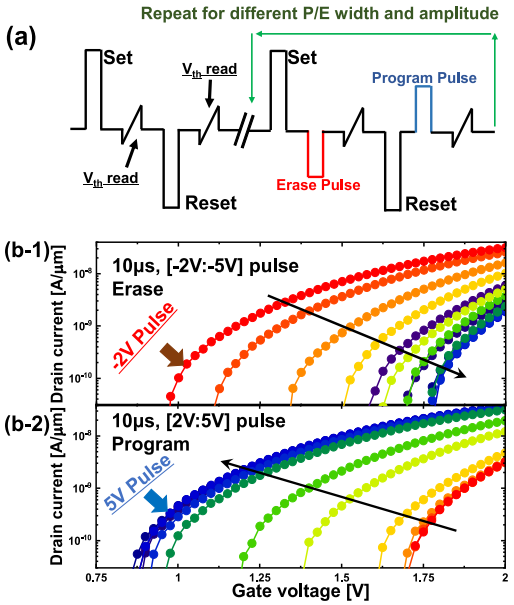

FIGURE 14. **(a) Schematic of the measurement scheme, Measured fast I_d-V_g curves of Device B with overlap by (b-1) erase pulse and by (b-2) program pulse. Fast I-V sweep range is set around V_{th} of the devices. V_d = 50 mV.**

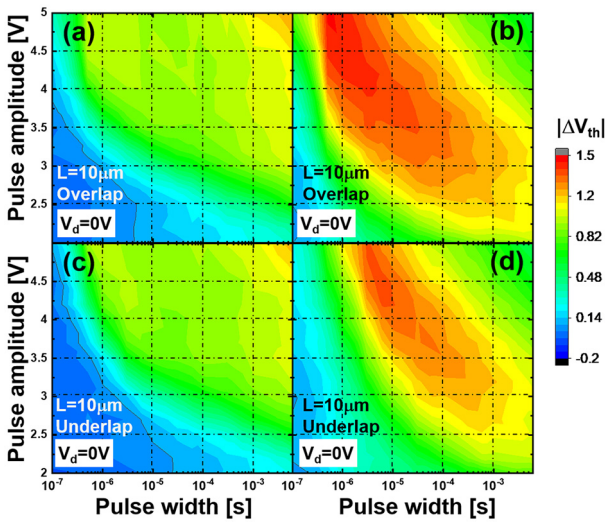

FIGURE 15. **Pulse program/erase characteristics of the overlap and underlap structure (V_d=0V): (a) overlap-program, (b) overlap-erase, (c) underlap-program, (d) underlap-erase.**

layer according to Fig. 11. The erase speed of the overlap device is about 100 ns, which is faster than about 1μs in the underlap device, because larger GIDL current of the overlap device can efficiently supply minority carrier holes in the channel and fix the channel potential instead of the floating body. The erase characteristics is nearly the same in the region of high voltage amplitude and long pulse width. This is because erase operation can utilize thermally generated hole carriers. Please note that our pulse measurement setup allows about 100ns with 10ns resolution, avoiding deformation of the pulse waveform in our measurement range. For

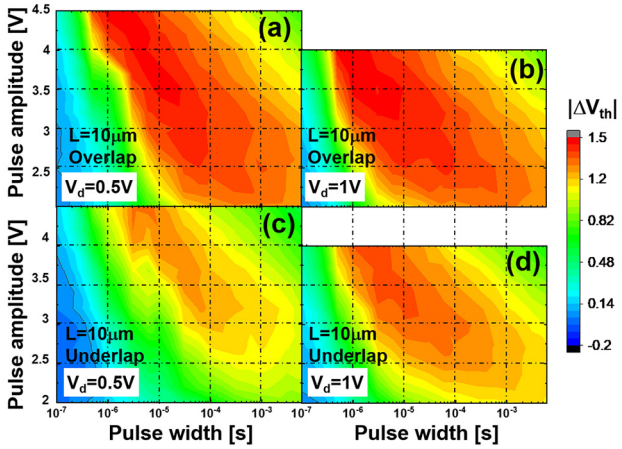

FIGURE 16. **Pulse erase characteristics of (a, b) overlap and (c, d)underlap structures at Vd=0.5V and 1V for erase operation.**

the erase characteristics with high voltage and long width, the ΔV_{th} becomes small which can be partly due to the hole trapping near the interface between Si and the IL [17], [25]. Whereas the program characteristics does not show such behavior because the electron trapping occurs near the border trap between the IL and the HZO layer which compensates and stabilizes the spontaneous polarization charge in our measurement range [16], [17].

Then, V_d is increased up to 1.0V for increasing GIDL current and thus improving erase operation [26]–[27] of the overlap (a) (b) and underlap device (c) (d) as shown in Fig. 16. To protect the gate oxide from breakdown, maximum amplitude is limited to 4.5V and 4V at V_d = 50mV and 1.0V, respectively. At higher V_d, the overlap device shows more efficient erase operation especially at low pulse amplitude (V_g < 3V with MW > 1.2V) in Fig. 16 (a) and (b). Whereas the underlap device does not show improvement except at V_d = 1.0V. At V_d = 1.0V, erase operation becomes slightly faster at lower pulse amplitude even for the underlap device. This is because the electric field from the drain expands under the gate and induces slight GIDL current.

V. RETENTION MODEL WITH NUCLEATION LIMITED SWITCHING

We developed a compact retention model based on the previous understanding of the polarization switching of FE-HfO_2. The model is made from the surface-potential based FET model, the nucleation-limited switching (NLS) model [10]–[13] and the retention model of FE-capacitor [14] as illustrated in Fig. 17. Border traps around FE-HfO_2/SiO_2 interface [15] are introduced as sheet charge (N_T) at the energy level of E_T for simplicity in the compact model. Interface state density is introduced as a constant value of D_{it}. Ferroelectric is modeled by Preisach model [28] for initialization and program/erase operation because of its less computation burden, and modeled by the NLS model for retention state.

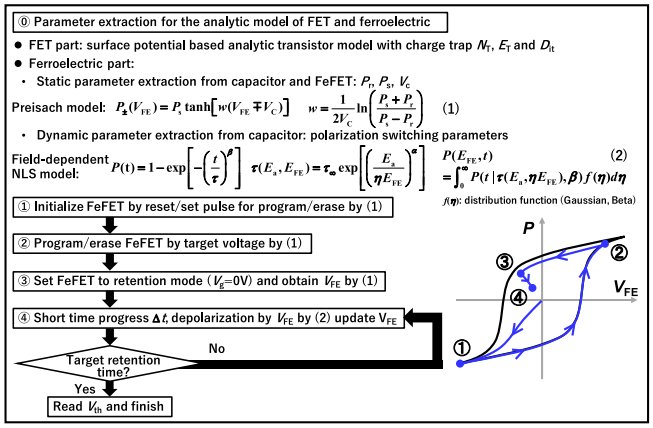

FIGURE 17. Simulation framework of the retention characteristics of a FeFET.

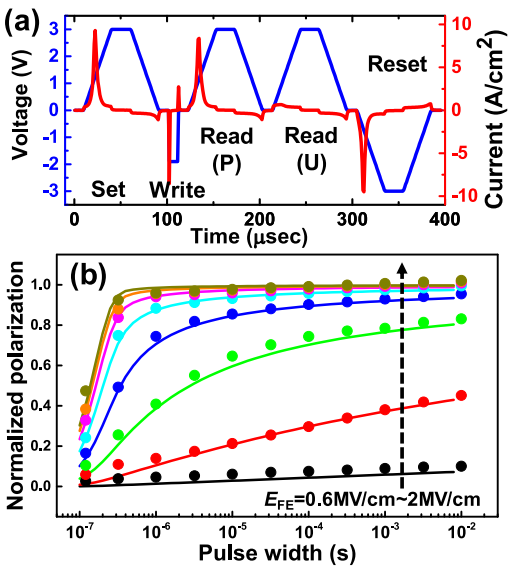

FIGURE 18. (a) Measured waveform of the polarization switching current through a FE-capacitor as well as applied waveform. (b) Measured normalized polarization charge density versus write pulse width as a function of write pulse amplitude.

First, the modeled FeFET is initialized by reset (set) voltage for program (erase) operation. Next, program (erase) voltage is applied at a target value. Then, the FeFET is set to the retention state at $V_g = 0V$. By using the calculated voltage at the ferroelectric (V_{FE}), depolarization takes place based on the NLS model in the short interval time Δt, and V_{FE} is updated. This depolarization step is repeated every time after the interval Δt till the target retention time. Finally, at the target retention time, V_{th} is extracted by sweeping V_g.

E_T was and set to 0.83eV from the Si midgap level by referring to the previous study [15]. N_T was adjusted in the range of $10^{12} \sim 10^{14}cm^{-2}$ by fitting the experimental time-zero V_{th} to the model V_{th}. Preisach model parameters were extracted by P-V measurement of the capacitor. NLS model parameters were extracted by the method in the previous work [12], [13]. Fig. 18 shows the example of the NLS

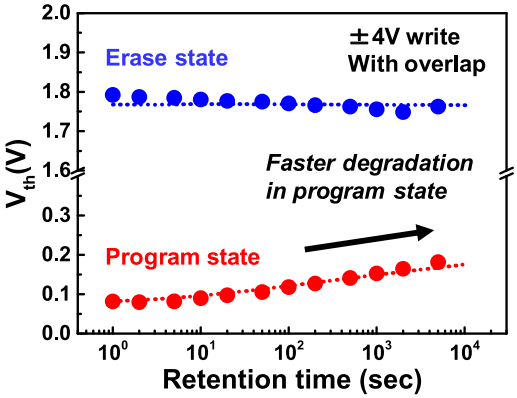

FIGURE 19. Measured retention characteristics of an FeFET with simulated curves by the framework in this work.

model parameter extraction of FE-HfO_2, where the model fits well to the experimental data.

Fig. 19 shows the measured retention characteristics with the proposed model. The Overall trend was qualitatively reproduced by the model. The program state degradation is worse than the erase state. The simulation indicates that this can be due to the detrapped electrons which originally compensate polarization charge during program operation but accelerate polarization reversal in turn during the retention state.

VI. SUMMARY

In this work, we fabricated SOI junctionless FeFETs and investigated the role of GIDL current for erase operation in planar FeFETs to emulate the erase operation in 3D vertical FeFETs by using GIDL. GIDL current can supply minority carrier holes to enable fast erase operation at low voltage. A gate stack with Ti layer insertion was proposed for low voltage operation. Write operation voltage < 2V was achieved with 10nm HZO. Finally, we developed a compact long-term FeFET retention model.

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