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A Study of ESD-mmWave-Switch Co-Design of 28GHz Distributed Travelling Wave Switch in 22nm FDSOI for 5G Systems

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ABSTRACT This paper presents the first co-design analysis of 28GHz broadband single-pole double-throw (SPDT) distributed travelling wave RF switches implemented in a foundry 22nm fully-depleted silicon-on-insulator (FDSOI) CMOS technology, featuring 9KV full-chip human body model (HBM) electrostatic discharge (ESD) protection. This ESD-protected millimeter wave (mmWave) SPDT switch is designed for highly reliable above-6GHz 5th-generation (5G) mobile systems, covering the n257 and n258 bands. Adverse influences of the inherent ESD-induced parasitic effects are characterized, revealing that the ESD effects can severely affect RF switch performance in mmWave bands. A new ESD-mmWave-switch co-design technique was developed to address this ESD design challenge for mmWave switches, which was validated in Si measurements, e.g., improving the switch insertion loss (IL) by ~4dB for the 28GHz SPDT travelling wave switches fabricated. This design also achieves the highest reported charged device model (CDM) ESD protection of ~1.84A in Si testing. This study proves that ESD-mmWave-switch co-design is critical to RF front-end designs for 5G mobile systems, which typically require robust ESD protection, but are also very sensitive to the inevitable ESD-induced parasitic effects.

INDEX TERMS 5G, TRx, switch, SOI, ESD co-design, mmWave, travelling wave.

I. INTRODUCTION

RF switches are indispensable components to RF front-end modules (FEM) and systems-on-chip (SoC) for mobile systems, particularly for complex 5G wireless applications utilizing ultrawide frequency spectrums, large number of dynamic frequency channels, and time division duplexing (TDD) technology across millimeter-wave frequency bands. Meanwhile, full-chip ESD protection is an emerging challenge for mmWave IC designs. Unfortunately, any on-chip ESD protection structures come with inevitable ESD-induced design overhead effects, e.g., parasitic capacitance (C_{ESD}), leakages and noises. Obviously, high-frequency broadband RF ICs are very sensitive to these ESD-induced parasitic effects, which requires careful design considerations [1], [2]. On the other hand, monolithic RF ICs and SoCs for consumer electronics typically require very robust ESD protection, which translates into much more severe ESD-induced parasitic effects that is becoming increasingly unacceptable to high-performance RF ICs for 5G systems [3]–[5]. Substantial R&D efforts have been devoted to RF ESD protection designs, mainly to minimize the ESD-induced parasitic C_{ESD} to reduce the adverse ESD impacts on RF ICs. Consequently, ESD-RFIC co-design becomes an important design technique for modern broadband RF ICs. Recently, [4] reports co-design of ESD protection and SP10T switches for 4G smartphones. Reference [5] discusses co-design of ESD protection and power amplifiers (PA). In mmWave frequency bands, ESD-protected PAs and low noise amplifiers (LNA) were reported, which however did not include ESD co-design considerations [6], [7]. Recently, significant influence of ESD protection on 28/38GHz RF switches for 5G mobiles was reported, showing severe insertion loss degradation of 5~10dB due to 4KV HBM ESD protection, which indicates that conventional RF ESD design techniques are incapable of handling robust ESD protection for millimeter-wave RF

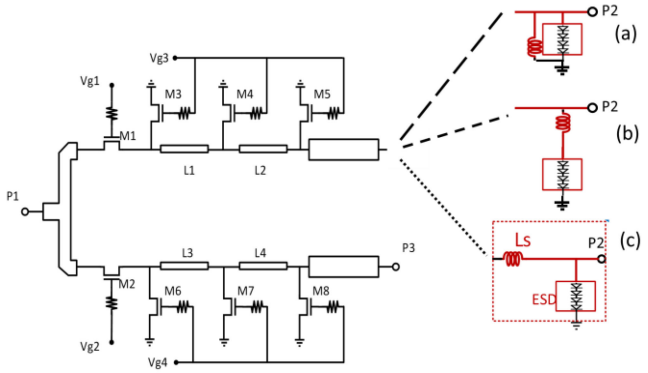

FIGURE 1. **Schematic of the ESD-protected distributed travelling-wave mm-wave SPDT switch featuring: (a) narrow-band LC shunt resonator ESD protection, (b) LC series resonator ESD protection with a center frequency far away from the operating frequency, and (c) L-shape ESD protection.**

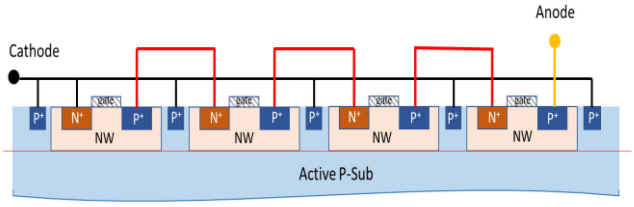

FIGURE 2. **A cross-section view for the gated four-diode-string ESD protection structure designed in this work.**

ICs [8]. It is obvious that ESD-RFIC co-design in mmWave frequency bands, particularly for above-6GHz 5G RF ICs, must be studied comprehensively and understood thoroughly, especially considering both HBM and CDM ESD protection for very high frequency and ultrawide bandwidth RF FEM designs. This paper, an extension to a conference brief [9], presents a comprehensive co-design analysis study of a 9KV-ESD-protected 28GHz distributed travelling wave mmWave SPDT RF switch designed and fabricated in a 22nm FD-SOI technology for 5G systems, aiming to provide a practical ESD-mmWave-switch co-design technique for above-6GHz 5G wireless systems.

II. MMWAVE TRAVELLING-WAVE SWITCH DESIGN

Conventional series-shunt transistor circuit topology offers excellent switch performance for sub-6GHz RF switches. Unfortunately, in the above-6GHz frequency bands, e.g., 28/38GHz, the specifications of series-shunt transistor RF switches suffer severe performance degradation [8]. Several designs were reported to address the mmWave switch design challenges using various design methods, for instance, using a unique SOI substrate featuring very high resistivity and a trap rich layer to alleviate the coupling effect [10], utilizing a special coupling line based artificial resonator structure for sub-terahertz operations [11], [12], and resorting to various MEMS structures and emerging materials [13]–[15]. Alternatively, travelling-wave-based RF switch topology becomes very attractive to ultrawide band millimeter-wave switches [16]–[19].

This work adopts a unique distributed travelling wave switch schematic to design a mmWave SPDT RF switch for 28GHz 5G mobile systems. Fig. 1 depicts the travelling wave mmWave SPDT switch implemented in a foundry 22nm fully-depleted SOI technology. This three-stage distributed travelling wave SPDT structure consists of inductive transmission lines (TL) and the corresponding controlling transistors. This distributed travelling wave SPDT circuit does not use quarter-wave transmission lines in order to reduce the switch die area for high-frequency operations of 28GHz and to avoid using long trace that will increase insertion loss (IL) along the lossy transmission lines. The series transistors (M1, M2) provide extra control of the SPDT switching status and improve its isolation (Iso). For power handling capability consideration, thick-oxide long-channel nMOSFETs are used for both series and shunt transistors (M1-M8). In this design, the on-state resistance (R_{on}) and off-state capacitance (C_{off}) of the unit-width MOSFET were extracted first, which allows to optimize the MOSFET widths jointly with the transmission lines for careful design trade-off. The inductive transmission line was designed to have a characteristic impedance of 70Ω. Generally, a complex massive-MIMO architecture in mmWave 5G systems requires many transmitting/receiving (TRx) switches. Accordingly, this design selects short transmission line segments with smaller inductance to save the SPDT switch die area. Correspondingly, the shunt MOSFETs are designed with smaller sizes to meet impedance requirements. Consequently, the controlling MOSFET sizes are designed as following: channel length L = 100nm for M1-M8, channel width W = 115μm for M1 and M2, and W = 20.3μm for M3-M8, respectively. A 10KΩ resistor is added to the gate to provide AC isolation.

III. FULL-CHIP ESD PROTECTION DESIGN

This 28GHz mm-wave SPDT switch was designed with full-chip 9KV HBM ESD protection. Fig. 2 shows the ESD protection utilizing a four-diode-string ESD protection structure and optimized by TCAD ESD simulation to prevent switch power dropout due to ESD-induced leakage. The gated diodes feature floating gates. The diode-string ESD protection structure is implemented in the "hybrid" region in the FDSOI technology, where the buried oxide isolator layer (BOX) in the SOI substrate was purposely removed in the ESD device layout area to allow direct ESD current discharging through the bulk region, which improves the ESD discharging conduction and heat dissipation via the substrate, and therefore greatly enhances its ESD current handling capability as predicted by TCAD ESD simulation depicted in Fig. 3. Fig. 3a shows the ESD protection diodes produced by TCAD simulation using a representative process, with and without the SOI BOX. Standard HBM zapping waveforms, generated by an HBM ESD equivalent circuit, are used as ESD zapping stimuli for transient TCAD ESD simulation. Figs. 3b/c depict the simulated transient HBM

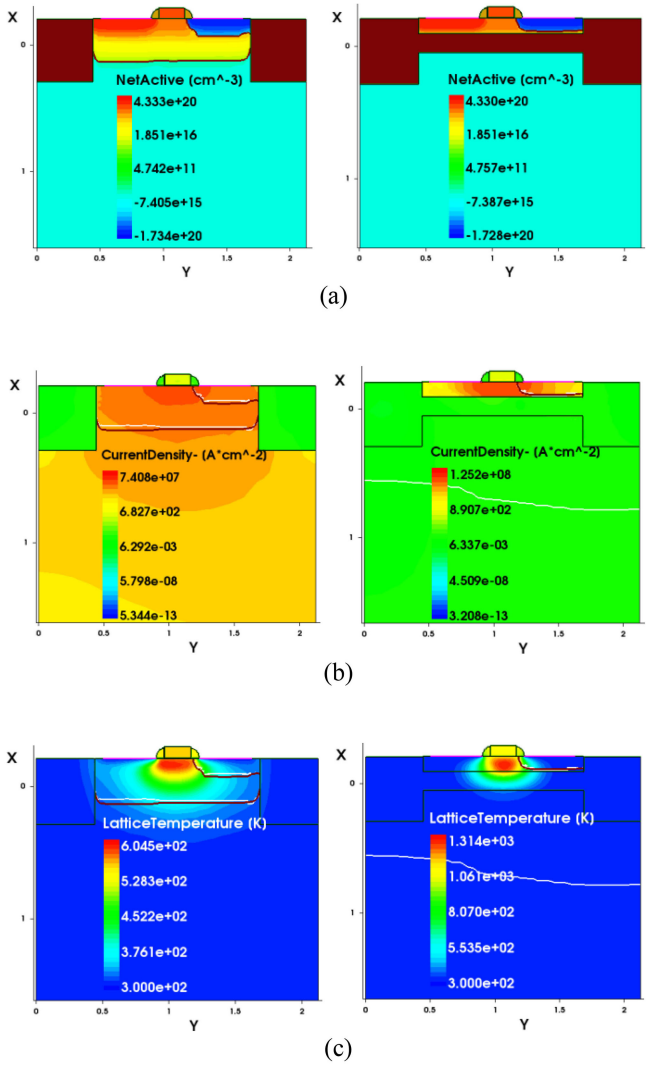

FIGURE 3. **TCAD ESD simulation reveals transient ESD discharging characteristics for the two diode-string ESD protection structures with (Right) and without (Left) a SOI BOX: (a) ESD diode cross-sections, (b) ESD discharging current flows, and (c) transient lattice temperature.**

ESD discharging characteristics for the two ESD protection structure splits (i.e., with and without BOX), respectively, revealing the transient ESD discharging current flows and lattice temperature distribution. It is observed that the ESD protection structure with SOI BOX suffers from higher local overheating compared to its non-BOX counterpart. This is obviously attributed to more severe ESD discharging current crowding and poorer heat dissipation inside the active ESD structure with SOI BOX isolation. TCAD ESD simulation for exemplar ESD diode strings show that the ESD structure with a SOI BOX fails at 1.13KV ($I_{t2} \sim 0.75$A), while the ESD diode without a SOI BOX passes a much higher level of 2.37KV ($I_{t2} \sim 1.56$A). Commonly used ESD protection diodes utilize either gated diode or shallow trench isolation (STI) diode structure. Compared to a STI ESD diode, a gated ESD diode is generally more ESD-robust due to its short and straight ESD discharging conduction path, which

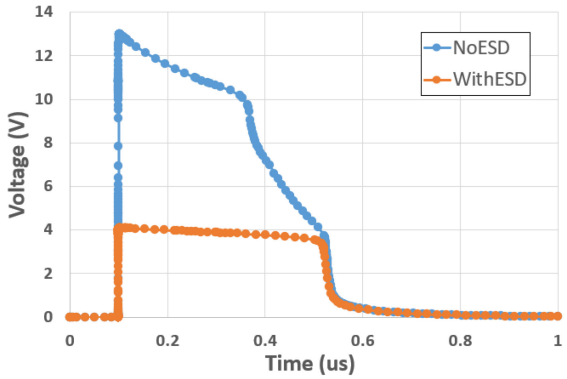

FIGURE 4. **Chip-level transient ESD discharging simulation shows transient voltage at the output nodes of the SPDT design splits without and with ESD protection under 2KV HBM ESD zapping. Without ESD protection, ESD failure occurs to M5 due to high transient voltage of ~13V. With ESD protection, the SPDT is safe due to a low clamping voltage of ~4V.**

results in lower ESD discharging resistance and faster ESD triggering speed [20], [21]. Therefore, this design utilizes gated four-diode-string ESD protection structure as shown in Fig. 2. The gated ESD diode structures were optimized for a gate length of 150nm and a diode width of 500μm for 9KV HBM ESD robustness. The four-diode-string ESD protection structure is designed to feature an ESD triggering voltage of $V_{t1} \sim 2$V and to handle an output power of 19dBm for 5G mobile systems. The ESD-induced parasitic capacitance of the gated four-diode-string is estimated to be $C_{ESD} \sim 50$fF, which is used for ESD-SPDT co-design to be discussed later. Chip-level transient HBM ESD simulation was carried out to evaluate the ESD protection of the 28GHz mmWave SPDT circuit. Fig. 4 depicts the simulated ESD voltage clamping behaviors at the SPDT output ports under exemplar 2KV HBM zapping, which reveals that, without ESD protection, the SPDT suffers high transient voltage stressing of up to 13V at the output node that causes breakdown ESD failure to MOSFET M5 due to very low breakdown voltage of 22nm FDSOI CMOS (BV $\sim$ 8.7V); while the output voltage is effectively clamped to a low level of 4V in the SPDT with ESD protection.

IV. ESD-MMWAVE-SWITCH CO-DESIGN

The conventional shunt L-C resonator ESD protection scheme, shown in Fig. 1(a), is not suitable for broadband RF ICs because the high-Q resonator makes this ESD protection scheme intrinsically be narrow band in nature. Alternatively, [22] reports a series L-C ESD protection topology for mmWave RF ICs as shown in Fig. 1(b), which creates a notch at low frequency and shows less impact to ultra-high frequency circuits. Reference [23] discusses a similar design using transmission lines for the inductors for ultra-high frequency ESD protection. However, this series L-C ESD protection method is not suitable for CDM ESD protection because the series inductor adds significant extra delay in ESD triggering under CDM ESD zapping, hence easily resulting in early CDM ESD failure.

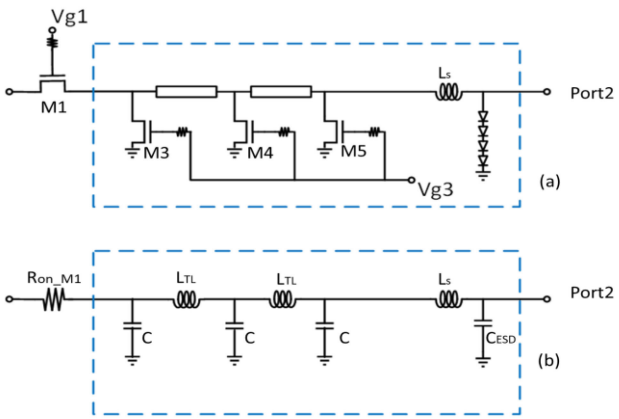

FIGURE 5. Equivalent circuit model for the traveling wave switch with L-shaped ESD protection structure for co-design consideration: (a) schematic of a switch branch circuit with four-diode-string ESD protection, and (b) equivalent circuit model with the ESD protection represented by C_{ESD}.

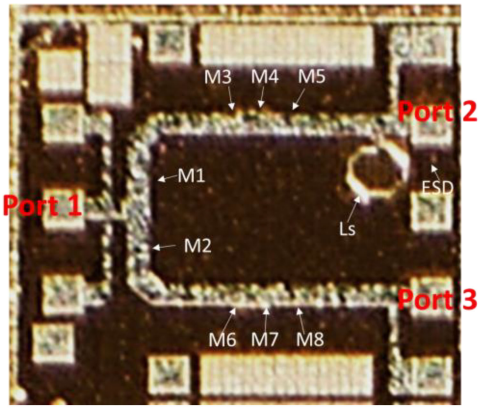

FIGURE 6. Die photo for the ESD-protected 28GHz distributed mm-wave travelling wave SPDT switch fabricated in a foundry 22nm FDSOI CMOS technology.

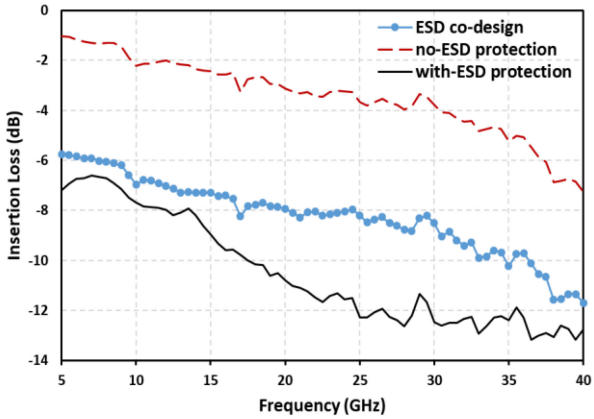

FIGURE 7. Measured IL for the SPDT switch splits: without ESD protection, with ESD protection (but no co-design optimization), and with ESD protection and co-design optimization.

To address this ESD design problem, we devised a novel L-shaped ESD protection topology to simultaneously address both RF impedance mismatching and CDM ESD discharging challenges in mmWave broadband designs as depicted in Fig. 1(c), which provides the desired broadband ESD response without causing circuit performance degradation to mmWave switches. Conceptually, the L-shape ESD matching network consists of the L_S and ESD-induced parasitic capacitance, C_{ESD}. Under CDM ESD stressing, the ESD protection structure forms a low-R_{on} CDM ESD discharging path. This L-shaped ESD protection scheme can instantaneously reduce the harmful high-frequency CDM ESD pulse magnitude and substantially delay the CDM ESD pulse propagation into the internal circuit, hence, providing efficient CDM ESD protection in addition to robust HBM ESD protection. Fig. 5 depicts the equivalent circuit of the L-shape ESD protection network used for ESD-mmWave-switch co-design analysis. In On-state, the travelling wave switch is equivalent to a distributed transmission line network formed by inductors and capacitors [24]. Ignoring the resistive loss, the characteristic impedance of the transmission line network can be expressed,

$$Z_0 = \sqrt{\frac{L_{TL}}{(C_{TL} + C_{FET})}}. \quad (1)$$

By carefully choosing an appropriate inductor value through co-design considerations to set

$$\sqrt{\frac{L_{TL}}{(C_{TL} + C_{FET})}} = \sqrt{\frac{L_s}{C_{ESD}}}, \quad (2)$$

the L-shape ESD protection block can be absorbed as an extra stage of the equivalent transmission line circuit for the ESD-protected travelling wave switch circuit branch. By careful design, the ESD-included characteristic impedance can be precisely set to match the source and load impedance, which leads to a lower VSWR circle, hence less RF signal power loss from mismatch, and eliminates the inherent ESD-induced impacts to the On-state insertion loss. When the travelling wave switch is in Off-state, the turned-off series transistor (M1) and turned-on shunt transistor (M3) will block most RF power. Therefore, the L-shape ESD protection structure will have minimum impact on the isolation. In this design, the L_S is calculated to be 125pH per Eq. (2). Including the parasitic effects of the backend metal lines and device structures, the inductor was optimized by HFSS simulation to have an inductance of 152pH with Q~25 at 28GHz.

V. CHARACTERIZATION AND DISCUSSION

Fabricated in a foundry 22nm FDSOI CMOS technology, the ESD-protected distributed travelling-wave 28GHz SPDT switches were characterized for both RF and ESD protection performance. Fig. 6 shows a die photo for the fabricated 28GHz SPDT mmWave switch optimized by ESD-mmWave co-design. Fig. 7 and Fig. 8 depict the key SPDT switch Specs, insertion loss and isolation respectively,

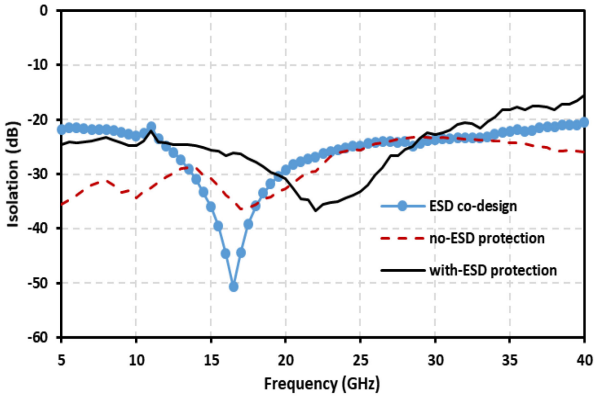

FIGURE 8. Measured Iso for the SPDT switch splits: without ESD protection, with ESD protection (but no co-design optimization), and with ESD protection and co-design optimization.

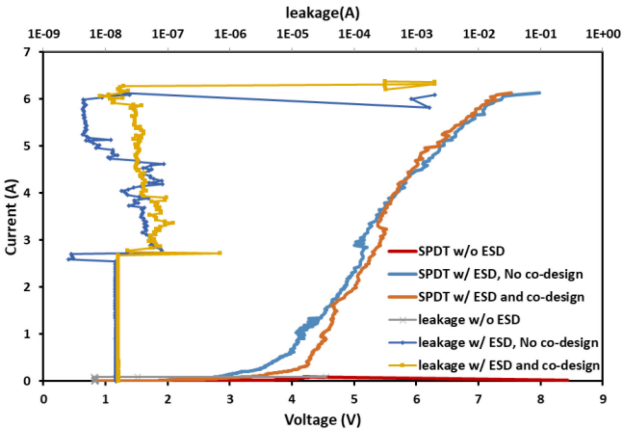

FIGURE 9. Measured HBM ESD protection performance of the mm-wave SPDT switches splits by TLP ESD testing shows that the best reported full-chip HBM ESD protection robustness of at least 9KV in mm-wave bands (linear scale).

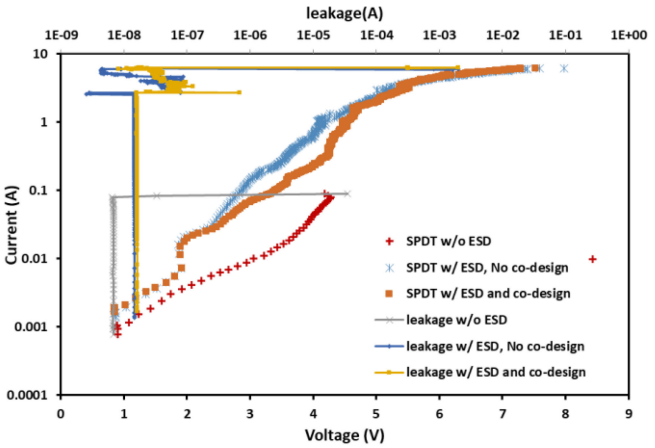

FIGURE 10. Zoom-in for the measured HBM ESD protection performance of the mm-wave SPDT switches reveals the ESD triggering details in log scale.

measured using an RF probe station and Agilent-E8363B PNA Network Analyzer. It is observed that, from 5GHz to 20GHz, the SPDT switch without ESD protection structure achieves IL of 1.0dB ∼ 3.1dB and Iso better than 30dB. Across the 5G n257 and n258 bands required, IL is better than 3.9dB and Iso is better than 23dB. Table-1 compares this work with relative designs reported, showing comparable broadband switch performance in the mmWave bands. Fig. 7 clearly shows the negative impacts of ESD-induced C_{ESD} on mmWave SPDT performance, i.e., a substantial degradation in IL, as much as an increase of ∼12.6dB at 28GHz. By ESD-mmWave co-design, the ESD-induced IL degradation was successfully recovered by ∼4dB across the whole 5-40GHz bandwidth measured. It is worth noting that, though the ESD-switch co-design concept is straightforward, the ESD co-design was not yet able to completely recover all the ESD-induced SPDT performance degradation as expected in this design for the following reasons: Ideally, accurate measurement of Si ESD structures before ESD-switch co-design is needed in order to achieve better results in practice designs, which requires two design iterations, or such ESD testing data must be available to designers when designing an ESD-protected switch. Unfortunately, since this was a design under an MPW tape-out program with limited foundry supports and allowed one Si fabrication opportunity only, this travelling wave switch design could not be carried out following the ideal ESD-mmWave-switch co-design procedures. In addition, the EM simulation parameters, such as materials permittivity, could not be accurately calibrated due to lack of foundry technology data on HFSS simulation models. Nevertheless, this work clearly demonstrates the severe performance impacts of ESD protection on mmWave travelling wave switch circuits and confirms that ESD-mmWave-switch co-design is important, useful and practical to design optimization of RF switches in mmWave bands.

Next, on-chip ESD protection characterization was conducted for both HBM ESD stressing by transient transmission line pulsing (TLP) ESD testing (Barth 4002 TLP+) and CDM ESD stressing by very-fast transmission line pulsing (VFTLP) ESD testing (Barth 4012 VFTLP+). Fig. 9 presents exemplar HBM ESD protection measurement result at P2-to-GND port by TLP ESD stressing for the three SDPT design splits, i.e., without ESD protection, with ESD protection (but no co-design), and with ESD protection and co-design optimization. The TLP testing pulse waveform conditions were set as: rising time t_r = 10ns and duration t_d = 100ns. The measured transient ESD discharging I-V curves shown in Fig. 9 and their zoom-in details depicted in Fig. 10 clearly show that the non-ESD-protected SPDT switch failed at very low ESD current level of I_{t2} ∼ 0.1A (i.e., HBM ESD robustness of ∼150V only). As a comparison, the L-shaped 4-diode-string ESD protection structure can protect the SPDT switch up to I_{t2} ∼ 6A (i.e., at least 9KV for HBM ESD protection), with ESD co-design optimization included. To our best knowledge, this is the highest full-chip ESD protection level reported for mmWave RF switches by measurement. Fig. 11 and Fig. 12 present the

TABLE 1. Comparison of relevant mmWave switch performance.

Refs.	Processes	Freq. (GHz)	Topologies	IL (dB)	Iso (dB)	ESD Protection
[8]	45nm SOI CMOS	26-30	Series-shunt with feed forward capacitor	<10 (8.8) [a]	>15 (19.6) [#]	4KV
[17]	180nm CMOS	DC-50	Travelling wave	<6* (5.0) [#]	>26* (27) [#]	No
[19]	65nm triple-well CMOS	20-80	Travelling wave	<5* (3.0) [#]	>15* (19) [#]	No
[25]	180nm SOI CMOS	DC-40	Series-shunt with matching inductor	<5* (2.3) [#]	>17* (17) [#]	No
This work	**22nm FDSOI**	**5-30**	**Travelling wave without ESD protection**	**<3.9 (3.9) [#]**	**>23 (24) [#]**	**No**
This work	**22nm FDSOI**	**5-30**	**Travelling wave - ESD protection co-design**	**<8.8 (8.8) [#]**	**>22 (25) [#]**	**9KV**

[*] Estimated from the curves. [#] value at 28GHz.

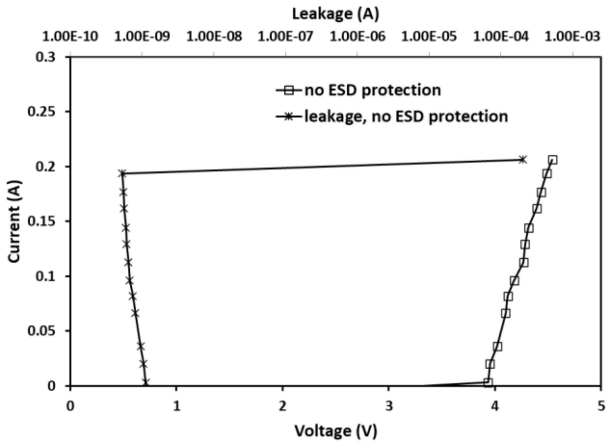

FIGURE 11. Measured CDM ESD protection performance of a sample mm-wave SPDT switch without ESD protection by VFTLP ESD testing shows that the SDPT can be easily damaged by CDM ESD pulses at a low level of ~0.2A only.

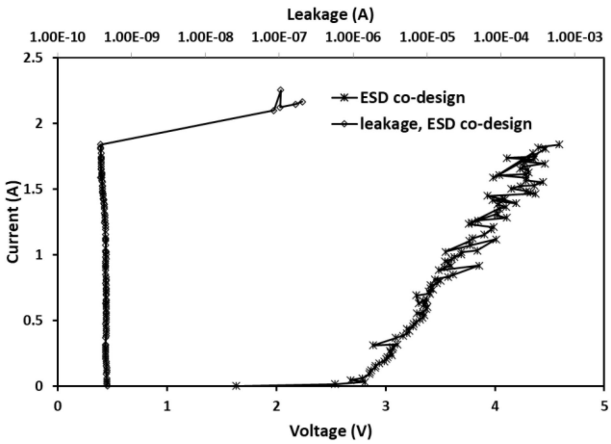

FIGURE 12. VFTLP-measured CDM ESD protection performance of a sample mm-wave SPDT switch with on-chip ESD protection and optimized by ESD-switch co-design shows that the L-shaped ESD protection structure provides very robust CDM ESD protection up to 1.84A.

measured CDM ESD discharging I-V curves by VFTLP testing for the SPDT switches without ESD protection and with ESD protection including ESD-SPDT co-design. The VFTLP testing pulse waveforms were set at t_r = 100ps and t_d = 1ns. Fig. 11 shows that, without on-chip ESD protection, the SPDT switch failed at very low CDM ESD stressing level, i.e., merely ~0.2A. In comparison, Fig. 12 shows that using our novel L-shaped ESD protection structure, the 28GHz SPDT switch passed a very high CDM ESD protection level of ~1.84A. To our best knowledge, this is the best-reported measured CDM ESD protection result for travelling wave RF switches in mmWave bands.

VI. CONCLUSION

This paper reports the first comprehensive ESD-mmWave-switch co-design analysis of mmWave 28GHz travelling wave SPDT switches designed and fabricated in foundry 22nm FDSOI CMOS technology for 5G n257 and n258 bands. The measured IL and Iso are comparable to the state-of-the-art mmWave switches around 28GHz. ESD testing shows that the novel L-shape ESD protection design can absorb the ESD parasitic capacitance into the travelling wave structure and substantially improve the performance of broadband RF switches in mmWave bands. The ESD-co-designed switch achieves the highest reported HBM ESD robustness of 9KV and the best-reported CDM ESD protection level of 1.84A in Si measurements. It is observed that the inevitable ESD-induced parasitic effects can severely affect RF switch performance in mmWave bands, which can be substantially recovered by careful ESD-switch co-design. This study proves that ESD-mmWave-switch co-design is important and useful in optimizing mmWave broadband switch designs for 5G mobile systems, which typically requires robust ESD protection, but is also very sensitive to any inherent ESD-induced parasitic effects.

ACKNOWLEDGMENT

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