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Formation Mechanism of Rounded SiGe-Etch Front in Isotropic SiGe Plasma Etching for Gate-All-Around FETs

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ABSTRACT We investigated the formation mechanism of a rounded silicon-germanium (SiGe)-etch front (rounding) in gate-all-around field-effect transistor (GAA-FET) manufacturing. This rounding is created by the isotropic etching of the SiGe layer after anisotropic etching of the SiGe/Si stack, which degrades device characteristics. The etch-time dependence of the rounding amount during isotropic SiGe etching with nitrogen trifluoride plasma indicates that rounding is mainly formed in an initial stage of SiGe etching, namely, etch time less than 15 s. Cross-sectional scanning transmission electron microscopy and energy dispersive x-ray spectroscopy (STEM EDX) measurement indicated that a Ge-containing layer formed on the sidewall of SiGe/Si patterns before isotropic SiGe etching. From these results, we propose a formation model of SiGe rounding below. The Ge composition in the Ge-containing layer has a gradient due to ion-assisted Ge diffusion during anisotropic etching of the SiGe/Si stack. This gradient induces rounding during isotropic SiGe etching because the etch rate of the SiGe layer decreases as the Ge composition decreases. To validate our model, the Ge-containing layer after anisotropic etching was removed by post-etch treatment and the Ge spectra on the sidewall was reduced to the detection limit of STEM EDX. As a result, the rounding amount after isotropic SiGe etching improved from 2.7 to 1.8 nm. This reduction indicates that the formation of the Ge-containing layer during anisotropic etching of the SiGe/Si stack is one of the main causes of rounding after isotropic SiGe etching.

INDEX TERMS Etch front, GAA-FET, isotropic etch, dry etch, selective SiGe etch.

I. INTRODUCTION

Scaling down a semiconductor device requires continuous improvement of device structures. In logic circuits, field-effect transistors (FETs) are changed from planar FETs to FinFET to overcome short-channel effects [1]–[4]. For scaling of FinFETs, fin height is increased to increase channel width. However, suppression of pattern leaning becomes critical for further height increase [5]. Gate-all-around (GAA) FETs were proposed for beyond FinFETs because they obtain large channel width [6]. For manufacturing GAA-FETs, a new process is required because the structure of GAA-FETs is more complex than that of FinFETs.

One of the key processes in GAA-FET manufacturing is isotropic silicon-germanium (SiGe) etching for inner-spacer formation [7]–[9]. A simplified GAA-FET manufacturing flow is shown in Fig. 1. In step (1), SiGe/Si-stacked layers with a dummy gate are prepared. In step (2), the stacked structure is anisotropically etched to form SiGe/Si patterns. In step (3), selective isotropic etching of SiGe between the Si layers is carried out. After isotropic etching, as shown in step (4), other GAA-FET manufacturing processes including the formation of a low-k inner spacer, source/drain epitaxy, and high-k metal gate, are conducted. In this manufacturing flow, isotropic SiGe etching of step (3) is necessary because it is new for GAA-FETs manufacturing.

There are two requirements for isotropic SiGe etching. One is the selectivity of SiGe to Si for maintaining long Si channel width. The other is a rectangle SiGe-etch front after SiGe etching. When a rounded-SiGe-etch front

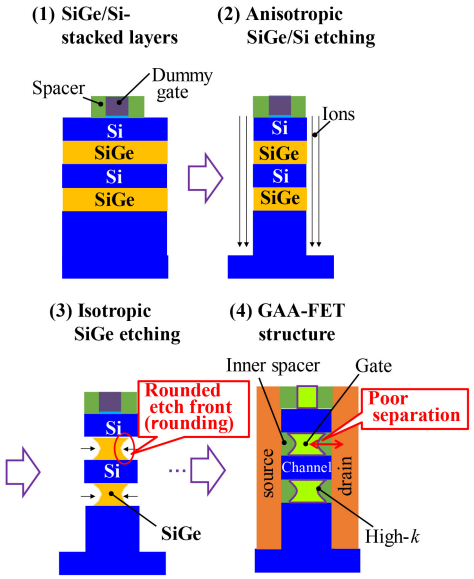

FIGURE 1. Schematic illustrations of GAA-FET manufacturing processes, and rounded-etch-front (rounding) issue in isotropic SiGe etching.

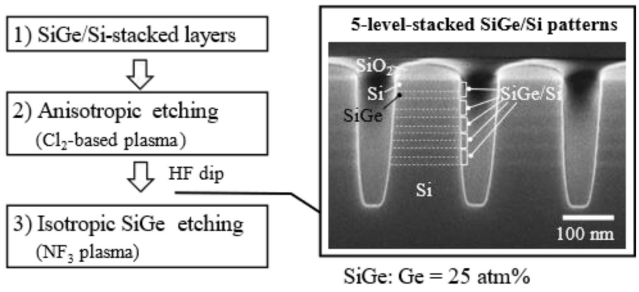

FIGURE 2. Experiment procedure for preparing 5-level-stacked SiGe/Si pattern.

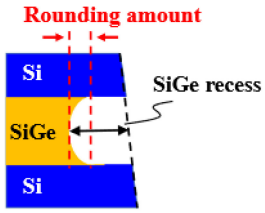

FIGURE 3. SiGe recess and rounding amount.

(rounding) is created, as shown in Fig. 1 (3), the subsequently formed inner spacer also becomes rounded. This rounding degrades device characteristics due to poor physical separation between the gate regions and source/drain epitaxy. For selective SiGe etching to Si, both wet and dry etching have been investigated [8]–[19]. In 2019, Loubet *et al.* reported that dry etching has an advantage on rounding reduction compared with wet etching [8]. However, the formation mechanism of rounding has not been clarified, and understanding this mechanism is important for further rounding reduction.

Given the above background, we investigated the formation mechanism of rounding after isotropic SiGe etching by focusing on dry etching with fluorine-containing plasma, which is a well-known process for SiGe etching [13]–[19]. From the results of this investigation, we propose a formation model that is based on the etch-time dependence of rounding amount in isotropic SiGe etching.

II. EXPERIMENT

The experimental procedure is shown in Fig. 2. First, SiGe/Si-stacked layers were epitaxially grown, and a line and space pattern of a silicon dioxide (SiO_2)-hard mask was created on this SiGe/Si stack. The Ge composition in the SiGe layer was set at 25%. The SiGe/Si stack was then anisotropically etched using chlorine gas (Cl_2)-based plasma with an electron cyclotron resonance plasma (ECR) etcher, and the 5-level-stacked SiGe/Si pattern was created. In anisotropic etching, high-ion energy with wafer-bias power of 450 W was used for obtaining a vertical etching profile. Under this condition, the voltage-peak-to-peak value (V_{pp}) of wafer bias power was over 1000 V. These patterns were then dipped in aqueous hydrogen fluoride (HF dip) to remove the native oxide layer before isotropic SiGe etching. A cross-sectional scanning electron microscopy image of SiGe/Si patterns after HF dip is also shown in Fig. 2. Finally, isotropic SiGe etching was conducted using the ECR etcher without wafer-bias power. In isotropic SiGe etching, nitrogen trifluoride (NF_3) plasma was used because fluorine-containing plasmas are commonly used for isotropic SiGe etching. The formation mechanism of rounding was investigated using the etch-time dependence of the etch profile, which is commonly discussed regarding the etching mechanism [20]–[22]. We used SiGe recess and rounding amount, as defined in Fig. 3, for etch-profile charcterization. The SiGe recess is the lateral distance from the Si-etch front to the SiGe one. The rounding amount is the width of the rounded-etch front. Cross-sectional transmission electron microscopy (TEM) was used to determine the nm-level difference. The average SiGe recess and rounding amount over the five levels (a total of 10-SiGe-etch fronts) were used to decrease measurement variability. Scanning TEM and energy dispersive x-ray spectroscopy (STEM EDX) was also used to investigate the surface composition of the SiGe/Si patterns.

III. RESULTS AND DISCUSSION

Figure 4 shows the cross-sectional TEM images of the SiGe/Si pattern after isotoropec SiGe etching at 60 s. The low-magnification image in Fig. 4 (a) shows that all the SiGe layers of both sides were etched and a total of 10-SiGe-etch fronts were obtained. Figure 4 (b) shows the enlarged image of Fig. 4 (a), showing that the etch front of the SiGe layer was rounded. From the results in Fig. 4, the average SiGe recess and rounding amount were 14.0 and 2.8 nm, respectively.

We next investigated the etch-time dependence of SiGe recess and rounding amount using TEM. Figure 5 shows the results of different etch times from 15 to 120 s. The SiGe

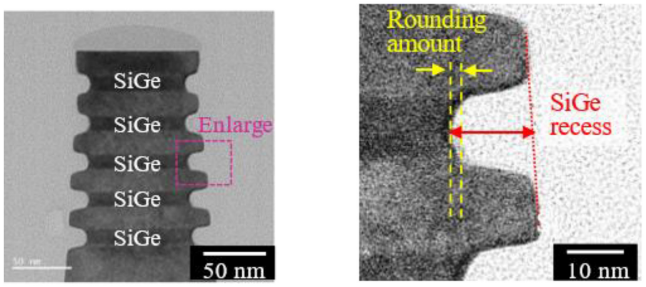

FIGURE 4. Cross-sectional TEM images of SiGe/Si pattern after isotropic SiGe etching at 60 s. (a) and (b) show low and high magnification image, respectively.

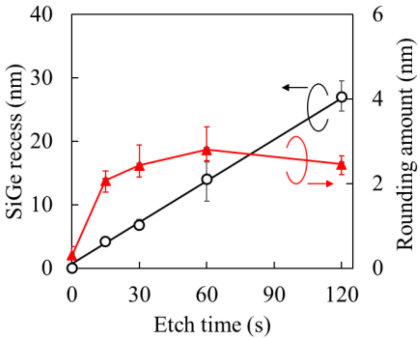

FIGURE 5. Etch-time dependence of SiGe recess and rounding amount during isotropic SiGe etching.

recess increased linearly as time increased. This indicates that the SiGe layer is etched continuously by NF_3 plasma. However, the rounding amount increased as the etch time increased and saturated at about 2.5 nm after 15 s. This indicates that rounding is mainly formed in the initial stage of isotropic SiGe etching, namely etch time less than 15 s. We also changed the isotopic etching conditions, namely, increasing process pressure and increasing wafer temperature, and created a SiGe recess over 20 nm. However, the rounding amount under all etching conditions were within the range from 2.4 to 2.8 nm and remained almost unchanged due to the isotropic etching conditions. Thus, it is concluded that the main cause of rounding is not the actual isotropic etching but the procedure before it.

One possible reason for rounding formation is the variation in the remaining oxide layer after HF dip because the etching durability of oxide is higher than that of SiGe or Si under isotropic etching conditions. Cross-sectional STEM images before and after HF dip are respectively shown in Figs. 6 (a) and (b). In Fig. 6, the hafnium oxide (HfO_2) layer was deposited just before STEM measurement to clear the boundary of the oxide layer. The black layer on the surface of the SiGe/Si patterns in Fig. 6 (a) is native oxide formed by air exposure after anisotropic etching. The results in Fig. 6 (b) indicate that this oxide layer can be mostly removed by HF dip, and variation in the oxide layer is not the reason for rounding after isotropic SiGe etching.

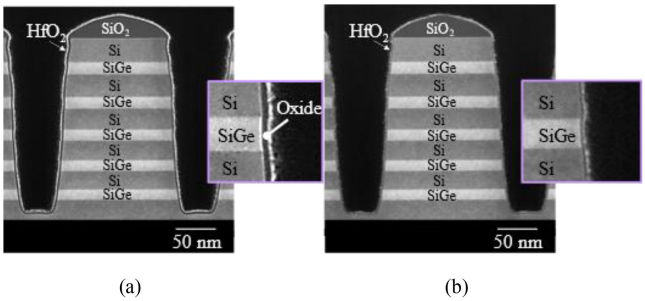

FIGURE 6. Cross-sectional STEM images of SiGe/Si patterns (a) before and (b) after HF dip.

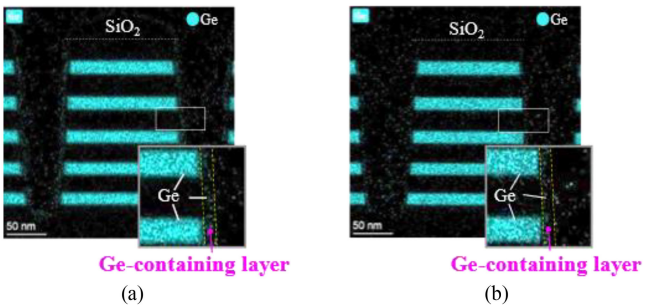

FIGURE 7. Ge composition on cross-sections of SiGe/Si patterns (a) before and (b) after HF dip. Composition is estimated from spectra during STEM EDX.

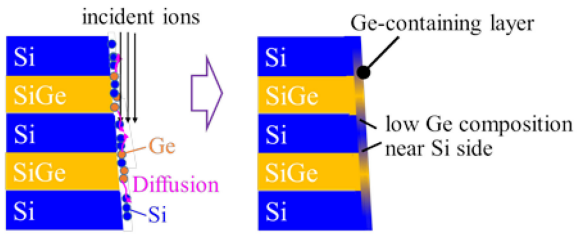

FIGURE 8. Formation mechanism of Ge-containing layer on sidewall of SiGe/Si patterns during anisotropic etching.

To investigate the other reason for rounding, surface composition of SiGe/Si patterns before and after HF dip were analyzed through STEM EDX. Fig. 7 shows the Ge composition from STEM-EDX spectra. We found that Ge exists not only in the SiGe layers but also on the sidewall of Si layers. After HF dip, the Ge amount on the sidewall decreased but could be detected. These results indicate that the Ge-containing layer remained before isotropic SiGe etching.

This Ge-containing layer can form during anisotropic etching using Cl_2-based plasma. It was reported that the surface diffusion of Ge atoms on a Si surface is accelerated by Ar ion bombardment due to the energy transfer from ions to Ge atoms [23], [24]. The diffusion coefficient of Ge increases when the incidence ion energy is more than 15 eV. In our study, the V_{pp} of the wafer bias power during anisotropic SiGe/Si etching was over 1000 V, which is sufficient energy for Ge diffusion. Therefore, the Ge-containing layer could be formed by ion-assisted Ge diffusion, as shown in Fig. 8,

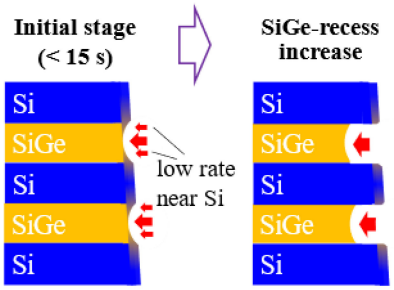

FIGURE 9. Formation mechanism of rounding in initial stage of isotropic SiGe etching.

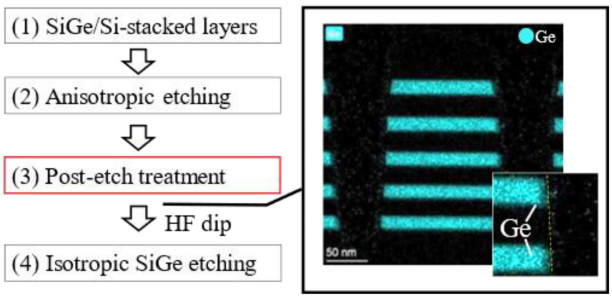

FIGURE 10. Improved process flow and STEM-EDX mapping of SiGe/Si patterns before HF dip.

and the Ge composition of the SiGe layer near the Si layer will be lower than that of before anisotropic etching because Ge atoms are moved from the SiGe surface to Si surface.

The formation of the Ge-containing layer, which has a gradient of Ge composition near the SiGe/Si interface, will induce rounding in the initial stage of isotropic SiGe etching. This mechanism is shown in Fig. 9, which illustrates a sidewall of SiGe/Si patterns during isotropic SiGe etching from the initial stage to SiGe-recess increase. In the initial stage, the Ge-containing layer is etched with fluorine-containing plasma (i.e., NF_3 plasma). It is well known that the SiGe etch rate using fluorine-containing plasma decreases as the Ge composition decreases [13]. Thus the SiGe etch rate near the SiGe/Si interface is lower than that of the center because the Ge composition near the interface is lower than that of the center. This etch rate difference causes rounding on the sidewall of the SiGe layers. After the Ge-containing layer is etched, SiGe etching is carried out and the SiGe recess amount is increased. In this stage, the SiGe etch rate becomes constant from the SiGe/Si interface to center of the SiGe layer because the Ge composition in the SiGe layer becomes constant. Therefore, the rounding amount remains almost unchanged even as the etch time increases. This is consistent with the etch-time dependence of the rounding amount in Fig. 5, where the rounding amount was saturated after SiGe etching at 15 s.

To validate our model, the Ge-containing layer was removed before isotropic etching, and the rounding amount after isotropic SiGe etching was compared between with and without the Ge-containing layer. Figure 10 shows this improved process flow and STEM-EDX image of the

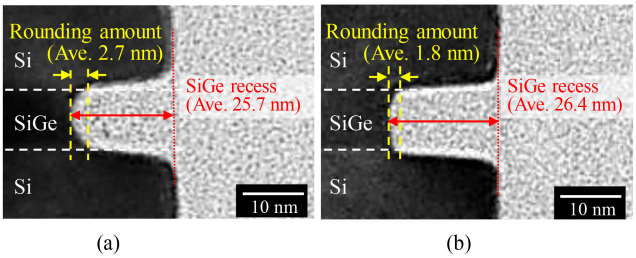

FIGURE 11. Comparison of etch profile after isotropic etching; (a) conventional process flow in Fig. 2 and (b) improved process flow in Fig. 10.

SiGe/Si pattern before HF dip. Post-etch treatment was introduced to prevent the formation of the Ge-containing layer. Comparison of the STEM-EDX images in Fig. 7 (a) and Fig. 10 indicates that the Ge spectra on the sidewall decreased by post-etch treatment and was below the detection limit of STEM EDX. Figure 11 shows the comparison of the etch profile after isotropic etching between the conventional process flow and improved one. The same isotropic SiGe etching condition was used for (a) and (b), but this condition was different from that used in Figs. 4 to 7. The average SiGe recess and rounding amount are also shown in the figure. These results clearly indicate that the improved process enabled the reducing in the rounding amount from 2.7 to 1.8 nm while the recess amounts were almost the same, i.e., around 26 nm. This reduction clearly indicates that the formation of the Ge-containing layer during anisotropic etching of the SiGe/Si stack is one of the main causes of rounding after isotropic SiGe etching.

As shown in Fig. 11, rounding amount at 1.8 nm remained; thus, further improvements are necessary. However, the formation mechanism of this rounding has not been clarified. One of the reasons for this rounding may be a small Ge-containing layer still remaining, which cannot be detected by STEM EDX, inducing rounding. Detailed analysis of the relationship between the surface condition and rounding formation is for future study.

IV. CONCLUSION

We investigated the mechanism of rounding formation after isotropic SiGe etching for GAA-FET manufacturing. We found that rounding in SiGe/Si patterns was mainly formed in the initial stage of the isotropic SiGe etching. STEM-EDX measurement revealed that, before isotropic SiGe etching, a Ge-containing layer was formed on the sidewall of SiGe/Si patterns. From these results, we proposed a formation model in which Ge composition in this Ge-containing layer had a gradient before isotropic etching and the difference in the SiGe etching rate by the Ge composition induces rounding. To validate our model, the Ge-containing layer was removed before isotropic etching. As a result, the rounding amount was reduced from 2.7 to 1.8 nm. This reduction indicates that the formation of the Ge-containing layer before isotropic etching is one of the main causes of rounding formation after isotropic SiGe etching.

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