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Hot-Carrier-Induced Reliability for Lateral DMOS Transistors With Split-STI Structures

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ABSTRACT In this work, four kinds of lateral double-diffused MOS (LDMOS) devices with different split shallow trench isolation (STI) structures (Device A: LDMOS with traditional split-STI, Device B: LDMOS with slope-STI, Device C with step-STI and Device D with H-shape-STI) have been fabricated and the hot-carrier reliabilities also have been investigated due to the serious environment they are endured. The maximum bulk current (I_{bmax}) stress and the maximum gate voltage (V_{gmax}) stress have been carried out and the inner mechanism of device degradation have been investigated successfully. With the assistance of the T-CAD simulation tools, it is found that the main damage point locates at the STI conners with a mount of interface states generation, inducing serious degradation for these four devices. The Device D owns high hot-carrier reliability due to its special structure with narrow split-STI. The worst device is Device C because of the presence of extra STI damage point. Finally, a mechanism verification, the charge pumping (CP) method has been applied to better understand this work.

INDEX TERMS Split-STI, LDMOS, hot-carrier reliability.

I. INTRODUCTION

Lateral double-diffused MOS (LDMOS) is usually applied in the integrated power circuits due to its high off-state breakdown voltage (BV_{off}), low special resistance ($R_{on,sp}$) and easy integration. With the development of integration process, the shallow trench isolation (STI) technology occurs and often applies in the LDMOS design. Based on the dielectric reduced surface electric field (RESURF) theory, the STI LDMOS owns better balance between the BV_{off} and $R_{on,sp}$ [1], [2]. In recent years, some approaches have been studied to improve the balance of BV_{off} and $R_{on,sp}$ of the STI LDMOS. For example, a special change applying on the STI profile can effectively reduce the $R_{on,sp}$ by decreasing the current block effect of STI [3], or splits the gate to realize higher BV_{off} by decreasing the electric field at STI corners [4]. However, the above approaches only do a little adjustment for the device structure, so the performance optimization is limited. To solve it, the split-STI LDMOS with split STI structure in the drift region has been proposed, which can exhibit ultra-low special resistance ($R_{on,sp}$), especially for the H-shape-STI structure [5]–[7].

Generally, the split-STI LDMOS is used as an output device such as display drivers, DC-DC converts and power managements, operating in high electric field and large current conditions [8]–[10]. In this way, the hot-carrier reliability is inevitably affected and even pull down the entire circuit performance. In some papers, the hot-carrier reliability of conventional split-STI LDMOS has been studied while other layouts are less reported [11]–[13]. Though the relative study has been investigated by our work [14], but it only focusses on the hot-carrier induced degradation under the I_{bmax} stress condition that is not comprehensive.

In this work, four devices with split-STI layout patterns have been fabricated to make better balance between BV_{off} and $R_{on,sp}$. Thanks to the breakdown point at the poly-gate plate edge of traditional split-STI device, changing the STI shape near the drain can be carried out to obtain lower $R_{on,sp}$ while maintains constant BV_{off}. Moreover, the hot-carrier

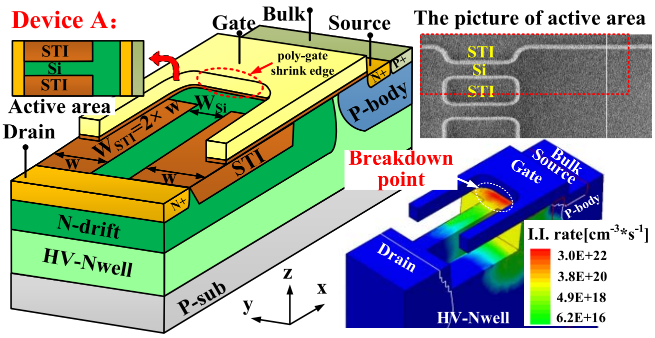

FIGURE 1. Schematic of conventional split-STI LDMOS (Device A) and 3D impact ionization rate (I.I. rate) distribution when off-state breakdown occurs.

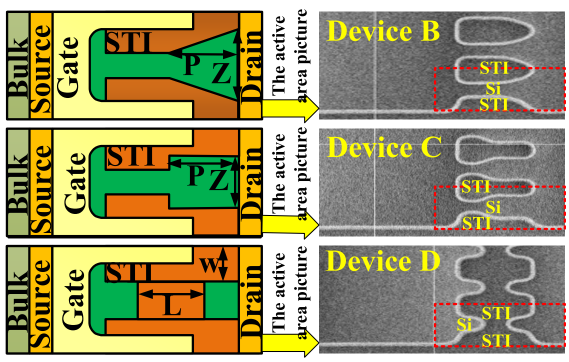

FIGURE 2. Top views and the active pictures of the three different STI layout patterns (Device B: slope-STI, Device C: step-STI and Device D: H-shape-STI).

TABLE 1. Main structure parameters for four devices.

Structure parameters /um \ Device Types	STI width (W_{STI})	Silicon width (W_{si})	Silicon width 1 (Z)	Adjusted STI length(P)	Small STI length (L)
A	0.8	0.2	N/A	N/A	N/A
B	0.8	0.2	0.6	0.5	N/A
C	0.8	0.2	0.6	0.5	N/A
D	0.6	0.4	N/A	N/A	0.4

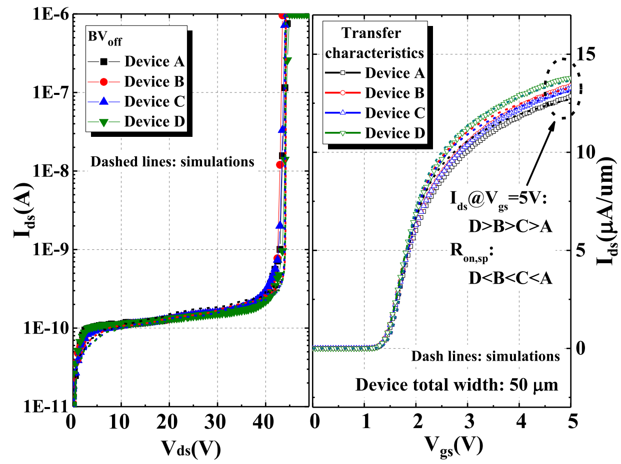

FIGURE 3. Measured and simulated off-state breakdown voltage (@V_{gs} = 0V) and transfer characteristics curves (@V_{gs} = 5V&V_{ds} = 0.1V) of Device A, B, C and D.

reliabilities of the four devices are also considered due to the serious conditions they operated. In our previous work, the hot-carrier reliabilities of the LDMOS with different split-STI structures have been studied by the calibrated T-CAD simulator [15]. To make a further comprehensive study of the hot-carrier reliabilities for the four devices, the CP method has been applied to verify the analyzed inner mechanisms by T-CAD simulator.

II. DEVICE STRUCTURE AND PARAMETERS

Fig. 1 shows the schematic of traditional split-STI LDMOS (Device A) and its 3D impact ionization rate (I.I. rate) distribution when the off-state breakdown occurs. The breakdown point of this device appears at the poly-gate plate edge. Thereby, it is feasible to realize a lower $R_{on,sp}$ by changing the structure of drain side while maintains constant BV_{off}. Based on this, three devices with different STI structures at drain side have been designed in this work (seen in Fig. 2 and Table 1). The split-STI at drain side of Device B and Device C have been narrowed with an slope STI and step STI, respectively, owning broden current path. The width of split STI of Device D is totaly narrowed to broden current path, meanwhile, the small STI is added with proper size to maintain BV_{off} without blocking current.

Fig. 3 shows the measured BV_{off} and transfer characteristics curves of four devices. It shows that the BV_{off} of these four devices is almost same, according with the former opinion. The trend of $R_{on,sp}$ (extracted @V_{gs} = 5V&V_{ds} = 0.1V) presents decreased tendency which is in order of Device A, C, B and D, indicating the realized lower $R_{on,sp}$. Furthermore, the simulated curves are also shown in Fig. 3. It demonstrates that the simulated results are in commodity with the measured data by the calibrated T-CAD simulation tools. The used simulation tools are included in the simulator Sentaurus from Synopsys. The device structure is built by the Tsuprem-4 and Sentaurus Structure Editor according to the real process flow. Then, the device electrical characteristics are simulated by the Sentaurus Device with Bandgap model including Slotboom, Mobility model including DopingDependence, Enormal, Phumob model and HighFieldsaturation, Recombination model including Shockley-Read-Hall, Auger and Avalanche.

III. EXPERIMENTS AND DISCUSSIONS

Because of the same BV_{off} for these four devices, the hot-carrier stress can be carried out successfully. The applied stress condition for drain contact sets about 1.1 times of operation voltage. For the gate contact, two stress conditions have been applied which is the maximum bulk current stress condition and the maximum operation gate voltage condition. In addition, the applied stress can be selectively interrupted to monitor the electrical characteristics such as R_{on} and V_{th}. The inner mechanism of the hot-carrier induced degradation of these two stresses for four devices will be

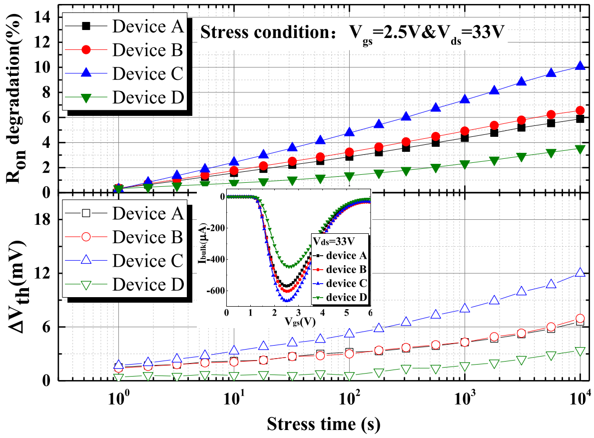

FIGURE 4. R_{on} degradations and Vth shifts of Device A, B, C and D under the I_{bmax} stress condition; Embedded figure: the measured bulk current curves of Device A, B, C and D when $V_{ds} = 33V$.

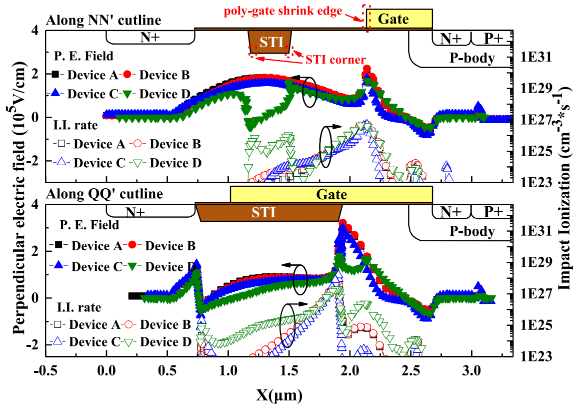

FIGURE 6. Top: the perpendicular electric field and I.I. rate distributions of Device A, B, C and D along NN′ cutline (@Y = 0.5um) under the I_{bmax} stress condition. Bottom: The perpendicular electric field and I.I. rate distributions of Device A, B, C and D along QQ′ cutline (@Y = 0.8um) under the I_{bmax} stress condition.

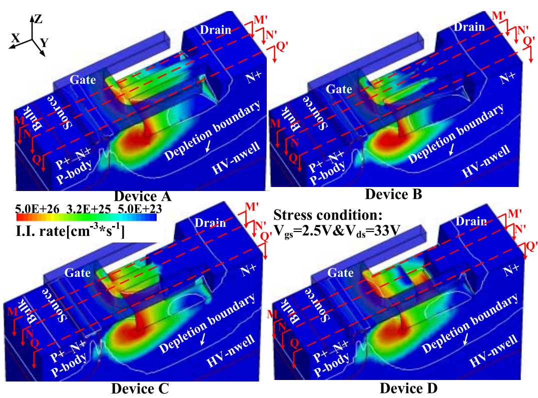

FIGURE 5. Whole 3D I.I. rate distributions of Device A, B, C and D under the I_{bmax} stress condition.

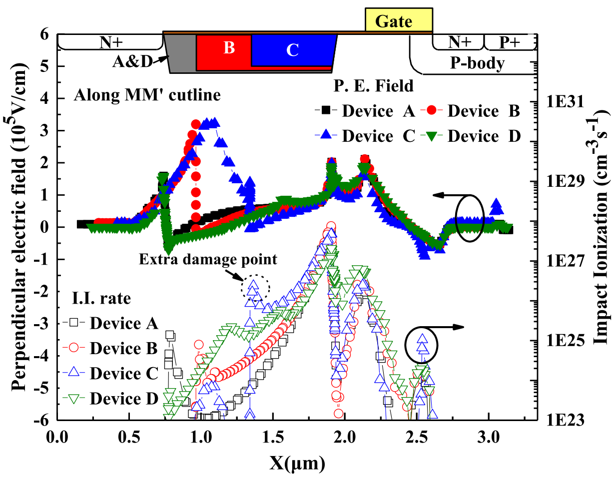

FIGURE 7. The perpendicular electric field and I.I. rate distributions of Device A, B, C and D along MM′ cutline (@Y=0.3um) under the I_{bmax} stress condition.

studied separately in two sections. The further verification of the analysis will be demonstrated through charge pumping method in last section.

A. MAXIMUM BULK CURRENT CONDITION

Fig. 4 shows R_{on} degradations and V_{th} shifts of four devices under the I_{bmax} stress condition. The maximum bulk current occurs in 2.5V for gate voltage, so the I_{bmax} stress sets in $V_{gs} = 2.5V$ and $V_{ds} = 33V$. For the I_{bmax} stress condition, the V_{th} is not degraded due to the small shifts less than 12mV. The R_{on} degradation tendency of all devices are increased monotonously and the degree of degradation serious in order of Device D, A/B and C.

In order to reveal the inner mechanism of the R_{on} degradation, the whole 3D I.I rate distributions of the four devices are shown in Fig. 5. The main impact ionization rate (I.I. rate) peaks occur in the poly-gate shrink edge and the STI corner near the source. To make the discussion more exact, the interface I.I. rate and perpendicular electric field along NN' and QQ' cutlines in Fig. 5 have been shown in Fig. 6. It can be found that the high positive perpendicular electric field (the direction is pointing to surface) at the ploy-gate shrink edge and the STI conners leads to the hot holes injection and interface states generation into the oxide of these two regions [16], [17]. Referring to R_{on} degradation trend in Fig. 4, the interface states generation is the dominated damage mechanism especially in the STI corners due to a serious I.I. rate and higher perpendicular electric field. In this way, the smallest R_{on} degradation appearing in Device D is benefited from the narrower STI width and weaker I.I. rate at the small STI corners. For the Device C, Fig. 7 indicates that an extra I.I. rate peak at the additional STI corners is responsible for Device C with worst R_{on} degradation comparing to Device A and B. In addition, the channel region is intact without any hot-carrier effect, that is why the V_{th} is almost constant.

B. MAXIMUM OPERATION GATE VOLTAGE CONDITION

For the V_{gmax} stress condition, the R_{on} degradation of four devices also increase as stress time rising and the degree of

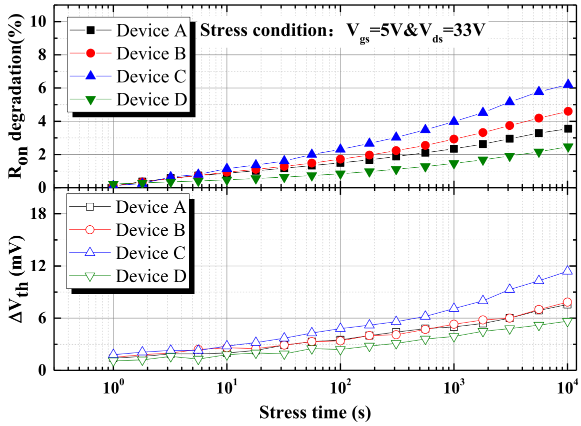

FIGURE 8. R_{on} degradations and V_{th} shifts of Device A, B, C and D under the V_{gmax} stress condition.

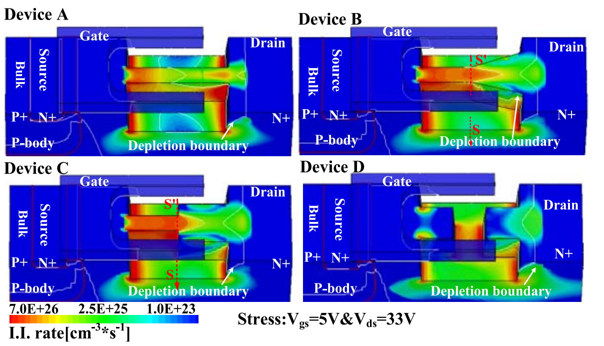

FIGURE 9. Whole 3D I.I. rate distributions of Device A, B, C and D under the V_{gmax} stress condition.

degradation serious is in order of Device D, A, B and C, which is shown in Fig. 8. Similarly, Fig. 9 indicates that the high I.I. rate regions of four devices occurs at the split-STI corners, which can generate amount of interface states to increase R_{on}. The Device D has a smallest R_{on} degradation due to the same reason as in the I_{bmax} stress.

Fig. 10 shows that smaller depletion region of surface silicon near the drain side can obtain longer surface current path, meaning that Device B and C will generate more interface states along the silicon surface that than Device A and D, and leads to serious R_{on} degradations of them. Similarly, the extra damage point of Device C is the reason for terrible R_{on} degradation comparing to Device B, as indicated in Fig. 11. Moreover, the R_{on} degradations of these devices under the V_{gmax} stress are weaker than that under the I_{bmax} stress due to the lower whole I.I. rate. Consequently, the hot-carrier reliabilities of four LDMOS devices with different split-STI structures are in order of Device D, A, B and C under the V_{gmax} stress condition.

C. MECHANISM VERIFICATION BY CHARGE PUMPING METHOD

In this paper, the degradation mechanisms of the four devices with different layouts have been discussed already

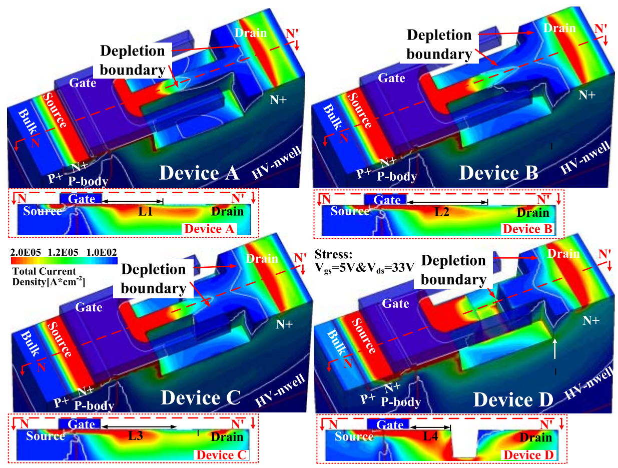

FIGURE 10. Whole 3D total current density distributions of Device A, B, C, and D under the V_{gmax} stress condition. Bottom right: The 2D total current density distributions of Device A, B, C and D along NN′ cutline under the V_{gmax} stress condition (L1 = 0.87μm, L2 = 1.15μm, L3 = 1.10μm, L4 = 0.56um).

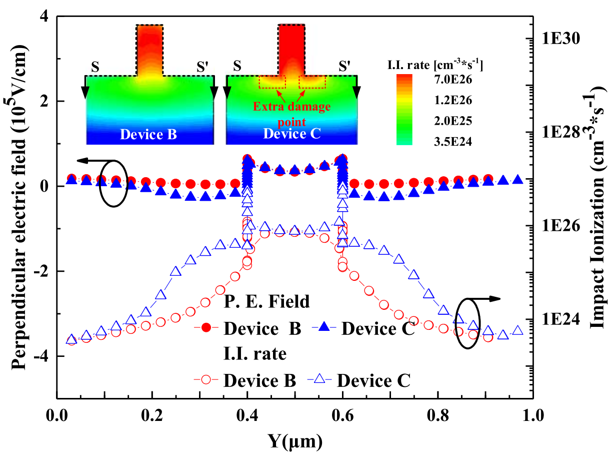

FIGURE 11. The 2D I.I. rate distributions, the perpendicular electric field and I.I. rate distributions of Device B and C along SS′ cutline (@X = 1.34um) under the V_{gmax} stress condition.

in the former two sections. In order to further verify the revealed degradation mechanisms, the CP experiments are performed [18], [19]. For the purpose of getting proper CP conditions, the gate voltage that inducing 1E14cm^{-3} electrons (V_{ge}) and 1E14cm^{-3} holes (V_{gh}) along the SiO_2/Si interface have been extracted by T-CAD simulation, as shown in Fig. 12. Both V_{ge} and V_{gh} present a negative shift from channel region to STI region because of the doping distribution. Furthermore, the V_{ge} and V_{gh} in STI region are below −20V, which exceeds the breakdown voltage of the gate oxide. Thus, the hot-carrier induced damage at the STI corners can not be measured by CP experiment.

To better reflect the real degradation mechanism, the CP experiment is carried out after the R_{on} and V_{th} monitoring. The CP current (I_{cp}) is monitored from the bulk contact to analyze the hot-carriers induced traps and the interface states

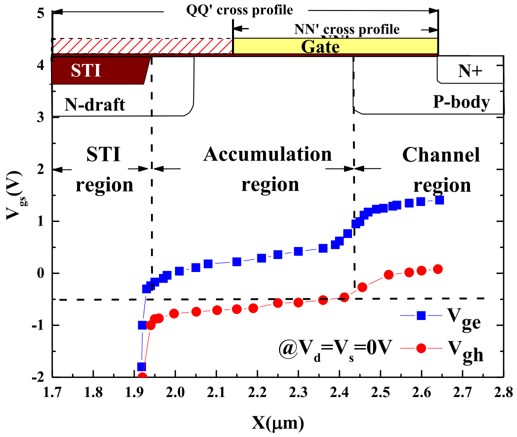

FIGURE 12. Simulated V_{ge} (@electrons = 1E14cm^{-3}) and V_{gh} (@holes = 1E14cm^{-3}) as functions of the lateral distance for device A, B, C and D.

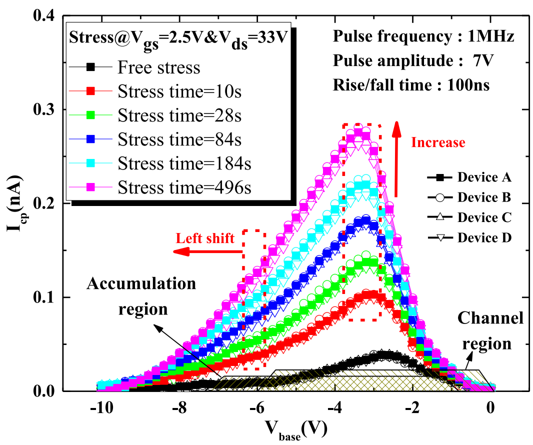

FIGURE 13. Measured CP curves for the Device A, B, C and D under the I_{bmax} stress condition.

generations. For the four devices, the CP measurements are operated with 7V gate pulse amplitude and 1MHz frequency, with the base voltage (V_{base}) of the pulse being varied from −10V to 0V. In theory, the condition for observing I_{cp} is that the region operates from inversion to accumulation [20]. Therefore, combining the gate voltage amplitude and the simulated V_{ge} and V_{gh}, the V_{base} of accumulation region is defined from −7.5V (the lowest V_{ge} of the accumulation region minus the gate pulse amplitude) to −0.4V (the highest V_{gh} of the accumulation region) and the V_{base} of channel region is defined from −6V (the lowest V_{ge} of the channel region minus the gate pulse amplitude) to 0V (the highest V_{gh} of the channel region).

For the I_{bmax} stress condition, the CP measurements are shown in Fig. 13. It is found that the peak of I_{cp} is increased during the stress time, indicating that the number of the generated interface states are increased in the accumulation region. Moreover, the I_{cp} curves shift left as the stress time increased, verifying that the hot holes are injected at accumulation region [21], [22]. Therefore, the above CP experiments

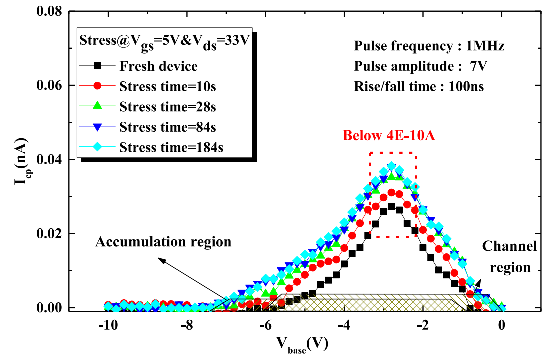

FIGURE 14. Measured CP curves for the device A under the V_{gmax} stress condition.

TABLE 2. Electrical characteristics and hot-carrier reliabilities for four devices.

Critical parameters \ Device Types	A	B	C	D
Electrical parameters				
BV_{off}/V	43.1	43.0	43.0	43.3
$R_{on,sp}$/mΩ·mm^2	21.4	20.9	20.6	20.3
Hot-carrier reliabilities				
Maximum degradation (R_{on})@I_{bmax}=1e^{4}s/%&V_{ds}=33V	5.8	6.5	10	3.5
Maximum degradation (R_{on})@V_{gmax}=1e^{4}s/%&V_{ds}=33V	3.5	4.6	6.2	2.5

further verify the analyses of R_{on} degradation mechanisms in Section III-A. In addition, the measured I_{cp} of the four devices is almost same due to the same structure with similar I.I. rate and perpendicular electric field at the poly-gate shrink edge.

For the V_{gmax} stress condition, the CP measurements of Device A are shown in Fig. 14. Obviously, the value of I_{cp} is very small at both accumulation region and channel region that can be omitted. It indicates that these regions are intact, coinciding with the discussions in section III-B. The CP measurements of other devices do not present in this figure due to the same experiment data.

To make full scene of them, the comprehensive performances and hot-carrier reliabilities comparisons between these devices have been listed in Table 2.

IV. CONCLUSION

In this paper, the hot-carrier-induced degradation of LDMOS with different split-STI structures under the I_{bmax} stress and V_{gmax} stress conditions have been investigated. For the I_{bmax} stress, the interface states generation in the STI corners is the main reason for the R_{on} degradation of four devices. Because of different shapes in the STI corner, the R_{on} degradation degree is in order of device C, A/B and D. For the V_{gmax} stress. The interface states generation in the STI corners still does the main reason for the R_{on} degradation for Device A, B, C and D. The interface states generation in the silicon surface at the drift region causes more R_{on} degradation for the device B and device C, comparing to device A and D. In addition, the serious R_{on} degradation for Device C is induced by its extra damage point in STI corner. Then, the measured CP current curves are further demonstrating the discussed inner mechanisms of R_{on} degradaion under the I_{bmax} stress and the V_{gmax} stress conditions. Consequently, the Device D is the optimum proposal in applied circuit because of its better electrical performance and high hot-carrier reliabilities.

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