Received 12 October 2021; revised 18 October 2021; accepted 2 November 2021. Date of publication 8 November 2021; date of current version 12 November 2021. The review of this article was arranged by Editor C. C. McAndrew.

Digital Object Identifier 10.1109/JEDS.2021.3125742

Figures-of-Merit of Lateral GaN Power Devices: Modeling and Comparison of HEMTs and PSJs

LUCA NELA, CATHERINE ERINE (Graduate Student Member, IEEE), MARIA VITTORIA OROPALLO, AND ELISON MATIOLI (Member, IEEE)

Power and Wide-Band-Gap Electronics Research Laboratory (POWERLAB), École Polytechnique Fédérale de Lausanne, CH-1015 Lausanne, Switzerland

CORRESPONDING AUTHOR: L. NELA (e-mail: luca.nela@epfl.ch)

This work was supported in part by the Swiss National Science Foundation through the Assistant Professor (AP) Energy under Grant PYAPP2_166901, and in part by the ECSEL Joint Undertaking (JU) under Grant 826392. The JU receives support from the European Union's Horizon 2020 Research and Innovation Program and Austria, Belgium, Germany, Italy, Norway, Slovakia, Spain, Sweden, and Switzerland.

ABSTRACT In this work, we propose a simple and yet accurate physical model to describe the figures-of-merit (FOMs) of lateral GaN power devices. While the performance limit of vertical devices is well understood, the FOMs of lateral devices are not properly described by current models. This work investigates the specific characteristics of the depletion in lateral devices, particularly focusing on the substantial potential of Polarization Super Junctions (PSJs) compared to conventional High-Electron-Mobility Transistors (HEMTs). Our results show that PSJs can result in more than a 10-fold decrease in specific on-resistance for the same breakdown voltage compared to HEMTs, which can be further improved by the use of multi-channel heterostructures. In addition, we demonstrate that PSJs lead to a significant reduction of the $R_{ON} \times E_{\text{oss}}$ figure-of-merit, both in the case of negligible and dominating parasitic contributions. This model enables a proper evaluation of the main figures-of-merit of lateral GaN power devices and shows the potential of PSJs to reduce both the DC and switching losses in power devices.

INDEX TERMS Gallium Nitride, polarization super junction, HEMT, off-state modeling.

I. INTRODUCTION

GaN-on-Si lateral devices have shown outstanding potential for power conversion applications and a substantial improvement in their performance has been achieved in recent years [1], [2]. Yet, the performance of current GaN High-Electron-Mobility Transistors (HEMTs) is still far below what is thought to be the limit for such devices [3]. In particular, their lateral architecture combined with the large density of the two-dimensional electron gas (2DEG) results in a peaked off-state electric field at the gate edge, which severely reduces the maximum achievable breakdown voltage (V_{BR}). To address this limitation, polarization super junctions (PSJs) have been proposed [4]–[9], which take advantage of the polarization fields naturally formed in GaN heterostructures to achieve charge balance. This approach enables to overcome the challenging GaN *p*-doping, which is necessary to achieve charge matching in conventional doping-based super junctions, by relying instead on polarization charges to induce a two-dimensional hole gas (2DHG). In PSJ devices, the charge compensation between electrons in the 2DEG and holes in the 2DHG (Fig. 1) results in an overall neutral drift region and thus in a flat off-state electric field profile.

Although PSJ devices have been experimentally demonstrated [10]–[14] and a flat electric field profile intuitively results in improved blocking capabilities, a quantitative analysis of the performance improvement enabled by PSJs with respect to conventional HEMTs is lacking, with current comparisons limited to the case of uniformly doped power devices [4]. This is due to two main reasons. On the one hand, while the on-resistance versus V_{BR} material limit is often used to show the potential of GaN compared to Si or SiC, such an approach cannot be used to accurately compare GaN HEMT and PSJ devices. In particular, while a uniform off-state field profile is typically assumed to extract the material limit [3], this assumption is not valid for HEMTs which, similarly to doped devices, present fixed

 JOURNAL OF THE ELECTRON DEVICES SOCIETY

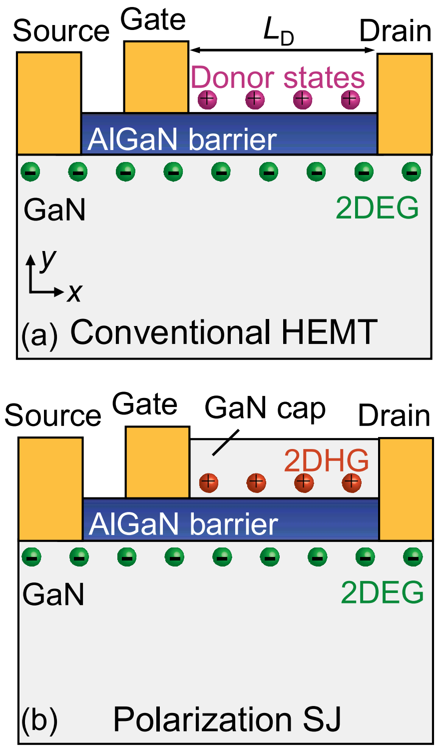

FIGURE 1. **(a) Schematic of conventional HEMT device and (b) of a Polarization Super Junction HEMT.**

charges in the depleted drift region (Fig. 1) [15], [16]. On the other hand, the lack of simple analytical models describing the off-state of PSJs and HEMTs does not allow easily comparing the performance of these devices and thus show the potential of polarization super junctions. In addition, an accurate investigation of PSJ switching performance is yet to be reported and some concerns are present due to the large charge depletion that is achieved in such devices, which could hinder their high-frequency operation.

In this work, we provide a detailed analysis and comparison of the main figures-of-merit describing the DC and switching performance of HEMT and PSJ devices. We propose a simple analytical model to describe the off-state behavior of HEMTs and PSJs based on the different carrier depletion mechanisms involved in such devices. From these results, we compare the $R_{ON,sp}$ vs V_{BR} performance of PSJs and HEMTs and show that a more than 10-time decrease in $R_{ON,sp}$ for the same V_{BR} can be achieved by PSJs with sheet resistance (R_{sh}) of 300 Ω/sq, which can be further improved by the use of multi-channel heterostructures to reduce R_{sh} down to ~80 Ω/sq [17]–[22]. In addition, we compare the switching losses of PSJs and HEMTs showing that a significant improvement in the $R_{ON} \times E_{oss}$ figure-of-merit, where E_{oss} is the energy stored in the device output capacitance, is achieved by PSJ devices both in the case of negligible and dominating parasitic contributions. This model enables a proper evaluation of the main figures-of-merit of lateral GaN power devices and shows the potential of PSJs to reduce both the DC and switching losses in power devices.

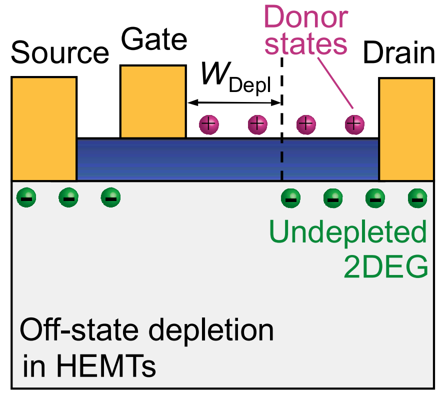

FIGURE 2. **Carrier depletion during the off-state in a HEMT device.**

II. MODELING

The main difference in the off-state behavior between PSJs and HEMTs comes from the origin of the 2DEG. In conventional GaN HEMTs, in which no GaN cap (or at most a thin cap of a few nanometers) is present on top of the AlGaN barrier, the source of electrons in the 2DEG are donor states at the interface [15], [16] (Fig. 1 (a)). These states are ionized by the polarization field, donating their electrons to the 2DEG and being left with a positive fixed charge with the same magnitude of 2DEG carrier concentration (N_s), similarly to what occurs in usual n-type doped semiconductors. On the contrary, in the case of PSJs, the thick GaN cap enables the formation of a 2DHG at the top AlGaN barrier interface having the same carrier concentration of the 2DEG [23], [24] (Fig. 1 (b)). The 2DHG provides the electrons to the 2DEG, without requiring the ionization of the donor states at the top interface. The key difference with respect to conventional HEMTs lies in the fact that the holes in the 2DHG are mobile and thus can be depleted in the off-state (if a proper ohmic contact between the gate/anode and the 2DHG is provided), while ionized donors are fixed charges that affect the off-state electric field profile according to the Poisson equation. This results in a neutral drift region in the off-state for PSJs, while positive fixed charges still remain in the case of HEMTs (Fig. 2).

To model such behaviors, the carrier depletion mechanisms for the two kinds of devices need to be investigated. Figure 3 (a) shows the simulated carrier depletion width (W_{Depl}) (see Fig. 2) as a function of the off-state voltage (V_D) for the drift region of a PSJ and HEMT device. It should be noted that the off-state depletion of the drift region of a diode and a transistor are equivalent, which enables employing the same general model for both devices. An intrinsic, 4 µm-thick buffer on an insulating substrate was considered to avoid any early breakdown through the buffer layer and provide a fair comparison between the two architectures. Throughout the manuscript, dashed lines represent

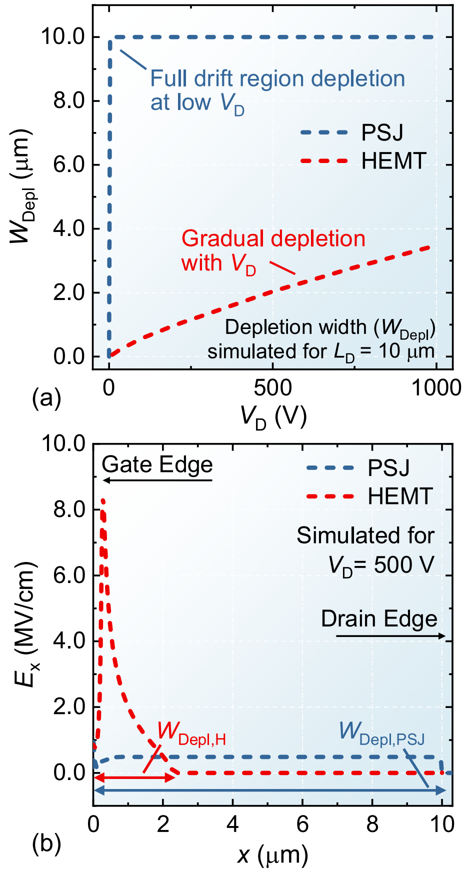

FIGURE 3. (a) Simulated carrier depletion width calculated fromthe gate edge (W_{Depl}) as a function of the off-state voltage for PSJs and HEMTs having the same drift region length. (b) Simulated off-state electric field profile in the 2DEG region along L_D for a PSJ and a HEMT device. All the simulation results presented in this work were obtained by employing the Atlas Silvaco software and using its built-in material parameters [52]. The polarization scale has been set to 0.92.

simulated results while solid lines are used for the analytical model. Blue lines are employed for PSJs while red is used for HEMTs.

PSJ devices show a complete carrier depletion of the whole drift region length (L_D) for V_D of only a few volts (Fig. 3 (a)). Such a depletion occurs for both electrons and holes, resulting in a neutral drift region. HEMTs present, instead, a smaller W_{Depl}, which requires much larger V_D values to grow and more closely resembles the case of doped semiconductors. The two different depletion mechanisms are directly linked to the off-state electric field profile in such devices. The efficient carrier depletion and the neutral drift region of PSJs result in a flat electric field profile in the whole L_D while the smaller W_{Depl} along with the presence of fixed positive charges in the depletion region lead to a non-uniform electric field profile with a peaked shape for HEMTs (Fig. 3 (b)). While based on these results PSJ devices intuitively should present improved off-state performance, an analytical model describing these devices is necessary to draw more quantitative conclusions while maintaining a detailed understanding of the physical mechanisms involved. In addition, this would enable determining the upper-performance limit of HEMTs and PSJs and properly estimating their potential and figures-of-merit for power conversion applications.

The off-state electric field profile for a HEMT is in general a complicated function due to the device's two-dimensional architecture (Fig. 2). Indeed, while a uniformly-doped semiconductor can be considered as a 1D problem, the presence of a sheet charge requires a two-dimensional treatment. Typical mathematical methods to address this problem are based on conformal mapping methods [25]–[29], which however result in very complicated and non-analytical solutions. Here, we propose a simplified approach that results in an analytical solution enabling direct comparison with PSJs, while still accurately describing the physical mechanisms that determine the device operation. In particular, the HEMT off-state electric field ($E_{x,HEMT}$) along the drift region direction (x) in the 2DEG region is approximated by a linear function having W_{Depl} as x-axis intercept and a slope such that the voltage drop in the depleted region is conserved (Fig. 4 (a)). The resulting expression is:

$$E_{x,HEMT} = \frac{qN_{s,HEMT}}{\varepsilon t_{eff}}\left(x - W_{Depl}\right) \tag{1}$$

where q is the magnitude of the electronic charge, $N_{s,HEMT}$ is the 2DEG concentration in the HEMT device and ε is GaN dielectric constant. t_{eff} is a geometrical parameter (in cm) which accounts for the electric field extension in the vertical direction due to its 2D distribution between the gate electrode and the undepleted 2DEG. This model enables us to treat a HEMT similarly to a conventional 1D doped device, greatly simplifying the mathematical expressions. It should be noted that the assumption of a linear field overestimates the breakdown voltage of HEMT devices, which in reality presents a more peaked electric field profile. However, since the goal of this work is to present the potential of PSJs with respect to conventional HEMT structures, this assumption only results in an underestimation of the performance improvement brought by PSJ. Besides, this model represents an improvement compared to previous works, in which the E_x profile of HEMTs is assumed to be flat in the whole drift region [3]. Such a hypothesis is not physically accurate due to the presence of ionized donor states with a positive charge and actually describes the case of PSJ devices, preventing a fair comparison between the two device architectures. The geometrical parameter t_{eff} accounts for the 2D distribution of the electric field between the gate electrode and the edge of the undepleted 2DEG. For this reason, it only depends on the device's geometrical parameters, such as the gate metal thickness and the dielectric constant of the passivation layer, and the depletion width, i.e. the separation between the gate electrode and the undepleted 2DEG. In particular, t_{eff} increases as W_{Depl} grows due to the more 2D shape of the electric field (Fig. 4 (b)). t_{eff} is instead independent of the specific combination of N_s and V_D that was

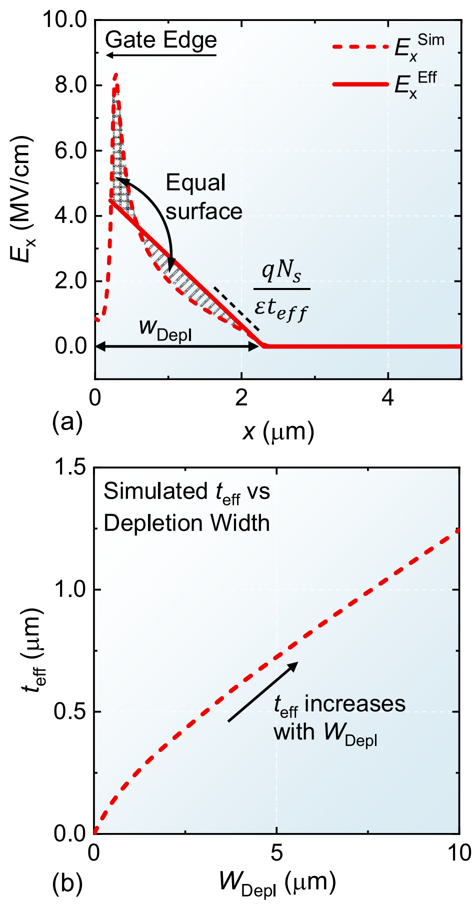

FIGURE 4. (a) Simulated off-state electric field (E_x^{Sim}) along L_D in the 2DEG region for a HEMT device and corresponding approximated linear field profile (E_x^{Eff}) assumed in the model (b) t_{eff} as a function of the depletion width extracted from the device simulation.

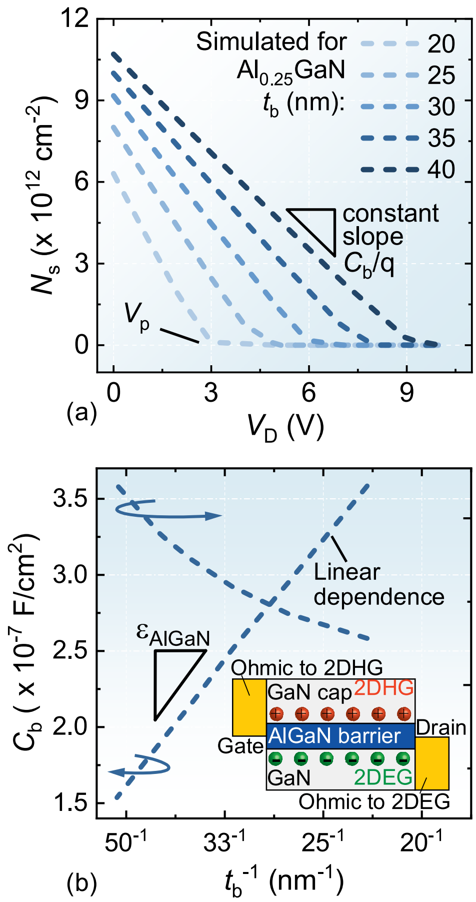

FIGURE 5. (a) Simulated carrier concentration N_s as a function of V_D for different $Al_{0.25}GaN$ barrier thicknesses. N_s was extracted by integrating the electron concentration in the 2DEG region along the vertical direction. A cut in the middle of the device's drift region was taken to avoid any possible carrier depletion from the contacts. (b) Barrier capacitance (C_b) and PSJ pinch off voltage (V_p), extracted from Figure 5 (a), as a function of the barrier thickness. The bottom-right inset shows a schematic of the simplified parallel plate capacitor model used to describe carrier depletion in PSJ devices.

required to achieve a certain depletion width. Indeed, such a combination only influences the magnitude of the electric field but not its distribution. While a mathematical formula for t_{eff} is challenging to obtain, its value can be determined from simulation by extracting the W_{Depl} for a certain off-state voltage V_D (Fig. 3 (a)) and using the expression:

$$t_{eff} = \frac{qN_{s,HEMT}W_{Depl}^2}{2\varepsilon V_D} \quad (2)$$

which is derived from eq. (1). Figure 4 (b) shows t_{eff} as a function of the depletion width for a HEMT with a 30 nm-thick $Al_{0.25}GaN$ barrier, 100 nm-thick gate contact, and 200 nm-thick Si_3N_4 passivation layer. Since the field distribution, and thus t_{eff}, depends on the exact device structure, slight adjustments to t_{eff} may be required in case a very different device architecture is used. However, for conventional device architectures, variations of t_{eff} well below 10 % are expected.

To model the off-state behavior of PSJs, the carrier depletion in these devices needs to be properly described. Figure 5 (a) shows the N_s as a function of the off-state voltage for different $Al_{0.25}GaN$ barrier thicknesses (t_b). While the N_s value at equilibrium ($V_D = 0$ V) increases for larger t_b, the carrier depletion varies linearly with the off-state voltage for all barrier thicknesses, which can be described by introducing an effective barrier capacitance (C_b) from the linear fit of the N_s vs V_D curve. Figure 5 (b) shows that C_b, extracted from Fig. 5 (a), increases linearly with the inverse of the barrier thickness (t_b^{-1}), with a slope equal to the dielectric constant of the AlGaN barrier. This behavior allows us to model the carrier depletion in PSJs with a simple parallel plate capacitor having the barrier as the insulator between the sheet charges of the 2DHG and 2DEG, with the gate providing an ohmic contact to the 2DHG and the drain to the 2DEG (Fig. 5 (b) inset). The 2DHG can be seen as acting similarly to a usual gate that forms a parallel-plate capacitor and uniformly depletes the 2DEG over the whole drift region, with a threshold voltage comparable to that of a typical Schottky gate. It should be noted that such a model is valid because of the small pinch-off voltage (V_p) required to completely deplete PSJ devices (Fig. 5 (b)) and the large Schottky barrier present between the drain metal and the 2DHG. In this condition, the conventional lateral depletion at the edges of the electrodes is negligible with respect to the drift region length and no significant leakage is present through the Schottky barrier. Besides, the barrier thickness is much smaller than L_D, which allows neglecting the parasitic capacitance between the two electrodes. The pinch-off voltage is only a few Volts for any realistic value of AlGaN barrier thickness (Fig. 5 (b)) and could be further reduced by employing higher polarization materials in the barrier, such as InAlN or AlN, which enable reducing t_b for a given N_s. Thanks to the small value of V_p compared to the breakdown voltage values considered in this work, the off-state electric field profile can be considered approximately flat in the whole PSJ drift region ($L_{D,PSJ}$) and be given by:

$$E_{x,SJ} = -\frac{V_D}{L_{D,PSJ}}. \quad (3)$$

III. STATIC FIGURE-OF-MERIT COMPARISON

Based on the electric field profiles for HEMTs and PSJs described in eqs. (1) and (3), we can compare the DC performance of the devices. It should be noticed that TCAD simulation was only employed to extract the t_{eff} parameter and to show the different physical mechanisms involved. The following analysis on the device figure-of-merit is entirely based on an analytical treatment. The breakdown voltage is typically obtained by considering the onset of avalanche breakdown by impact ionization, with the ionization integral being simplified by using Fulop's power law [3], [30]. Solving the resulting ionization integral using eqs. (1) and (3) and considering a complete depletion of the drift region, as in the case of a well-designed power device, one obtains a relation between V_{BR} and the drift region length for both device types, as described in [3]:

$$V_{BR,PSJ}\ [\mathrm{V}] = 0.94 \times 10^6\ L_{D,PSJ}^{6/7}\ [\mathrm{cm}] \quad (4)$$

$$V_{BR,HEMT}\ [\mathrm{V}] = 0.63 \times 10^6\ L_{D,HEMT}^{6/7}\ [\mathrm{cm}]. \quad (5)$$

These expressions, which depend only on the E_x profile and not on the carrier concentration, set an important link between the drift region length of PSJs and HEMTs. In particular, for a given V_{BR}, $L_{D,PSJ} = 0.67 \times L_{D,HEMT}$, which means that PSJ devices can have a shorter drift region to hold the same voltage thanks to the improved off-state electric field profile. Besides, one obtains also a relation between V_{BR} and N_s for HEMTs

$$V_{BR,HEMT}[\mathrm{V}] = 2.5 \times 10^{15}\mathrm{x}\left(N_{s,HEMT}\left[\mathrm{cm}^{-2}\right]/t_{eff}[\mathrm{cm}]\right)^{-3/4} \quad (6)$$

while, thanks to the very small value of V_p for any realistic carrier concentration, in a first approximation V_{BR} does not depend on N_s in PSJs.

For a lateral device, the specific on-resistance ($R_{ON,SP}$) is given by:

$$R_{ON,SP} = \frac{L_D^2}{q\mu N_s} \quad (7)$$

with μ the electron mobility. By inserting eq. (4) (for a PSJ) and eq. (5-6) (for a HEMT) in eq. (7), one can extract the expression of the device minimum $R_{ON,SP}$ achievable for a certain V_{BR}, which represents the main figure-of-merit to assess the upper-performance limit of power devices:

$$R_{ON,sp,HEMT}\left[\Omega \times \mathrm{cm}^2\right] = \frac{5.2 \times 10^{-16}}{\mu[\mathrm{cm}^2/\mathrm{Vs}]t_{eff}[\mathrm{cm}]} V_{BR}^{11/3}[\mathrm{V}] \quad (8)$$

$$R_{ON,sp,PSJ}\left[\Omega \times \mathrm{cm}^2\right] = 1.15 \times 10^{-14} \times R_{sh}[\Omega] V_{BR}^{7/3}[\mathrm{V}] \quad (9)$$

where R_{sh} is the heterostructure sheet resistance ($R_{sh} = 1/q\mu N_s$). To obtain t_{eff} as a function of V_{BR}, one can apply eq. (5) to Fig. 4 (b) in order to link W_{Depl} to V_{BR} since, for a well-designed power HEMT, W_{Depl} corresponds to L_D at the breakdown. Fig 6 (a) shows the dependence of t_{eff} on V_{BR}, which can be inserted in eq. (8) to plot HEMTs' specific on-resistance (Fig. 6 (b)). To further simplify eq. (8) and obtain a more general expression, one can approximate t_{eff} as a linear function of V_{BR} (Fig. 6 (a)). In addition, eq. (9) can be expressed as a function of N_s to offer a direct comparison between $R_{ON,sp,HEMT}$ and $R_{ON,sp,PSJ}$:

$$\begin{cases} R_{ON,sp,HEMT}\left[\Omega \times \mathrm{cm}^2\right] = \dfrac{7 \times 10^{-9}}{\mu\left[\frac{\mathrm{cm}^2}{\mathrm{Vs}}\right]} V_{BR}^{8/3}[\mathrm{V}] & (10) \\ R_{ON,sp,PSJ}\left[\Omega \times \mathrm{cm}^2\right] = \dfrac{0.7 \times 10^5}{\mu\left[\frac{\mathrm{cm}^2}{\mathrm{Vs}}\right] N_s\left[\mathrm{cm}^{-2}\right]} V_{BR}^{7/3}[\mathrm{V}] & (11) \end{cases}$$

Finally, the reduction in the specific on-resistance for PSJs compared to HEMTs can be derived considering the ratio between eqs. (11) and (10) and assuming the same mobility for the two devices:

$$\frac{R_{ON,sp,PSJ}}{R_{ON,sp,HEMT}} = \frac{1}{N_s\left[\mathrm{x}\ 10^{13}\mathrm{cm}^{-2}\right] V_{BR}^{1/3}[\mathrm{V}]} \quad (12)$$

A significant improvement in the $R_{ON,SP}$ vs V_{BR} limit can be achieved by PSJs using conventional AlGaN/GaN single-channel heterostructures. For instance, $R_{ON,SP,PSJ}$ can be reduced up to 10 times compared to $R_{ON,SP,HEMT}$ for typical heterostructures having $R_{sh} \sim 300$ Ω/sq (or $N_s \sim 1 \times 10^{13}$ cm^{-2}) for a breakdown voltage of 1000 V (Fig. 6 (b)), with a further reduction when devices with larger V_{BR} are considered (eq. (12)). It should be noted that often the electric field profile of HEMT devices is approximated to be flat in the whole L_D, which however erroneously results in the same $R_{ON,SP}$ vs V_{BR} limit as for PSJ devices. Nevertheless, as previously discussed, such an assumption is not physically accurate and leads to an overestimation of the potential of HEMT devices. This explains why real HEMTs present performance very far from this limit, which is instead properly described by the proposed model (Fig. 6 (b)).

In addition, we observe that for HEMTs, the V_{BR} depends on N_s (see eq. (6)) and thus the carrier concentration does not appear in eqs. (8) and (10). This is the usual situation for conventional semiconductor devices for which

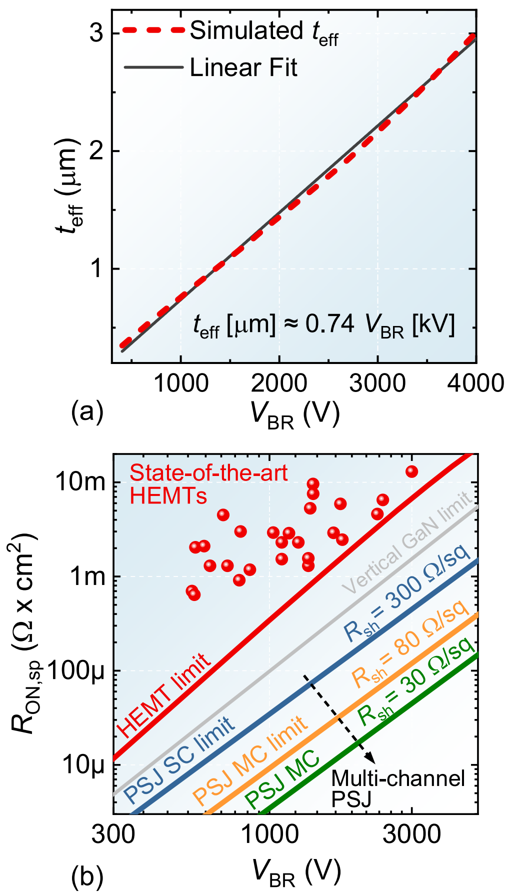

FIGURE 6. (a) t_{eff} as a function of the breakdown voltage extracted from Fig. 4 (b) and eq. (5), and corresponding linear fit (in black). (b) $R_{ON,SP}$ vs V_{BR} benchmark for HEMTs and PSJs with single and multiple channel heterostructures (SC and MC respectively) calculated from eqs. (8) and (9). Electron mobility of 2000 cm2/Vs was used. The solid lines represent the calculated theoretical limits for each architecture while the performance of state-of-the-art HEMTs devices in literature is reported in red dots.

there is a trade-off between the carrier concentration and the blocking capabilities. On the contrary, R_{sh} (and thus N_s) does not affect the off-state electric field (eq. (3)) and the breakdown voltage for PSJs (eqs. (9) and (11)), which allows increasing the device conductivity without degrading its blocking performance. While, one could achieve a low sheet resistance in conventional single-channel heterostructures by proper design of an AlN or AlInN barrier, a more effective way to significantly reduce the heterostructure R_{sh} is by using multiple parallel channels, which enable to increase the carrier concentration without degrading the mobility [17], [18], [31]. Besides, the growth of the multi-channel structure typically requires only a small increase in the growth time compared to the rest of the heterostructure, thus providing a cost-effective solution to significantly reduce the on-resistance in power devices. Following this approach, AlGaN/GaN multi-channel heterostructures with R_{sh} ∼ 80 Ω/sq have been shown experimentally, both with doped and undoped barrier layers, and power devices based on these structures have been demonstrated [17]–[21], revealing the feasibility in achieving high voltages in such high conductivity structures. Further increase in the number of channels and higher polarization barrier materials (such as lattice-matched InAlN [32] and AlN [33]) have resulted in structures with R_{sh} value down to ∼30 Ω/sq. As shown in Fig. 6 (b), the reduced sheet resistance of multi-channel PSJ devices would enable a considerable improvement in the $R_{ON,SP}$ vs V_{BR} trade-off, resulting in a decrease of the device resistance without affecting its off-state behavior.

IV. SWITCHING LOSSES COMPARISON

The different carrier depletion mechanisms in HEMTs and PSJs directly affect the device output capacitance (C_{oss}), which largely determines its switching losses. In particular, during hard switching, the energy stored in C_{oss} (E_{oss}) is dissipated at each switching cycle, resulting in the following expression for the hard-switching losses [34]–[36] (where losses during the turn-off are typically negligible for GaN devices and thus not considered [37], [38]):

$$P_{SW} = fE_{oss} + P_{IV} \tag{13}$$

where f is the operating frequency and P_{IV} is a term related to the current-voltage overlap during the switching transition.

The device C_{oss} can be modeled as the sum of a first term describing the carrier depletion in the drift region [25], [39], [40] (which depends on V_D), and a second contribution (C_p) related to the device geometry and the parasitic capacitance terms (which is independent on voltage) [25], [41]. According to the previous analysis on the carrier depletion (Figs. (4–5)), we can approximate C_{oss} as a step function for PSJs and as an increasing function $\sim 1/\sqrt{V_D}$ for HEMTs:

$$C_{oss,PSJ} = \begin{cases} C_b L_{D,PSJ} + C_p, & \text{for } V_D \leq V_p \\ C_p, & \text{for } V_D > V_p \end{cases} \tag{14}$$

$$C_{oss,HEMT} = \sqrt{\frac{q\varepsilon t_{eff} N_{s,HEMT}}{2V_D}} + C_p. \tag{15}$$

By integrating eqs. (14) and (15) with respect to V_D, the device output charge Q_{oss} is obtained, and a second integration results in E_{oss}:

$$E_{oss,PSJ} = \begin{cases} 1/2 C_b V_D^2 L_{D,PSJ} + 1/2 C_p V_D^2, & \text{for } V_D \leq V_p \\ 1/2 C_b V_p^2 L_{D,PSJ} + 1/2 C_p V_D^2, & \text{for } V_D > V_p \end{cases} \tag{16}$$

$$E_{oss,HEMT} \geq \frac{\sqrt{2\varepsilon q N_{s,HEMT} t_{eff}}}{3} V_D^{3/2} + \frac{1}{2} C_p V_D^2 \tag{17}$$

where the ≥ sign in eq. (17) results from assuming t_{eff} to be an increasing function with V_D, which is verified in Fig. 4 (b) and Fig. 6 (a). In order to analyze this result, two different cases will be considered, i.e. the situation in which the carrier depletion is the main term in C_{oss} (C_p negligible) and the case in which C_p is instead the dominant term. The relative magnitude of the two terms can strongly depend on the device structure and its packaging strategy, making it useful to consider both cases. Besides, to compare

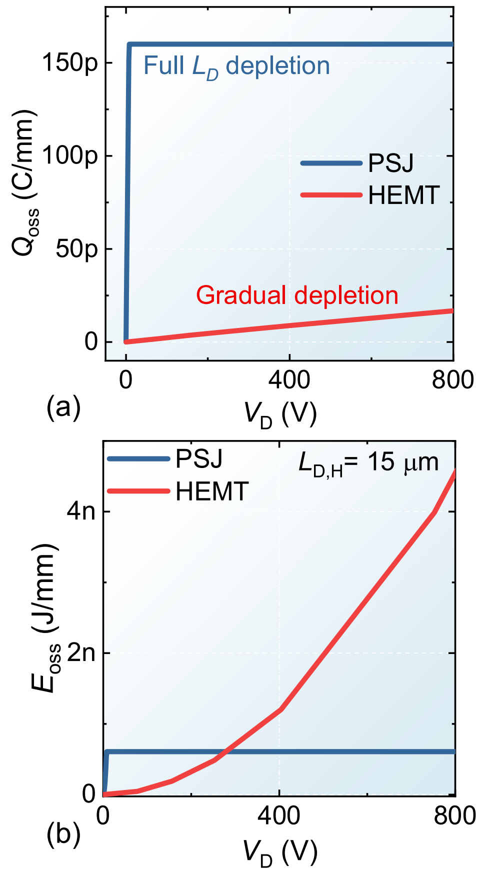

FIGURE 7. (a) Q_{oss} and (b) E_{oss} as a function of V_D for HEMT and PSJ devices in the case of negligible C_p calculated from eqs. (16) and (17).

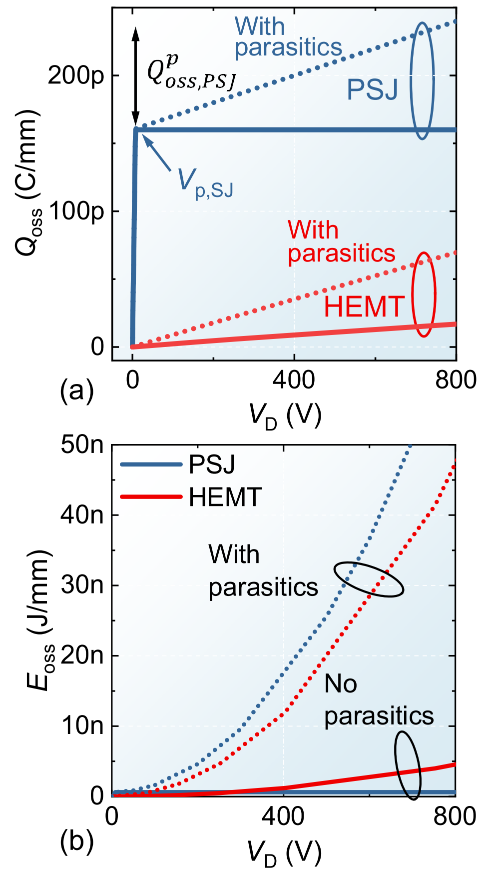

FIGURE 8. (a) Q_{oss} and (b) E_{oss} as a function of V_D for HEMT and PSJ devices for a negligible (solid lines) and non-negligible (dotted lines) parasitic capacitance contribution calculated from eqs. (16) and (17). C_p was set to 1 pF/cm for PSJs and 0.66 pF/cm for HEMTs, which reflects the different L_D required by the two devices to achieve the same V_{BR}.

devices having the same V_{BR}, eqs. (4), (5) and (6) will be considered, which impose $L_{D,PSJ} = 0.67 \times L_{D,HEMT}$ and set a relation between the HEMT carrier density and its V_{BR}.

The output charge for a negligible C_p is shown in Fig. 7 (a). Since Q_{oss} directly depends on the depletion width, a similar behavior as in Fig. 3 (a) is observed, with the PSJ output charge increasing sharply with V_D until the full drift region depletion at $V_D = V_p$ and with the HEMT Q_{oss} gradually rising over the whole V_D range. These differences in the Q_{oss} vs V_D profile result in an E_{oss} value that is larger for PSJs at low operating voltages but becomes much smaller than that of HEMTs when large V_D values are considered (Fig. 7 (b)). In particular, comparing the important switching figure-of-merit (FOM) $R_{ON} \times E_{oss}$ at the device rated voltage for PSJs and HEMTs, an important relationship is obtained:

$$\frac{R_{ON,PSJ} \times E_{oss,PSJ}}{R_{ON,HEMT} \times E_{oss,HEMT}} = 0.67\frac{V_p}{V_{BR}} \quad \text{for} \quad C_p = 0 \qquad (18)$$

Since the PSJs pinch-off voltage V_p is much smaller than the breakdown voltage of typical power devices (Fig. 5 (b)), PSJs enable to achieve a significant reduction in the $R_{ON} \times E_{oss}$ FOM, which increases as devices with larger voltage ratings are considered.

In real power devices, parasitic capacitance contributions to C_{oss} related to the device geometry rather than the drift region depletion can become significant depending on the device architecture. While an exact estimation requires the precise knowledge of the device structure, here a C_p of 1 pF/cm for $L_{D,PSJ}$ of 10 μm is assumed, which is a typical value for multi-finger scaled-up devices [25], [27]. Besides, we consider $C_p \sim 1/L_D$, resulting in a C_p value of 0.66 pF/cm for $L_{D,HEMT}$ of 15 μm. This assumption is favorable for HEMTs as parasitic terms usually have a weaker dependence on L_D for typical device dimensions [25], [27], [42].

Figure 8 (a) presents Q_{oss} as a function of V_D for non-negligible C_p. As a result of the parasitic contributions, an increase of Q_{oss} is observed, which is larger for PSJs due to the shorter drift region length. The corresponding E_{oss} vs V_D curves are presented in Fig. 8 (b), which shows a dominant contribution from the C_p term with respect to the depletion contribution. In this situation, PSJs present a larger E_{oss} value, due to their shorter L_D. However, a fair comparison between the two devices requires considering the $R_{ON} \times E_{oss}$ FOM:

$$\frac{R_{ON,PSJ} \times E_{oss,PSJ}}{R_{ON,HEMT} \times E_{oss,HEMT}} = \frac{3.4 \times 10^{20} \times \mathrm{t_{eff}[cm]}}{N_{s,PSJ}[\mathrm{cm}^{-2}]V_{BR}^{4/3}[\mathrm{V}]} \qquad (19)$$

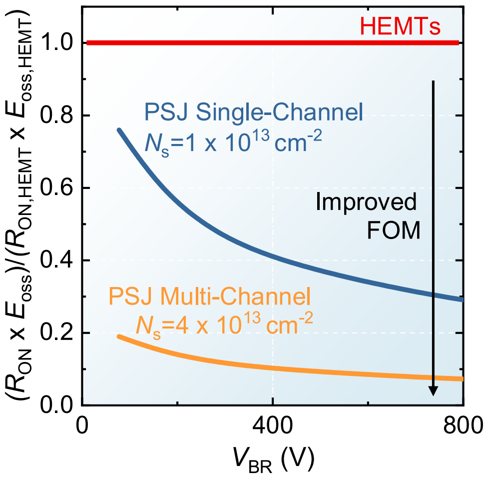

FIGURE 9. **Ratio between the $R_{ON} \times E_{oss}$ figure-of-merit for PSJs and HEMTs in the case of non-negligible parasitic capacitance contributions calculated from eq. (19).**

which can be further simplified in case the linear fit of t_{eff} vs V_{BR} (Fig. 6 (a)) is used:

$$\frac{R_{ON,PSJ} \times E_{oss,PSJ}}{R_{ON,HEMT} \times E_{oss,HEMT}} = \frac{2.5}{N_{s,PSJ}[\text{x } 10^{13}\text{cm}^{-2}]V_{BR}^{1/3}[\text{V}]} \tag{20}$$

The decoupling of N_s from the off-state performance for PSJ devices results in a better $R_{ON} \times E_{oss}$ FOM, which improves as the device V_{BR} increases (Fig. 9). Besides, by employing multi-channel structures with larger N_s it is possible to further reduce $R_{ON} \times E_{oss}$ to values 10 times lower than for HEMT devices.

Finally, for what concerns the P_{IV} contribution in eq. (13), this term is proportional to the external load current and is linked to the time required to discharge C_{oss} through the device channel. This time is usually determined by the circuit operation and by the addition of an external gate resistor to control the dV/dt. In these conditions, HEMTs and PSJs would exhibit similar P_{IV} as this term is entirely controlled by the external circuit. However, in the absence of a gate resistor or in the case of very low gate-path resistance, the transition speed depends only on the device properties. In this case, the strong non-linearity of C_{oss} for PSJ devices (see eq. (14)) results in a reduced overlap term at high voltages with respect to HEMTs. This is due to the efficient carrier depletion in PSJs, which leads to a very low C_{oss} value for off-state voltages above the pinch-off and translates in a reduction of the P_{IV} overlap term compared to HEMTs, similarly to what has been reported for Si devices [43]. Thus, since for PSJ devices the P_{IV} term is smaller or equal than for HEMTs while the E_{oss} contribution is much-reduced for any condition, we can conclude that PSJs result in a significant decrease of the overall switching losses.

V. MODEL BOUNDARIES

GaN lateral devices typically present a large density of traps at the heterostructure top interface. Electrons trapped in these surface states during the off-state partly deplete the 2DEG close to the gate edge and alleviate the electric field peak, resulting in an improvement of the device breakdown voltage [44]–[47] through a virtual gate effect. Yet, this mechanism is highly undesirable as it degrades the device resistance in the on-state, resulting in current collapse phenomena [48], [49]. A similar reasoning can also be applied to trap states in the buffer layer, which are often introduced to increase its resistivity but can act as trapping centers for electrons in the 2DEG. Thus, a more meaningful indicator of the device performance is represented by the dynamic on-resistance rather than the DC R_{ON}, which does not take into account trapping effects. In this work, the presence of trap states has not been considered as the exact estimation of their density and energy level is highly dependent on the device design and passivation strategy. However, all the analyses here reported remain valid by simply replacing R_{ON} with the dynamic on-resistance ($R_{ON,dyn}$) measured for experimental devices.

GaN layers also present a certain concentration of unintentional impurities (e.g., Si or O) due to contaminations during the growth, which can act as fixed net charges and affect the electric field profile. Nevertheless, recent advances in MOCVD growth have enabled impurity concentrations as low as 3×10^{15} cm^{-3} [50], [51], preventing significant effects on the device's off-state behavior. In this work, the role of impurities has not been included since their concentration can vary significantly depending on the growth technique and parameters, which prevents drawing any general conclusion. However, in the case of a significant presence of impurities, this can be readily accounted for in the presented equations by including an additional fixed net charge term.

Finally, GaN HEMTs usually also have few field plate (FP) structures. While the analytical treatment of field plates is rather straightforward [25], [28], their design varies significantly from device to device making it difficult to provide a general model. Yet, some considerations can be drawn. One of the main goals of FPs is to reduce the electric field peak at the gate edge. While the field profile in the FPs region differs from the one here presented, FPs typically extend only for a few microns and the majority of the off-state voltage falls on the portion of the drift region without FP. This situation is well described by the proposed model, which can be extended to include the presence of FPs [25], [28] once the precise device structure under investigation is known. Finally, the use of FPs results in an increased C_{oss} parasitic contribution (C_p) due to the reduced distance between electrodes, which increases the switching losses and poses an additional trade-off between E_{oss} and the blocking performance. The proposed model and analysis offer precious general insights into the operation mechanisms of two investigated devices and can be easily adapted to a specific device architecture, once its precise structure is known.

VI. CONCLUSION

In this work, we provided a detailed analysis and comparison of the main figures-of-merit describing the DC and switching performance of HEMT and PSJ devices. We proposed a simple analytical model to describe the off-state behavior of HEMTs and PSJs based on the different carrier depletion mechanisms involved in such devices. Based on these results, we showed that a 10-time decrease in $R_{\mathrm{ON,sp}}$ for the same V_{BR} can be achieved by single-channel PSJs, which can be further improved by the use of multi-channel heterostructures to reduce the sheet resistance. In addition, we compared the switching losses of PSJs and HEMTs showing that PSJ devices result in a significant improvement in the $R_{\mathrm{ON}} \times E_{\mathrm{oss}}$ figure-of-merit both in the case of negligible and dominating parasitic contributions. This model enables a proper evaluation of the main figures-of-merit of lateral GaN power devices and shows the potential of PSJs to reduce both the DC and switching losses in power devices.

REFERENCES

[1] K. J. Chen *et al.*, "GaN-on-Si power technology: Devices and applications," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 779–795, Mar. 2017, doi: 10.1109/TED.2017.2657579.

[2] H. Amano *et al.*, "The 2018 GaN power electronics roadmap," *J. Phys. D. Appl. Phys.*, vol. 51, no. 16, 2018, Art. no. 163001.

[3] B. J. Baliga, "Gallium nitride devices for power electronic applications," *Semicond. Sci. Technol.*, vol. 28, no. 7, 2013, Art. no. 074011, doi: 10.1088/0268-1242/28/7/074011.

[4] A. Nakajima, K. Adachi, M. Shimizu, and H. Okumura, "Improvement of unipolar power device performance using a polarization junction," *Appl. Phys. Lett.*, vol. 89, no. 19, pp. 87–90, 2006, doi: 10.1063/1.2372758.

[5] H. Ishida *et al.*, "Unlimited high breakdown voltage by natural super junction of polarized semiconductor," *IEEE Electron Device Lett.*, vol. 29, no. 10, pp. 1087–1089, Oct. 2008, doi: 10.1109/LED.2008.2002753.

[6] S. Han, J. Song, and R. Chu, "Design of GaN/AlGaN/GaN super-heterojunction schottky diode," *IEEE Trans. Electron Devices*, vol. 67, no. 1, pp. 69–74, Jan. 2020, doi: 10.1109/TED.2019.2953843.

[7] B. Song, M. Zhu, Z. Hu, K. Nomoto, D. Jena, and H. Xing, "Design and optimization of GaN lateral polarization-doped super-junction (LPSJ): An analytical study," in *Proc. Int. Symp. Power Semicond. Devices ICs*, 2015, pp. 273–276, doi: 10.1109/ISPSD.2015.7123442.

[8] H. Huang, J. Cheng, B. Yi, W. Zhang, and W. T. Ng, "A unified model for vertical doped and polarized superjunction GaN devices," *Appl. Phys. Lett.*, vol. 116, no. 10, 2020, Art. no. 102103, doi: 10.1063/1.5142855.

[9] X. Zhou, J. R. Howell-Clark, Z. Guo, C. W. Hitchcock, and T. P. Chow, "Performance limits of vertical GaN of conventional doped PN and natural polarization superjunction devices," *Appl. Phys. Lett.*, vol. 115, no. 11, 2019, Art. no. 112104, doi: 10.1063/1.5109389.

[10] A. Nakajima, Y. Sumida, M. H. Dhyani, H. Kawai, and E. M. Narayanan, "GaN-based super heterojunction field effect transistors using the polarization junction concept," *IEEE Electron Device Lett.*, vol. 32, no. 4, pp. 542–544, Apr. 2011, doi: 10.1109/LED.2011.2105242.

[11] H. Kawai *et al.*, "Low cost high voltage GaN polarization superjunction field effect transistors," *Phys. Status Solidi Appl. Mater. Sci.*, vol. 214, no. 8, 2017, Art. no. 1600834, doi: 10.1002/pssa.201600834.

[12] B. Shankar and M. Shrivastava, "Safe operating area of polarization super-junction GaN HEMTs and diodes," *IEEE Trans. Electron Devices*, vol. 66, no. 10, pp. 4140–4147, Oct. 2019, doi: 10.1109/TED.2019.2933362.

[13] S.-W. Han *et al.*, "Experimental demonstration of charge-balanced GaN super-heterojunction schottky barrier diode capable of 2.8 kV switching," *IEEE Electron Device Lett.*, vol. 41, no. 12, pp. 1758–1761, Dec. 2020, doi: 10.1109/LED.2020.3029619.

[14] V. Unni *et al.*, "2.4kV GaN polarization superjunction schottky barrier diodes on semi-insulating 6H-SiC substrate," in *Proc. Int. Symp. Power Semicond. Devices ICs*, 2014, pp. 245–248, doi: 10.1109/ISPSD.2014.6856022.

[15] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors," *Appl. Phys. Lett.*, vol. 77, no. 2, p. 250, 2000, doi: 10.1063/1.126940.

[16] S. Heikman, S. Keller, Y. Wu, J. S. Speck, S. P. DenBaars, and U. K. Mishra, "Polarization effects in AlGaN/GaN and GaN/AlGaN/GaN heterostructures," *J. Appl. Phys.*, vol. 93, no. 12, pp. 10114–10118, 2003, doi: 10.1063/1.1577222.

[17] L. Nela *et al.*, "Multi-channel nanowire devices for efficient power conversion," *Nat. Electron.*, vol. 4, pp. 284–290, Mar. 2021, doi: 10.1038/s41928-021-00550-8.

[18] J. Ma *et al.*, "1200 V multi-channel power devices with 2.8 Ω·mm ON-resistance," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2019, pp. 4.1.1–4.1.4, doi: 10.1109/IEDM19573.2019.8993536.

[19] L. Nela *et al.*, "Conformal passivation of multi-channel GaN power transistors for reduced current collapse," *IEEE Electron Device Lett.*, vol. 42, no. 1, pp. 86–89, 2020, doi: 10.1109/led.2020.3038808.

[20] J. Ma, C. Erine, P. Xiang, K. Cheng, and E. Matioli, "Multi-channel tri-gate normally-on/off AlGaN/ GaN MOSHEMTs on Si substrate with high breakdown voltage and low ON-resistance," *Appl. Phys. Lett.*, vol. 113, no. 24, 2018, Art. no. 242102, doi: 10.1063/1.5064407.

[21] J. Ma, G. Kampitsis, P. Xiang, K. Cheng, and E. Matioli, "Multi-channel tri-gate GaN power schottky diodes with low ON-resistance," *IEEE Electron Device Lett.*, vol. 40, no. 2, pp. 275–278, 2018, doi: 10.1109/LED.2018.2887199.

[22] M. Xiao *et al.*, "3.3 kV multi-channel AlGaN/GaN schottky barrier diodes with P-GaN termination," *IEEE Electron Device Lett.*, vol. 41, no. 8, pp. 1177–1180, Aug. 2020, doi: 10.1109/LED.2020.3005934.

[23] A. Nakajima *et al.*, "Generation and transportation mechanisms for two-dimensional hole gases in GaN/AlGaN/GaN double heterostructures," *J. Appl. Phys.*, vol. 115, no. 15, 2014, Art. no. 153707, doi: 10.1063/1.4872242.

[24] P. Liu *et al.*, "Characterization of two-dimensional hole gas at GaN/AlGaN heterointerface," in *Proc. 1st IEEE Work. Wide Bandgap Power Devices Appl. (WiPDA)*, 2013, pp. 155–158, doi: 10.1109/WiPDA.2013.6695585.

[25] D. Čučak *et al.*, "Physics-based analytical model for input, output, and reverse capacitance of a GaN HEMT with the field-plate structure," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 2189–2202, Mar. 2017, doi: 10.1109/TPEL.2016.2569404.

[26] D. Cucak *et al.*, "Physical model for GaN HEMT design optimization in high frequency switching applications," in *Proc. Eur. Solid-State Device Res. Conf.*, 2014, pp. 393–396, doi: 10.1109/ESSDERC.2014.6948843.

[27] D. Čučak, "Physics-based analytical modelling and optimization of the GaN HEMT with the field-plate structure for application in high-frequency switching converters," Ph.D. dissertaion, Automática, Ingeniería Eléctrica y Electrónica e Informática Industrial, E.T.S.I. Industriales (UPM), Madrid, Spain, 2017. [Online]. Available: https://oa.upm.es/47672/1/DEJANA_CUCAK.pdf

[28] J. Liu *et al.*, "Analytical model for the potential and electric field distributions of AlGaN/GaN HEMTs with gate-connected FP based on equivalent potential method," *Superlattices Microstruct.*, vol. 138, Feb. 2020, Art. no. 106327, doi: 10.1016/j.spmi.2019.106327.

[29] J. Si, J. Wei, W. Chen, and B. Zhang, "Electric field distribution around drain-side gate edge in algan/gan hemts: Analytical approach," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3223–3229, Oct. 2013, doi: 10.1109/TED.2013.2272055.

[30] W. Fulop, "Calculation of avalanche breakdown voltages of silicon $p-n$ junctions," *Solid-State Electron.*, vol. 10, no. 1, pp. 39–43, 1967, doi: 10.1016/0038-1101(67)90111-6.

[31] C. Erine, J. Ma, G. Santoruvo, and E. Matioli, "Multi-channel AlGaN/GaN in-plane-gate field-effect transistors," *IEEE Electron Device Lett.*, vol. 41, no. 3, pp. 321–324, Mar. 2020, doi: 10.1109/LED.2020.2967458.

[32] P. Sohi, J.-F. Carlin, M. D. Rossel, R. Erni, N. Grandjean, and E. Matioli, "High conductivity InAlN/GaN multi-channel two-dimensional electron gases," *Semicond. Sci. Technol.*, vol. 36, no. 5, p. 6, 2021, doi: 10.1088/1361-6641/abf3a7.

[33] Y. Cao, K. Wang, G. Li, T. Kosel, H. Xing, and D. Jena, "MBE growth of high conductivity single and multiple AlN/GaN heterojunctions," *J. Cryst. Growth*, vol. 323, no. 1, pp. 529–533, 2011,

doi: 10.1016/j.jcrysgro.2010.12.047.

[34] L. Nela, N. Perera, C. Erine, and E. Matioli, "Performance of GaN power devices for cryogenic applications down to 4.2 K," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7412–7416, Jul. 2020, doi: 10.1109/TPEL.2020.3047466.

[35] E. A. Jones, F. Wang, D. Costinett, Z. Zhang, and B. Guo, "Temperature-dependent turn-on loss analysis for GaN HFETs," in *Proc. IEEE Conf. Appl. Power Electron. Expo. (APEC)*, 2016, pp. 1010–1017, doi: 10.1109/APEC.2016.7467994.

[36] R. Hou, J. Lu, and D. Chen, "Parasitic capacitance Eqoss loss mechanism, calculation, and measurement in hard-switching for GaN HEMTs," in *Proc. IEEE Conf. Appl. Power Electron. Expo. (APEC)*, pp. 919–924, Mar. 2018, doi: 10.1109/APEC.2018.8341124.

[37] G. Deboy, O. Haeberlen, and M. Treu, "Perspective of loss mechanisms for silicon and wide band-gap power devices," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 2, pp. 89–100, 2017, doi: 10.24295/cpsstpea.2017.00010.

[38] X. Li, L. Zhang, S. Guo, Y. Lei, A. Q. Huang, and B. Zhang, "Understanding switching losses in SiC MOSFET: Toward lossless switching," in *Proc. IEEE 3rd Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, 2015, pp. 257–262.

[39] L. Nela, G. Kampitsis, J. Ma, and E. Matioli, "Fast-switching Tri-anode schottky barrier diodes for monolithically integrated GaN-on-Si power circuits," *IEEE Electron Device Lett.*, vol. 41, no. 1, pp. 99–102, Jan. 2020, doi: 10.1109/LED.2019.2957700.

[40] L. Nela, R. Van Erp, G. Kampitsis, H. K. Yildirim, J. Ma, and E. Matioli, "Ultra-compact, high-frequency power integrated circuits based on GaN-on-Si Schottky barrier diodes," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1269–1273, Feb. 2021, doi: 10.1109/tpel.2020.3008226.

[41] C. Yin, Y. Li, and Y. Pei, "AlGaN/GaN HEMTs large signal model considering nonlinear Cds," in *Proc. Int. Appl. Comput. Electromagn. Soc. Symp. (ACES)*, 2017, pp. 1–2.

[42] F. R. Zypman, "Mathematical expression for the capacitance of coplanar strips," *J. Electrostat.*, vol. 101, Sep. 2019, Art. no. 103371, doi: 10.1016/j.elstat.2019.103371.

[43] *Superjunction MOSFET for Charger Applications—Application Note*, Infineon Technol. AG, Neubiberg, Germany, 2016.

[44] A. Nakajima, S. Yagi, M. Shimizu, and H. Okumura, "Effect of deep trap on breakdown voltage in AlGaN/GaN HEMTs," in *Proc. Mater. Sci. Forum*, vol. 600–603, Sep. 2008, pp. 1345–1348, doi: 10.4028/www.scientific.net/msf.600-603.1345.

[45] L. Zhu *et al.*, "Theoretical analysis of buffer trapping effects on off-state breakdown between gate and drain in AlGaN/GaN HEMTs," in *Proc. IEEE Int. Conf. Integr. Circuits Microsyst. (ICICM)*, 2017, pp. 33–36, doi: 10.1109/ICAM.2016.7813558.

[46] A. M. Wells, M. J. Uren, R. S. Balmer, K. P. Hilton, T. Martin, and M. Missous, "Direct demonstration of the 'virtual gate' mechanism for current collapse in AlGaN/GaN HFETs," *Solid-State Electron.*, vol. 49, no. 2, pp. 279–282, 2005, doi: 10.1016/j.sse.2004.10.003.

[47] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Misha, "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 560–566, Mar. 2001, doi: 10.1109/16.906451.

[48] T. Hashizume, K. Nishiguchi, S. Kaneki, J. Kuzmik, and Z. Yatabe, "State of the art on gate insulation and surface passivation for GaN-based power HEMTs," *Mater. Sci. Semicond. Process.*, vol. 78, pp. 85–95, May 2018, doi: 10.1016/j.mssp.2017.09.028.

[49] Z. Yatabe, J. T. Asubar, and T. Hashizume, "Insulated gate and surface passivation structures for GaN-based power transistors," *J. Phys. D. Appl. Phys.*, vol. 49, no. 39, Sep. 2016, Art. no. 393001, doi: 10.1088/0022-3727/49/39/393001.

[50] T. Ciarkowski, "Low impurity content GaN prepared via OMVPE for use in power electronic devices: Connection between growth rate, ammonia flow, and impurity incorporation," Virginia Polytechnic Inst. State Univ., Blacksburg, VA, USA, 2019.

[51] T. Ciarkowski *et al.*, "Connection between carbon incorporation and growth rate for GaN epitaxial layers prepared by OMVPE," *Materials*, vol. 12, no. 15, p. 2455, 2019, doi: 10.3390/ma12152455.

[52] J. Piprek, *Nitride Semiconductor Devices—Principles and Simulation*. Hoboken, NJ, USA: Wiley, 2007, doi: 10.1002/9783527610723.