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A High-Performance SiC Super-Junction MOSFET With a Step-Doping Profile

HAO HUANG[1], YING WANG[1], CHENG-HAO YU[1], ZHAO-HUAN TANG[2], XING-JI LI[3] (Senior Member, IEEE), JIAN-QUN YANG[3], AND FEI CAO[1]

1 Key Laboratory of RF Circuits and Systems, Ministry of Education, Hangzhou Dianzi University, Hangzhou 310018, China
2 The National Key Laboratory of Analog Integrated Circuits, China Electronics Technology Group Corporation, Chongqin 400060, China
3 National Key Laboratory of Materials Behavior and Evaluation Technology in Space Environment, Harbin Institute of Technology, Harbin 150080, China

CORRESPONDING AUTHORS: Y. WANG and C.-H. YU (e-mail: wangying7711@yahoo.com; yuchenghao@hdu.edu.cn)

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ABSTRACT In this article, we investigate a 4H-SiC super- junction (SJ) MOSFET structure with a charge-imbalance doping-profile. According to our numerical simulations and comparisons with the conventional SiC VDMOS (C-VDMOS) and SiC SJ VDMOS (SJ-VDMOS) devices, the SJ-MOD structure offers a better trade-off between breakdown voltage (BV) and specific on-resistance ($R_{on,sp}$). This leads to a high figure of merit ($FOM = BV^2/R_{on,sp}$). In addition, due to the reduced electric field peak, the single-event burnout (SEB) of the device is significantly improved. The simulation results indicate that, using a LET value of 0.1 pC/μm and a 3000K global device temperature as the criterion for burning, the specific burnout-threshold voltage (using the optimal parameters of the proposed structure) exceeds that of the conventional structure. This indicates that the modified super-junction structure can indeed be used for different voltage-classes of the hardening SiC super-junction devices in the future.

INDEX TERMS SiC MOSFET, breakdown voltage, specific on-resistance, figure of merit.

I. INTRODUCTION

Higher rated voltage, lower on-resistance, better switching frequency, and superior radiation-resistance are among the many very useful properties of silicon carbide. It is a promising material for high-power applications [1]–[4]. Recently, many studies of SiC devices with different structures were conducted [5]–[10]. The studies typically focused on device performance, which was mainly characterized by breakdown voltage (BV), specific on-resistance ($R_{on,sp}$), maximum gate-oxide field ($E_{ox,max}$), and gate charge (Q_g) [11], [12].

In 2004, Miura *et al.* fabricated the first SiC lateral SJ-diode [13]. Its breakdown voltage was found to be more than 3 times higher than the theoretically expected value. In 2008, Yu and Sheng developed a novel analytical model for both the breakdown voltage and on-resistance of the 4H-SiC super-junction devices [14]. In 2014, Kosugi *et al.* performed the first experiment to show that the SiC could be used for multilayer epitaxial technology. Both epitaxial growth and MeV-class implantation steps were alternately repeated, and a device with a BV of 1545 V and an $R_{on,sp}$ of 1.06 mΩ·cm^2 was successfully fabricated [15]. Recently, the reliability of the SiC-SJ devices has also been studied in more depth. Gonzalez *et al.* investigated the Si and SiC diodes, compared the performance of Si and SiC devices, discussed device reliability, and considered avalanche ruggedness [16].

Single-event burnout (SEB) is considered as a catastrophic effect, which causes the power MOSFETs to fail in space applications [17]. In silicon-based processes, the SEB-triggering mechanism generates a transient current, which causes the parasitic bipolar transistor to produce excessive current and lead to the thermal destruction of the device [18]. In a SiC-based process, on the other hand, the above mechanism contributes less to a SEB. The biggest problem is the impact ionization under the high electric field, which produces a rapidly increasing current in the device [19].

Charge imbalance doping device was first proposed by Vudumula and Kotamraju [20]. In recent years, researchers have combined wide-gap semiconductors with this structure to apply to silicon carbide-based MOSFETs, and they have obtained better characteristics [21].

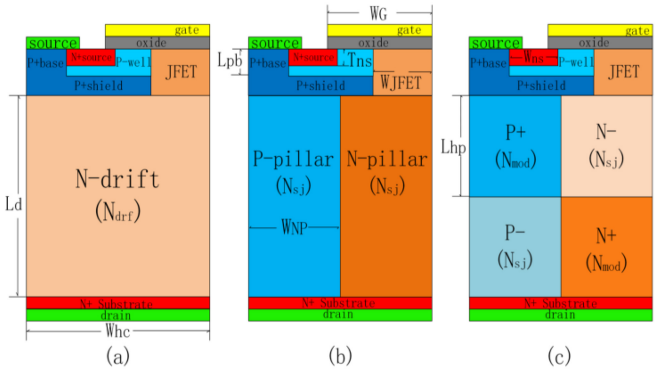

FIGURE 1. The structures of the three studied SiC MOSFET devices:(a) C-VDMOS, (b) SJ-VDMOS, and (c) SJ-MOD-VDMOS.

In this paper, we investigated a SiC power super-junction MOSFET with a charge-imbalance doping-profile, which is referred to as a super-junction-modified VDMOSFET (SJ-MOD-VDMOS). The performance of the SiC MOSFETs was simulated using the Silvaco TCAD ATLAS. The main design idea was to reduce the electric field intensity by adding a different doping-profile as electric-field modulation structure to enable optimization. In addition, the outcomes of this study may facilitate SEB hardening effect via super-junction silicon carbide structure. The TCAD simulation indicated that, compared with a conventional VD-MOSFET and a conventional super-junction MOSFET, the SJ-MOD-VDMOSFET significantly reduced the area specific on- resistance.

This approach also yielded a high figure of merit (FOM = $BV^2/R_{on,sp}$). Furthermore, the simulation results showed that, for a LET value of 0.1 pC/μm and 3000K global device temperature as burning criterion, the specific burnout threshold voltage (using optimal parameters) of the proposed structure was higher than for the conventional structure.

II. DESCRIPTIONS OF DEVICE STRUCTURE AND FABRICATION PROCEDURE

Figs. 1(a)-(c) show the schematic diagrams of the SiC conventional p-type shield region VDMOS (C-VDMOS) [22], the SiC conventional super-junction VDMOS (SJ-VDMOS) [23], and the SiC super-junction modified VDMOS (SJ-MOD- VDMOS). As shown in Fig. 1, both the conventional SJ and the modified SJ have a P/N column instead of the typical drift-region in a conventional VDMOS. Compared with the conventional SJ structure, the SJ-MOD P/N column is doped unevenly. The important device parameters are listed in Table 1. To facilitate a comparison in terms of performance, the thickness of the epitaxial layer in the three devices was set to be equal, and the device parameters of the proposed structure were optimized to achieve the best performance.

The process flow of the SJ-MOD-VDMOS is presented in Fig. 2. First, the N+layer and the N−layer were formed on the N+ substrate as the starting material, as shown in Fig. 2(a). Next, as can be seen in Fig. 2(b), the trench was formed by the dry etching process. Then, the chemical-vapor deposition trench filling was completed [24], [25]. Sequential depositions of the P− layer and P+ layer were formed to achieve the SJ p-type pillar, shown in Fig. 2(c). Then, an N−type JFET epitaxial layer was grown on the drift layer as shown in Fig. 2(d). Next the P+ shield region and p-well region were formed by the ion implantation. Further, the N+ source and P+ base region were formed on the p-well layer by ion implantation, as shown in Fig. 2(e). P+shield layer reduced the electric field enhancement in the middle of the gate oxide, protected it from the high electric fields under blocking state. Then, the gate oxide was formed

TABLE 1. Device parameters for the simulations.

Parameter	Value
Drift/pillar depth (L_d)	10 μm
Width of half cell (W_{hc})	5.5 μm
Substrate thickness (T_{sub})	1 μm
p-base region thickness (L_{pb})	0.5 μm
Width of half JFET region (W_{JFET})	2 μm
Deep of JFET region (L_{JFET})	*1* μm
Length of channel	0.5 μm
Gate oxide thickness (T_{os})	80 nm
Width of half gate oxide (W_G)	3 μm
Thickness of n+source junction (T_{ns})	0.3 μm
Width of half N/P pillar (W_{NP})	2.75 μm
Length of half pillar (L_{hp})	5 μm
p-base dopant concentration	1.0×10^{19} cm^{-3}
n^- drift dopant concentration (N_{drift})	OPTIMIZED
n^+ source dopant concentration	1×10^{19} cm^{-3}
p+shield region dopant concentration	1×10^{19} cm^{-3}
JFET region dopant concentration	2×10^{16} cm^{-3}
p-well dopant concentration	6×10^{16} cm^{-3}
SJ-pillar dopant concentration (N_{sj})	OPTIMIZED
SJ-mod dopant concentration (N_{mod})	OPTIMIZED

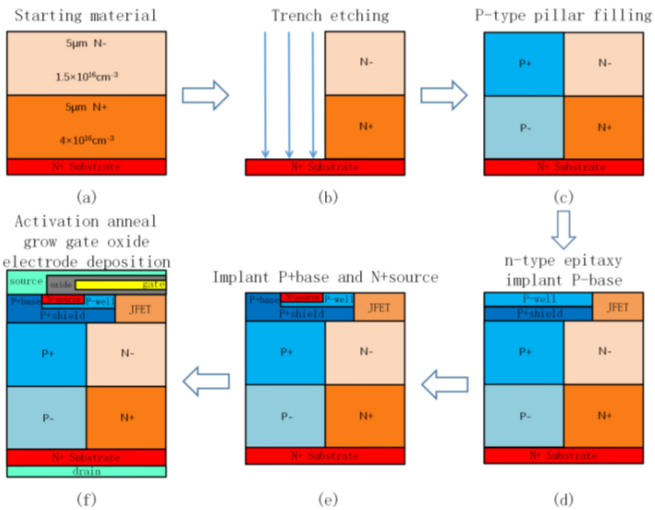

FIGURE 2. Fabrication process of the SJ-MOD-VDMOSFET.

TABLE 2. SEB parameters for the simulations.

Parameter	value
Temperature	300K
LET	0.1pC/μm
Track radius	0.05μm
Initial charge generation time	10ps
Temporal Gaussian function width	2ps
Ion track length	13μm

by the thermally oxidized process, and the three electrodes were fabricated. The whole device structure was shown in Fig. 2(f).

III. NUMERICAL SIMULATION SETUP

In this article, we investigated and compared the performance of a 4H-SiC super-junction modified VDMOS, a conventional VDMOS, and a conventional super-junction VDMOS, which are shown in Fig. 1. The simulations were done by using the Silvaco ATLAS device simulator, which could perform a 2-D numerical simulation [26]. At room temperature (300 K), the source was always grounded.

The forward characteristics, the breakdown characteristics, transient SEB events were carried out by using different physical models [27]. Two models, ANALYTIC (Caughey Thomas Analytic model) and FLDMOB (FLD mobility model), also take into account concentration-dependent mobility (CONMOB), which characterizes the relationship between carrier concentration and the mobility. In addition, because of the heavily doped region, a bandgap narrowing (BGN) model was introduced. Both the incomplete-ionization model and the Selberherr model were also utilized to calculate the ionization rate. The recombination models included the Shockley-Read- Hall (SHR) model and the AUGER model. Furthermore, LAT.TEMP was used for the lattice-heating simulation. For the transient SEB simulation, the used physical parameters were temperature-dependent.

The important material parameters of the ion radiation, which were used in the simulations were shown in Table 2 [24], [28]–[31]. The goal of this study was to simulate impact ionizing accurately. The generation rate function that considered the electron-hole pair generation in a specific structure area, the generation rate, could be formulated as follows:

$$Rate = A(l) \times R(\omega, l) \times T(t) \tag{1}$$

Here, $A(l)$ was the LET generation density. $R(\omega, l)$ and $T(t)$ indicated the spatial and temporal Gaussian functions, which were used to describe the generated electron-hole pairs along the ion track. The linear energy-transfer was constant along the ionization track. It was selected because the LET was relatively invariable throughout a certain range [32]–[34]. Specifically, the LET value was set to 0.1 pC/μm. The other parameters, which were used in the SEB simulation, were shown in Table 2.

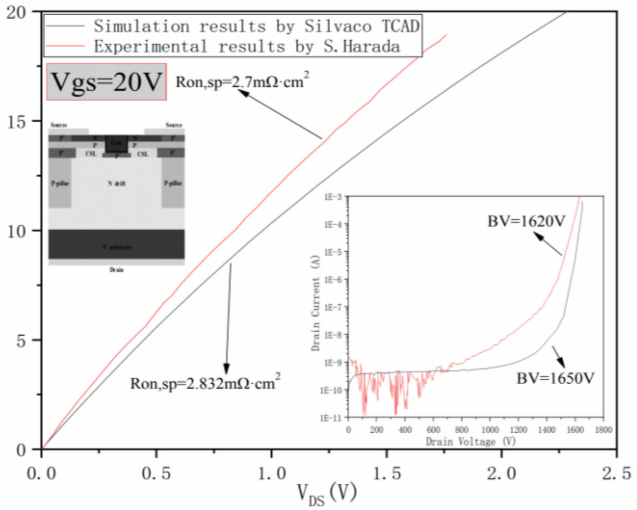

FIGURE 3. I_D–V_{DS} characteristics and off-state characteristics from the simulation and experiment results of IE-MOSFET to validate the effectiveness of models used in the simulation.

In order to calibrate the simulation model or verify the accuracy of the model, Fig. 3 compares the I_D-V_{DS} characteristics and off-state characteristics of the IE-UMOSFET abstracted from the experimental results by Harada *et al.* [25]. The simulation results were performed at $Vgs = 20$ V and $Vds = 1$ V. The $R_{on,sp}$ of 2.7mΩ·cm^2 from the experimental result was almost similar to that of 2.832 mΩ·cm^2 from Silvaco TCAD simulation, and at $Vgs = 0$V, the $BV = 1620$V from the experimental result was almost similar to that of 1650V from Silvaco TCAD simulation.

IV. ANALYSIS AND DISCUSSIONS

In this section, we presented and analyzed the simulation results of the on-state characteristic, the off-state characteristics and the single-event burnout characteristic. The results demonstrated that the basic features of the proposed structure have been significantly improved. In addition. Compared with the first two devices, the SJ-MOD VDMOS was less sensitive against the SEB than the conventional VDMOSFET and conventional SJ-VDMOS because of the gradient doping in drift region.

A. ON-STATE CHARACTERISTIC

Fig. 4 shows the output characteristics of the three devices. The doping concentrations for the three devices were optimized to present the maximum FOM. N_{drift} was 5×10^{15}cm^{-3} in the C-VDMOS structure, while N_{sj} was 1.5×10^{16}cm^{-3} in both the SJ-VDMOS and the SJ-MOD-VDMOS. Furthermore, N_{mod} was 4×10^{16}cm^{-3} in the SJ-MOD-VDMOS. At $V_{GS} = 20$V and $V_{DS} = 1$V, the $R_{on,sp}$ (specific on-resistance) of the proposed device was calculated to be 2.92mΩ·cm^2, while the $R_{on,sp}$ of the conventional VDMOS and conventional SJ-VDMOS were 5.92 mΩ·cm^2

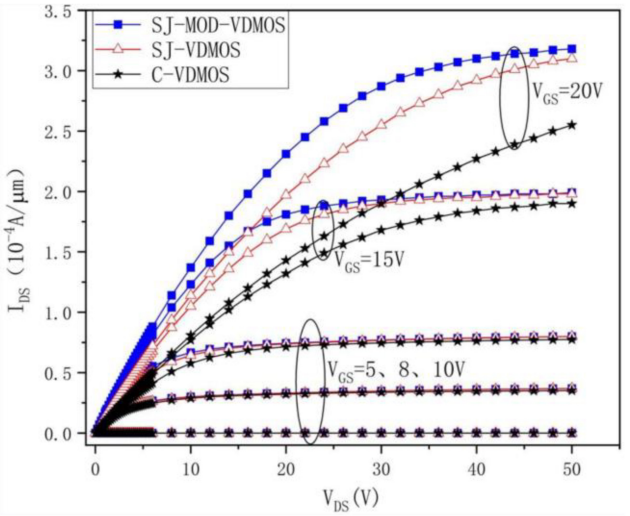

FIGURE 4. ON−state characteristics for the three optimized structures.

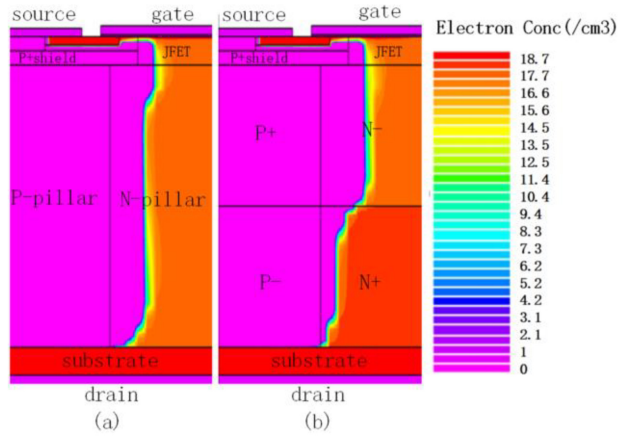

FIGURE 5. Distribution of the electron concentration in (a) the SJ-VDMOS, and (b) the SJ-MOD-VDMOS.

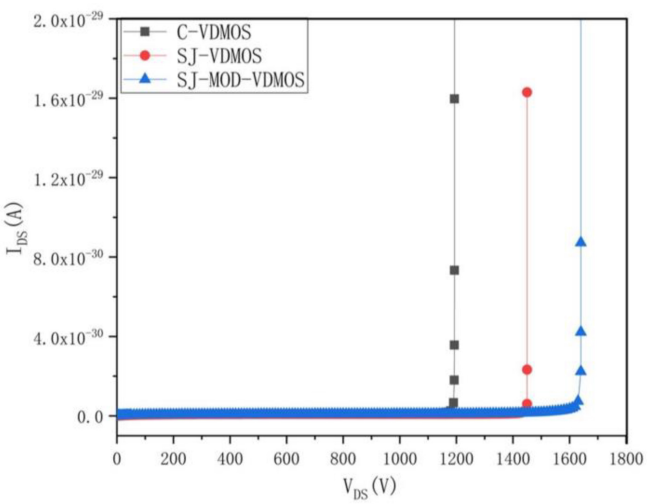

FIGURE 6. OFF-state characteristic of the three optimized structures. V_{GS} = 0V, and all devices have the same width (1μm).

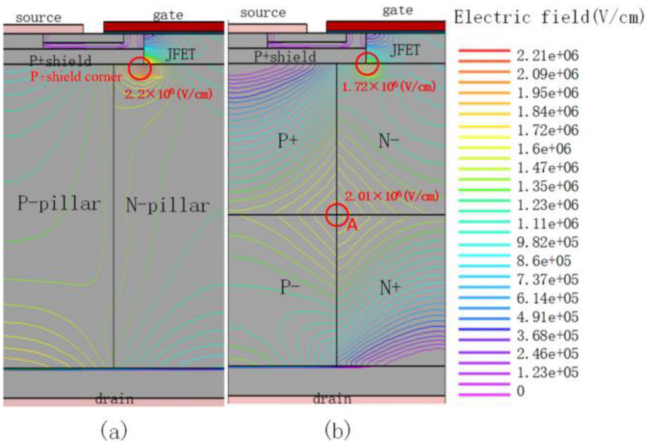

FIGURE 7. Electric field distribution of the SJ-VDMOS and the SJ-MOD-VDMOS. (V_{GS} = 0V, V_{DS} = 1200V) both devices have the same width (1μm).

and 4.04 mΩ·cm^2, respectively. Here, the $R_{on,sp}$ was calculated using the function of $W \cdot V_{ds}/I_{ds}$. Thus, the current path was widened, as shown in the Fig. 5. The heavily doped p-type region at high-position made the current path slightly narrower. However, in the on state, a suitably optimized concentration could enable a good trade-off result for the $R_{on,sp}$ decrease.

Because of the higher N_{sj}, the specific on-resistance of both SJ devices were much lower than for the C-VDMOS device. Compared with C-VDMOS and SJ-VDMOS, the $R_{on,sp}$ decreased by 50.7% and 27.7%, respectively. In other words, the novel structure had a significantly better on-state characteristic than the referenced devices.

B. OFF-STATE CHARACTERISTICS

Fig. 6 shows the off-state characteristic curves of the three structures, it can be seen that the *BVs* of the SJ-MOD-VDMOS, SJ-VDMOS and C-VDMOS were 1668V, 1452 V, and 1194 V, respectively. Generally, the widths of the SJ NP pillars were equal, and the doping concentrations were the same. Hence, the charge balance can be obtained more easily to ensure the breakdown voltage [14]. However, in the actual MOSFET structure, a slight charge-imbalance can alter the electric-field structure under high bias [35], which increases the breakdown voltage. Fig. 7(a) and (b) are the electric field line distributions of the two devices for $V_{GS} = 0$V and $V_{DS} = 1200$V.

The electric modulation structure distributed the electric field peak in the corners to give a value less than 3MV/cm, which was the safe operating electric field of the SiC device. The electric field peak of the new structure appeared at the position A and P+ shield corner as shown in Fig. 7. To obtain the maximum breakdown voltage, the N_{mod} was adjusted to 4×10^{16}cm^{-3}. In this way, the electric fields at points A and p+shield corner were almost identical. Furthermore, at $V_{GS} = 0$V and $V_{DS} = 1200$V, we can see that the maximum p+shield corner of the SJ-VDMOS was 2.2×10^6V/cm, while

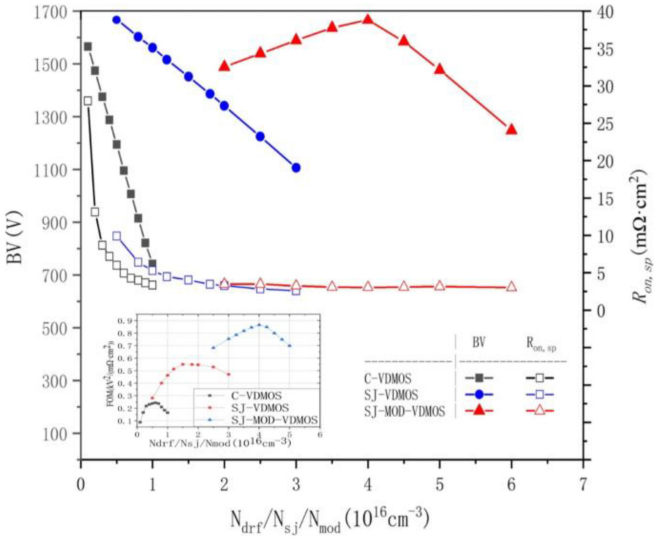

FIGURE 8. Dependency of the BV and $R_{on,sp}$ on the doping concentration (N_{sj} for the SJ-VDMOS devices, N_{drf} for the C-VDMOS device, N_{mod} for the SJ-MOD-VDMOS N+/P+ region while the N−/P−regions were set to a constant doping concentration of 1.5×10^{16}cm^{-3}). The inset shows the dependency of the FOM on the doping concentration. All three devices have the same width (1μm).

the SJ-MOD-VDMOS was 1.72×10^{6}V/cm. The electric field at position A was 2.01×10^{6}V/cm, which is slightly higher than the electric field in the corners. Clearly, the high-field region of the SJ-MOD- VDMOS was much smaller than that in the SJ-VDMOS. Thus, as the drain bias voltage continuing to increase, the SJ-MOD-VDMOS was more difficult to reach the electric field limitation.

Fig. 8 shows the breakdown voltage and $R_{on,sp}$ with the doping. Among them, the SJ-MOD-VDMOS curve was go with N_{mod} when N_{sj} was set to the optimized constant value of 1.5×10^{16}cm^{-3} as mentioned above. As the N_{drift} and N_{sj} increased in the C-VDMOS and SJ-VDMOS, both breakdown voltage and on-resistance decreased simultaneously. However, in the SJ-MOD- VDMOS, the breakdown voltage firstly increased and then decreased with increasing in N_{mod}.

This was because the charge-imbalance, which was caused by the change of N_{mod}. Point A in Fig. 7 initially shared the peak electric field peak in the P+shield corner, Subsequently, as N_{mod} increased, the electric-field peak shifted to point A, which triggered the avalanche breakdown. Hence, when the N_{mod} exceeded 4×10^{16}cm^{-3}, as the doping concentration increased, the charge-imbalance led to a substantial decrease in the *BV*. Overall, these results indicated that, under the same thickness of drift region, the *BV* of the SJ-MOD-VDMOS was improved by 216V and 474V compared with the SJ-VDMOS and the C-VDMOS, respectively. In addition, the $R_{on,sp}$ of the SJ-MOD-VDMOS was reduced by 1.12 mΩ·cm^2 and 3.00 mΩ·cm^2, compared with the two devices above. The maximum FOM of the SJ-MOD-VDMOS calculate to be 0.953 kV^2/(mΩ·cm^2) while the maximum FOM of the conventional VDMOS and conventional SJ-VDMOS were 0.241 kV^2/(mΩ·cm^2) and 0.522 kV^2/(mΩ·cm^2). The maximum FOM of the SJ-MOD- VDMOS was improved by 0.431 kV^2/(mΩ·cm^2) and 0.712 kV^2/(mΩ·cm^2), respectively. Therefore, the trade-off between the BV and $R_{on,sp}$ was much better in the SJ-MOD-VDMOS, compared with the SJ-VDMOS and C-VDMOS devices as shown in Fig. 8.

C. SINGLE-EVENT BURNOUT CHARACTERISTIC

The SEB simulation parameters were listed in Table 2. We simulated the global device temperature as a function of the transient time after a heavy-ion penetrating the device. Earlier studies indicated that SEB in a SiC device caused a thermal damage when the temperature exceeded the melting point of SiC (3100 K) [36]. Therefore, we chose 3000 K as the SEB failure criterion.

The VDMOS devices were investigated using electro-thermal and thermal finite-element simulations. The thermal contacts were set as temperature boundaries with an initial value 300K. When the maximum temperature exceeded the melting point of SiC (3000K) during the simulation, an SEB was confirmed [37], [38]. In previous studies [39], [40], the tilting-angle dependence of heavy-ion-induced degradation was thoroughly investigated. It was found that the ions penetrating vertically had the worst impact. However, the studies to locate the most sensitive areas to induce SEB in a VDMOS, yielded inconsistent outcomes [41]–[45]. To find the most destructive ion-strike position for SEB, three locations were selected in the conventional device: the top of the gate, the top of the JFET, and the top of the P+ source [46].

Fig. 9 shows the maximum global device temperature for the three types of devices vs. transient time. Fig. 9 (a) and Fig. 9 (b) show the C-VDMOS and SJ-VDMOS following the ion impact, with V_{DS} = 700V and LET = 0.1pC/μm. Fig. 9 (c) shows the SJ-MOD-VDMOS after ion impact. The device temperatures for the three structures increased gradually with increasing time firstly before they reached a peak value, then, the device temperature decreases. The temperature increased in the structure occurred due to the self-heating effect caused by impact ionization and multiplication of ionized carriers. The most sensitive impact position appeared to be at the top of the inversion channel for all three types devices. Hence, to compare the SEB performance for the three structures more accurately, the ion impact locations were all selected to be the most sensitive area.

Fig. 10 shows the correlation between the drain bias voltage and global device temperature at LET = 0.1 pC/μm. To compare the SEB hardening effect for the three devices more directly, we made their drift-region thicknesses equal. As shown in Fig. 10 that, the C-VDMOS and SJ-VDMOS did not differ significantly to show the same SEB effect at 800 V. This also suggested that the increase in breakdown voltage, which was caused by the super-junction structure, did not improve the SEB threshold voltage much. This result was consistent with the previous report [47].

Fig. 11 shows the distributions of the electric field abstracted at different times along the ion-track (after the ion

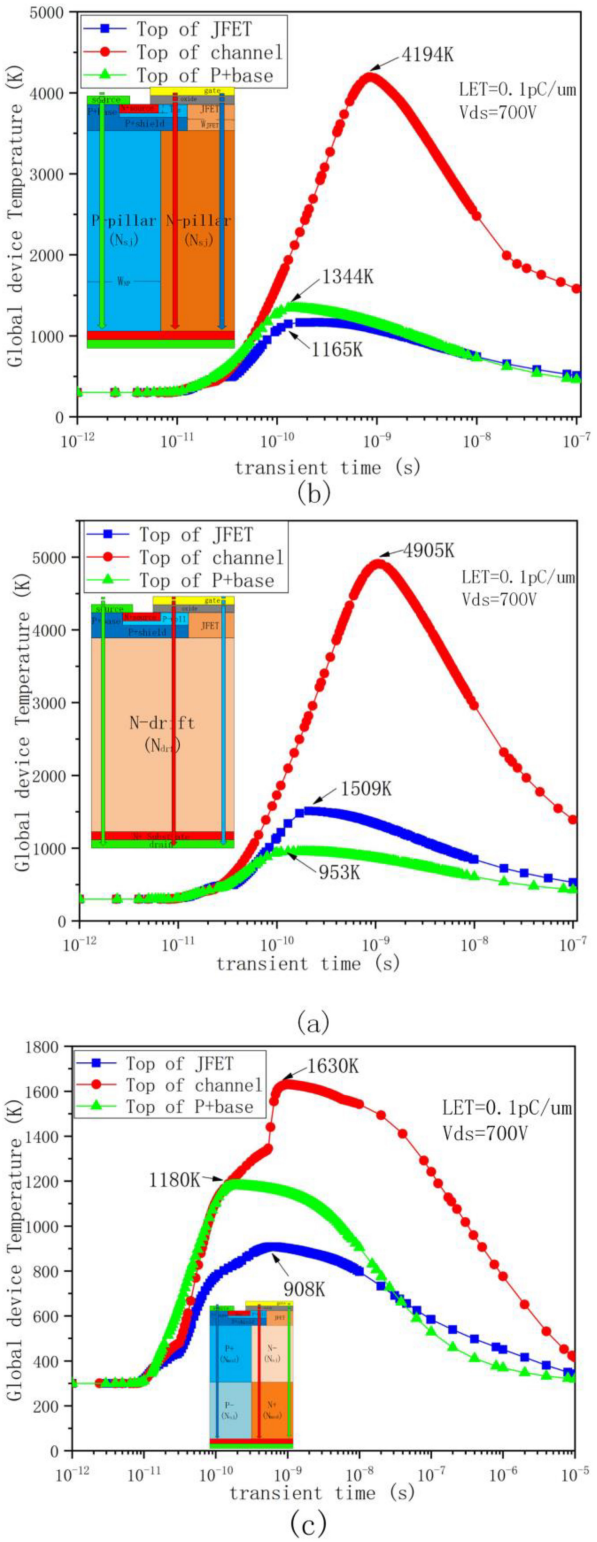

FIGURE 9. **TCAD ion simulations of MOSFETs. Shown are the global device temperatures (K) versus transient time (s), following ion-penetration at different positions, LET = 0.1pC/μm V_{DS} = 700V, for (a) C-VDMOS, (b) SJ-VDMOS, (c) SJ-MOD-VDMOS.**

strike), and the lattice temperature distributions at 1ns for the SJ-VDMOS, SJ-MOD-VDMOS and C-VDMOS devices (V_{DS} = 600V, LET = 0.1pC/μm). The kinetic energy of the

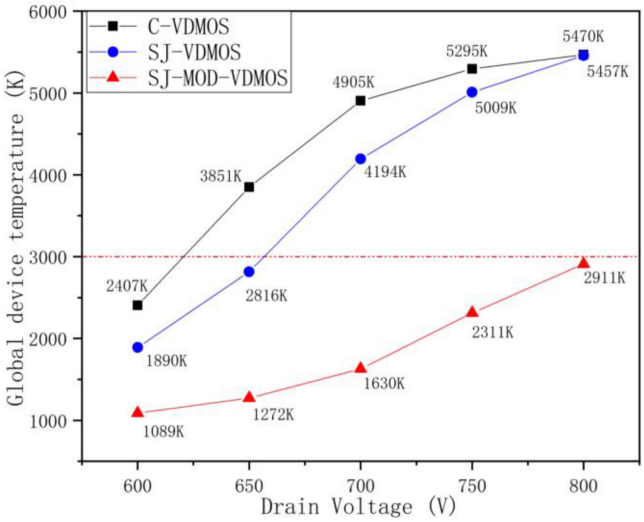

FIGURE 10. **The maximum global device temperature for the three types VDMOS following an ion penetrating under different drain bias voltages.**

heavy ions broke the covalent bonds, and many electron-hole pairs were generated along the ion trajectory [48]. The excited carriers created an extremely low-resistance path, which connected the source and drain, for a very short time. Due to the thermal effect of the current, the lattice temperature increased along the ion tracks. Local high electric fields played an important role in the generation of the high temperature. In addition, Fig. 11 also gave the high temperature areas which were approximate the local high electric field. The N−/N+ step doping-profile layer of the SJ-MOD-VDMOS acted like a buffer layer. Compared with the C-VDMOS and conventional SJ structure, the N−/N+ homojunction could transfer the electric field peak from the drift/drain homojunction quickly. As a result, the electric field peak of the SJ-MOD-VDMOS shifted to the N−/N+ homojunction already at 1ns. However, this did not occur in the SJ-VDMOS.

Fig. 12 also shows the generation rate distribution after ion impact for the SJ-VDMOS and the SJ-MOD-VDMOS at V_{DS} = 600 V. The generation rate distribution indicates that the N−/N+ homojunction decreases the impact ionization at the drift/drain junction effectively.

V. FEASIBILITY VERIFICATION

Since the N layer and N+ layer were fabricated by the substrate epitaxy, the mature SiC epitaxy technology would not cause large process errors. So, in this feasibility verification, we did not discuss the consequences of parameter changes in the N+/N− region. However, SiC groove trench filling process might have large process defects. To verify the feasibility of the process, proving that the general inaccuracy of process would not seriously affect device performance, we simulated the effect of the parameter of P+layer and P-layer region on the SEB threshold voltage.

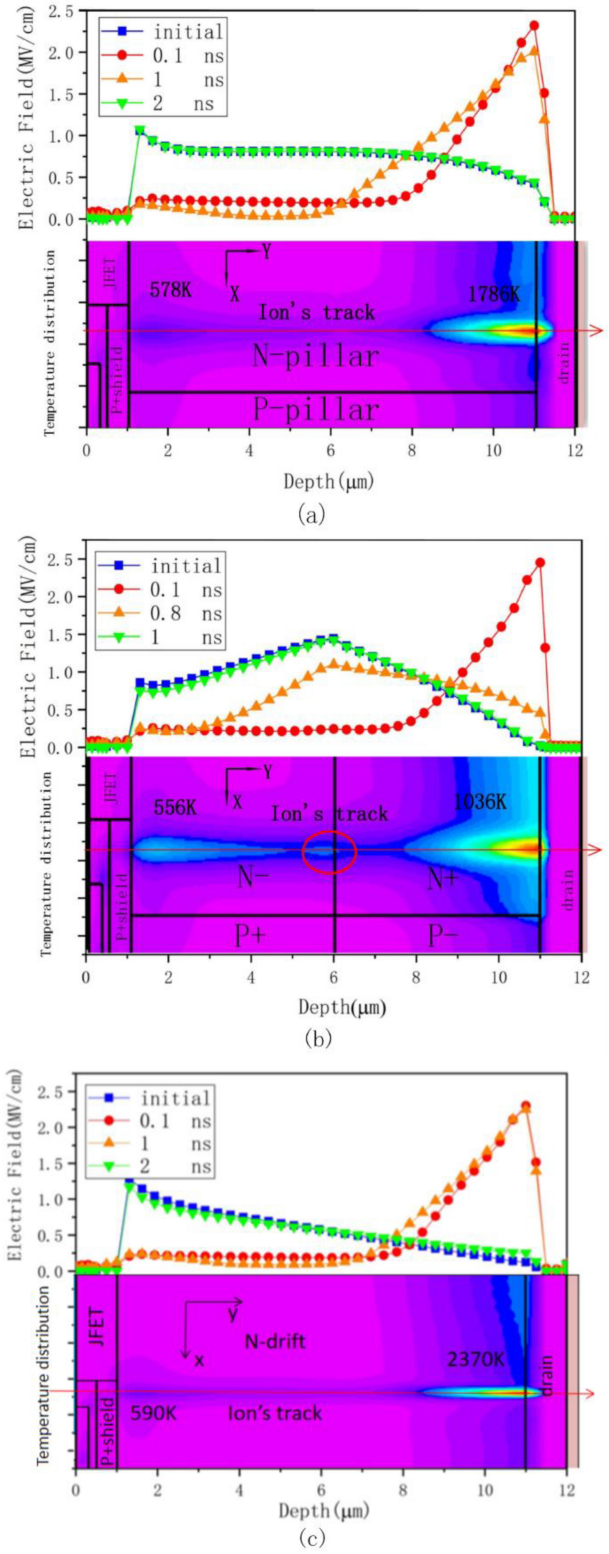

FIGURE 11. **The Electric-field distribution and temperature distribution, obtained at t = 1ns (after the ion strike); (a)SJ-VDMOS, (b)SJ-MOD-VDMOS, (c)C-VDMOS, (V_{DS} = 600V, LET = 0.1pC/μm).**

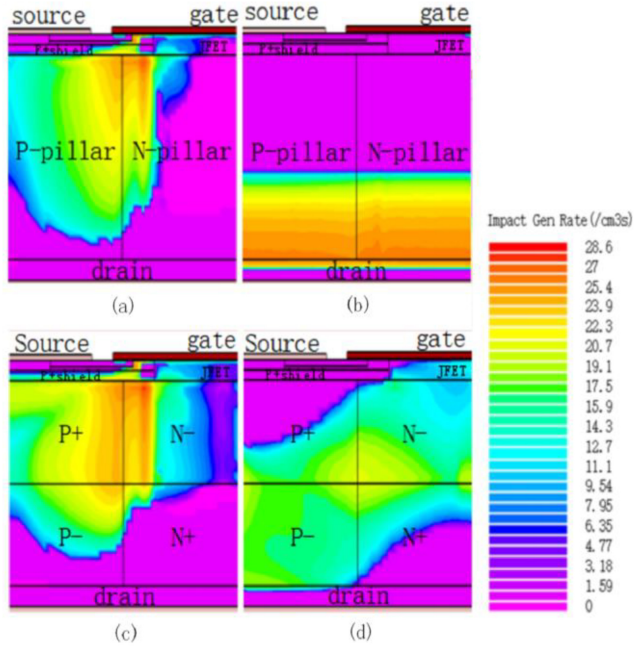

FIGURE 12. **The carrier generation-rate distribution for the SJ-VDMOS and the SJ-MOD-VDMOS at V_{DS} = 600V and LET = 0.1pC/μm: (a) and (c) with10 ps after the ion strike. (b) and (d) with10 ns after the ion strike.**

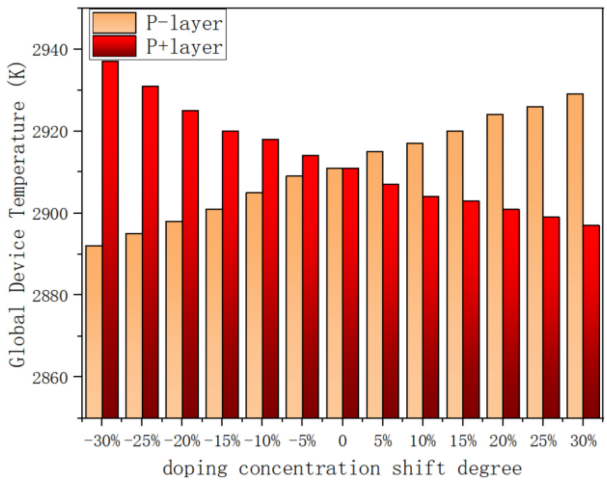

FIGURE 13. **The relationship between maximum global device temperature and the degree of doping concentration shift in P-layer and P+layer relative to optimized concentration.**

Fig. 13 shows the relationship between maximum global device temperature and the degree of doping concentration shift in P-layer and P+layer relative to the optimized concentration. As can be seen in Fig. 12, the shift of doping concentration had nearly no effect on the device SEB characteristic. As the doping concentration gap between the P+ layer and the P layer expands, the maximum global device temperature decreased, and the SEB burnout threshold slightly increased.

Fig. 14 shows the second case of non-ideal process, the relationship between the degree of P+/P− homojunction misalignment between the P+layer and the P-layer, and the global device temperature. The phenomena in Fig. 13 and Fig. 14 can be explained by the electric field distribution of

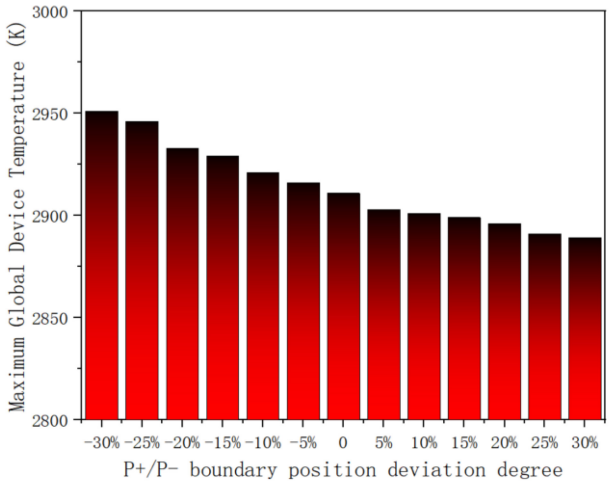

FIGURE 14. The relationship between maximum global device temperature and the degree of doping concentration shift in P-layer and P+layer relative to optimized concentration.

SJ-MOD-VDMOS. The simulation results showed that the changes in the parameters of the P+ and P− layers caused by process errors would not greatly affect the SEB characteristics of the device. This also showed that the process window for SEB performance of SJ-MOD structure was larger.

VI. CONCLUSION

In this paper, we determined that a SiC super-junction MOSFET with a step doping-profile, SJ-MOD-VDMOS, could successfully combine the benefits of both a super-junction structure and imbalanced doping. Thanks to the super-junction, the electric field peak could be further reduced, and a high BV was obtained. Furthermore, a low $R_{on,sp}$ led to a high figure of merit (FOM $= BV^2/R_{on,sp}$), which represented a good trade-off between BV and $R_{on,sp}$. Compared to the conventional super-junction VDMOS structure, the FOM of the optimized structure could be increased by 157.3%. In addition, it was found that the N−/N+ homojunction of the SJ-MOD- VDMOS could act like a buffer layer based on the SEB simulations, i.e., the critical burnout voltage of the SJ-MOD-VDMOS was 800V. On the other hand, the SEB-threshold voltage of a conventional super-junction device was only 650V which was the same as the non-hardened VDMOS structure, i.e., SJ-MOD-VDMOS demonstrated better SEB performance than the SJ-VDMOS.

REFERENCES

[1] J. A. Cooper, M. R. Melloch, R. Singh, A. Agarwal, and J. W. Palmour, "Status and prospects for SiC power MOSFETs," *IEEE Trans. Electron Devices*, vol. 49, no. 4, pp. 658–664, Apr. 2002, doi: 10.1109/16.992876.

[2] A. Elasser and T. P. Chow, "Silicon carbide benefits and advantages for power electronics circuits and systems," *Proc. IEEE*, vol. 90, no. 6, pp. 969–986, Jun. 2002, doi: 10.1109/JPROC.2002.1021562.

[3] M. Bhatnagar and B. J. Baliga, "Comparison of 6H-SiC, 3C-SiC, and Si for power devices," *IEEE Trans. Electron Devices*, vol. 40, no. 3, pp. 645–655, Mar. 1993, doi: 10.1109/16.199372.

[4] X. Li *et al.*, "A SiC power MOSFET loss model suitable for high-frequency applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8268–8276, Oct. 2017, doi: 10.1109/TIE.2017.2703910.

[5] A. Agarwal, K. Han, and B. J. Baliga, "Analysis of 1.2 kV 4H-SiC trench-gate MOSFETs with thick trench bottom oxide," in *Proc. IEEE 6th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Atlanta, GA, USA, 2018, pp. 125–129, doi: 10.1109/WiPDA.2018.8569070.

[6] K. Yao, H. Yano, and N. Iwamuro, "Investigation of UIS capability for −600V class vertical SiC p-channel MOSFET," in *Proc. 31st Int. Symp. Power Semicond. Devices ICs (ISPSD)*, Shanghai, China, 2019, pp. 187–190, doi: 10.1109/ISPSD.2019.8757607.

[7] K. Han and B. J. Baliga, "1.2-kV 4H-SiC SenseFET with monolithically integrated sensing resistor," *IEEE Electron Device Lett.*, vol. 41, no. 3, pp. 437–440, Mar. 2020, doi: 10.1109/LED.2020.2964773.

[8] X. Deng, X. Xu, X. Li, X. Li, Y. Wen, and W. Chen, "A novel SiC MOSFET embedding low barrier diode with enhanced third quadrant and switching performance," *IEEE Electron Device Lett.*, vol. 41, no. 10, pp. 1472–1475, Oct. 2020, doi: 10.1109/LED.2020.3017650.

[9] K. Li *et al.*, "A new SiC split-gate MOSFET structure with protruded P-base and the mesa above JFET for improving HF-FOM," in *Proc. 16th China Int. Forum Solid-State Lighting Int. Forum Wide Bandgap Semicond. China (SSLChina: IFWS)*, Shenzhen, China, 2019, pp. 29–32, doi: 10.1109/SSLChinaIFWS49075.2019.9019759.

[10] J. An, M. Namai, H. Yano, and N. Iwamuro, "Investigation of robustness capability of −730 V P-channel vertical SiC power MOSFET for complementary inverter applications," *IEEE Trans. Electron Devices*, vol. 64, no. 10, pp. 4219–4225, Oct. 2017, doi: 10.1109/TED.2017.2742542.

[11] Y.-Z. Cheng, Y. Wang, X. Wu, and F. Cao, "4H-SiC UMOSFET with an electric field modulation region below P-body," *IEEE Trans. Electron Devices*, vol. 67, no. 8, pp. 3298–3303, Aug. 2020, doi: 10.1109/TED.2020.3004777.

[12] S. Hu, Y. Huang, T. Liu, J. Guo, J. Wang, and J. Luo, "A comparative study of a deep-trench superjunction SiC VDMOS device," *J. Comput. Electron.*, vol. 18, pp. 553–560, Feb. 2019, doi: 10.1007/s10825-019-01318-2.

[13] M. Miura, S. Nakamura, J. Suda, T. Kimoto, and H. Matsunami, "Fabrication of SiC lateral super junction diodes with multiple stacking p- and n-layers," *IEEE Electron Device Lett.*, vol. 24, no. 5, pp. 321–323, May 2003, doi: 10.1109/LED.2003.812561.

[14] L. Yu and K. Sheng, "Modeling and optimal device design for 4H-SiC super-junction devices," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 1961–1969, Aug. 2008, doi: 10.1109/TED.2008.926648.

[15] R. Kosugi *et al.*, "First experimental demonstration of SiC super-junction (SJ) structure by multi-epitaxial growth method," in *Proc. IEEE 26th Int. Symp. Power Semicond. Devices IC's (ISPSD)*, Waikoloa, HI, USA, 2014, pp. 346–349, doi: 10.1109/ISPSD.2014.6856047.

[16] J. O. Gonzalez, R. Wu, S. Jahdi, and O. Alatise, "Performance and reliability review of 650 V and 900 V silicon and SiC devices: MOSFETs, cascode JFETs and IGBTs," *IEEE Trans. Ind. Electron.*, vol. 67, no. 9, pp. 7375–7385, Sep. 2020, doi: 10.1109/TIE.2019.2945299.

[17] M. Zerarka, P. Austin, G. Toulon, F. Morancho, H. Arbess, and J. Tasselli, "Behavioral study of single-event burnout in power devices for natural radiation environment applications," *IEEE Trans. Electron Devices*, vol. 59, no. 12, pp. 3482–3488, Dec. 2012, doi: 10.1109/TED.2012.2222889.

[18] Y. Yoshiura *et al.*, "Simple simulation approach for the first trigger step of SEB (single event burn-out) based upon physical analysis for Si high voltage bipolar device," in *Proc. 28th Int. Symp. Power Semicond. Devices ICs (ISPSD)*, Prague, Czech Republic, 2016, pp. 315–318, doi: 10.1109/ISPSD.2016.7520841.

[19] E. Mizuta, S. Kuboyama, H. Abe, Y. Iwata, and T. Tamura, "Investigation of single-event damages on silicon carbide (SiC) power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 4, pp. 1924–1928, Aug. 2014, doi: 10.1109/TNS.2014.2336911.

[20] P. Vudumula and S. Kotamraju, "Design and optimization of SiC super-junction MOSFET using vertical variation doping profile," *IEEE Trans. Electron Devices*, vol. 66, no. 3, pp. 1402–1408, Mar. 2019, doi: 10.1109/TED.2019.2894650.

[21] Z. Lin, H. Huang, and X. Chen, "An improved superjunction structure with variation vertical doping profile," *IEEE Trans. Electron Devices*, vol. 62, no. 1, pp. 228–231, Jan. 2015, doi: 10.1109/TED.2014.2372819.

[22] C. Wang, J. Bu, L. Song, C. Zeng, Z. Han, and J. Luo, "A simulation model for power VDMOS," in *Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits (EDSSC)*, Xi'an, China, 2019, pp. 1–3, doi: 10.1109/EDSSC.2019.8754237.

[23] L. Zhang, H. Yu, Y. Wu, Z. Yang, and J. Zhu, "On state output characteristics and transconductance analysis of high voltage (600V) SJ-VDMOS," in *Proc. IEEE 11th Int. Conf. Solid-State Integr. Circuit Technol.*, Xi'an, China, 2012, pp. 1–3, doi: 10.1109/ICSICT.2012.6466711.

[24] X. Zhong, B. Wang, J. Wang, and K. Sheng, "Experimental demonstration and analysis of a 1.35kV 0.92mΩ·cm^2 SiC superjunction schottky diode," *IEEE Trans. Electron Devices*, vol. 65, no. 4, pp. 1458–1465, Apr. 2018, doi: 10.1109/TED.2018.2809475.

[25] S. Harada *et al.*, "First demonstration of dynamic characteristics for SiC superjunction MOSFET realized using multi-epitaxial growth method," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2018, pp. 1–4, doi: 10.1109/IEDM.2018.8614670.

[26] *ATLAS User's Manual: Device Simulation Software*, Silvaco, Santa Clara, CA, USA, 2008.

[27] G. H. Johnson, J. M. Palau, C. Dachs, K. F. Galloway, and R. D. Schrimpf, "A review of the techniques used for modeling single-event effects in power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 43, no. 2, pp. 546–560, Apr. 1996, doi: 10.1109/23.490900.

[28] J. Wang *et al.*, "Characterization, modeling, and application of 10-kV SiC MOSFET," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 1798–1806, Aug. 2008, doi: 10.1109/TED.2008.926650.

[29] M. Roschke and F. Schwierz, "Electron mobility models for 4H, 6H, and 3C SiC [MESFETs]," *IEEE Trans. Electron Devices*, vol. 48, no. 7, pp. 1442–1447, Jul. 2001, doi: 10.1109/16.930664.

[30] A. K. Agarwal, S. Seshadri, and L. B. Rowland, "Temperature dependence of Fowler–Nordheim current in 6H- and 4H-SiC MOS capacitors," *IEEE Electron Device Lett.*, vol. 18, no. 12, pp. 592–594, Dec. 1997, doi: 10.1109/55.644081.

[31] H. Yano, T. Hirao, T. Kimoto, H. Matsunami, K. Asano, and Y. Sugawara, "High channel mobility in inversion layers of 4H-SiC MOSFETs by utilizing (112∼0) face," *IEEE Electron Device Lett.*, vol. 20, no. 12, pp. 611–613, Dec. 1999, doi: 10.1109/55.806101.

[32] H. Niwa, J. Suda, and T. Kimoto, "Impact ionization coefficients in 4H-SiC toward ultrahigh-voltage power devices," *IEEE Trans. Electron Devices*, vol. 62, no. 10, pp. 3326–3333, Oct. 2015, doi: 10.1109/TED.2015.2466445.

[33] R. Raghunathan and B. J. Baliga, "Measurement of electron and hole impact ionization coefficients for SiC," in *Proc. 9th Int. Symp. Power Semicond. Devices IC's*, Weimar, Germany, 1997, pp. 173–176, doi: 10.1109/ISPSD.1997.601463.

[34] D. Stefanakis, X. Chi, T. Maeda, M. Kaneko, and T. Kimoto, "Experimental determination of impact ionization coefficients along <1120> in 4H-SiC," *IEEE Trans. Electron Devices*, vol. 67, no. 9, pp. 3740–3744, Sep. 2020, doi: 10.1109/TED.2020.3012118.

[35] N. Gupta and A. Naugarhiya, "1.4kV planar gate superjunction IGBT with stepped doping profile in drift and collector region," *Silicon*, vol. 13, pp. 697–706, Apr. 2020. [Online]. Available: https://doi.org/10.1007/s12633-020-00456-8

[36] C. Abbate *et al.*, "Thermal damage in SiC Schottky diodes induced by SE heavy ions," *Microelectron. Rel.*, vol. 54, nos. 9–10, pp. 2200–2206, Aug. 2014.

[37] C.-H. Yu, Y. Wang, F. Cao, L.-L. Huang, and Y.-Y. Wang, "Research of single-event burnout in power planar VDMOSFETs by localized carrier lifetime control," *IEEE Trans. Electron Devices*, vol. 62, no. 1, pp. 143–148, Jan. 2015, doi: 10.1109/TED.2014.2365817.

[38] A. F. Witulski *et al.*, "Single-event burnout of SiC junction barrier Schottky diode high-voltage power devices," *IEEE Trans. Nucl. Sci.*, vol. 65, no. 1, pp. 256–261, Jan. 2018, doi: 10.1109/TNS.2017.2782227.

[39] A. Javanainen *et al.*, "Incident angle effect on heavy ion induced reverse leakage current in SiC Schottky diodes," in *Proc. 16th Eur. Conf. Radiat. Effects Compon. Syst. (RADECS)*, Bremen, Germany, 2016, pp. 1–4, doi: 10.1109/RADECS.2016.8093100.

[40] A. Javanainen *et al.*, "Heavy-ion-induced degradation in SiC Schottky diodes: Incident angle and energy deposition dependence," *IEEE Trans. Nucl. Sci.*, vol. 64, no. 8, pp. 2031–2037, Aug. 2017, doi: 10.1109/TNS.2017.2717045.

[41] Q. Li *et al.*, "Study on single-event burnout of SiC VDMOSFET: Failure mechanism and influence factors," in *Proc. 20th Int. Conf. Electron. Packag. Technol. (ICEPT)*, Hong Kong, 2019, pp. 1–5, doi: 10.1109/ICEPT47577.2019.245733.

[42] X. Zhou, Y. Jia, D. Hu, and Y. Wu, "A simulation-based comparison between Si and SiC MOSFETs on single-event burnout susceptibility," *IEEE Trans. Electron Devices*, vol. 66, no. 6, pp. 2551–2556, Jun. 2019, doi: 10.1109/TED.2019.2908970.

[43] A. F. Witulski *et al.*, "Single-event burnout mechanisms in SiC power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 65, no. 8, pp. 1951–1955, Aug. 2018, doi: 10.1109/TNS.2018.2849405.

[44] D. R. Ball *et al.*, "Estimating terrestrial neutron-induced SEB cross sections and FIT rates for high-voltage SiC power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 66, no. 1, pp. 337–343, Jan. 2019, doi: 10.1109/TNS.2018.2885734.

[45] J. Lu *et al.*, "Impact of varied buffer layer designs on single-event response of 1.2-kV SiC power MOSFETs," *IEEE Trans. Electron Devices*, vol. 67, no. 9, pp. 3698–3704, Sep. 2020, doi: 10.1109/TED.2020.3008398.

[46] M. Allenspach *et al.*, "SEGR and SEB in n-channel power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 43, no. 6, pp. 2927–2931, Dec. 1996.

[47] N. Ikeda, S. Kuboyama, and S. Matsuda, "Single-event burnout of Super-junction power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3332–3335, Dec. 2004, doi: 10.1109/TNS.2004.839511.

[48] D. R. Ball *et al.*, "Ion-induced energy pulse mechanism for single-event burnout in high-voltage SiC power MOSFETs and junction barrier Schottky diodes," *IEEE Trans. Nucl. Sci.*, vol. 67, no. 1, pp. 22–28, Jan. 2020, doi: 10.1109/TNS.2019.2955922.