Received 15 May 2021; revised 25 September 2021; accepted 24 October 2021. Date of publication 29 October 2021; date of current version 9 November 2021.
The review of this article was arranged by Editor S. Chakrabarti.

Digital Object Identifier 10.1109/JEDS.2021.3123978

Gate Oxide and Implantation Process Co-Optimization for Low-Power MCU Applications

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This work was supported in part by the Science and Technology Commission of Shanghai Municipality under Grant 21DZ1100700 and Grant 20501130202, and in part by the NSFC under Grant 61904033.

ABSTRACT The fast development in microcontroller unit (MCU) technology has urged continuous decreasing in power consumption by different assignment of operating status among devices. In this work, we focused on the ultra-high Vth (UHVT) transistor and used gate oxide thickness and Vth implantation co-optimization to minimize the gate leakage current towards low-power MCU applications. Based on the 55 nm node, it has been found both theoretically and experimentally that the leakage level has been significantly reduced at different temperature in n-FET, p-FET, data flip-flop (DFF) and inverter (INV). Upon MCU testing under active, sleep and deep sleep modes, obvious decrease in the power consumption is also achieved, providing a promising optimization approach towards a better balance between the speed and power in modern MCU technology.

INDEX TERMS MCU, gate oxide, static power consumption, gate leakage.

I. INTRODUCTION

With the emerging technologies in Internet-of-Things (IOT) and artificial intelligence, there is a growing demand for the high-performance microcontroller unit (MCU), which integrates central processing unit (CPU), memory, digital, analog, input/output and other components for signal and data processing. However, the development of MCU technology has been largely bottlenecked by the power consumption which can be hardly further reduced in advanced fabrication technology nodes [1]–[3]. In general, the power consumption in MCU is minimized through distributing different status like active, sleep and deep sleep modes in analog, digital, memory and input/output (I/O) components according to different circuit functions [4]. For example, in active mode, all the circuits are activated providing boosted system frequency for CPU function. In sleep mode, the CPU as well as the memory and cyclic redundancy check (CRC) circuits will be turned off to decrease the power consumption, while the high-speed clock will be further turned off in deep sleep mode. Thus, the power consumption consists of static and dynamic power consumptions, which are originated from the power during standby and operation status, respectively [5]–[7]. Fig. 1(a) shows the MCU power consumption percentage of analog, digital, memory and I/O components under active, sleep and deep sleep modes. It is clear that the dynamic power consumption in digital circuit under active mode occupies almost half of the total power consumption, and ~70% of the power consumption is from the analog circuit in sleep mode. Over 80% of the power is consumed by digital circuit in deep sleep mode which is the common state for most devices in a low-power system.

Considering the fact that transistors with different Vth levels are incorporated in building the digital circuits, an optimized balance between the performance and leakage can be achieved by properly assigning FET with higher Vth for better leakage and lower Vth for better performance [8]–[10]. The leakage current level dominated by the channel and gate leakage current under turn-off state further determines the static power consumption [11]–[13]. Fig. 1(b) shows the dynamic and static power consumption of a 10W logic gate digital circuit in MCU when using devices of UHVT, high Vth (HVT) and regular Vth (RVT) FETs with different Vth.

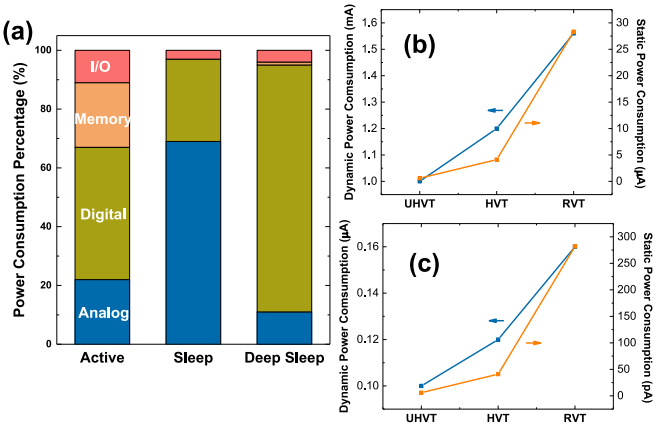

FIGURE 1. (a) The MCU power consumption percentage of analog, digital, memory and I/O components under active, sleep and deep sleep modes. (b) The dynamic and static power consumption of the digital circuit using UHVT, HVT and RVT devices, respectively. (c) Comparison of dynamic and static power consumption of individual device of UHVT, HVT and RVT FETs with 2 μm channel length and 0.06 μm channel width.

Fig. 1(c) shows the dynamic and static power consumption of individual FET device with different Vth. The device channel length is 2 μm and the channel width is 0.06 μm. Using lower Vth devices, the power consumption will be greatly increased. This is also the major reason that HVT and RVT are largely used in the design of low-power digital circuit design [14]. However, although adjusting the doping concentration can control the channel leakage in HVT (or UHVT) devices, it is difficult to suppress the gate leakage which increases with thinner gate oxide and higher lightly doped drain (LDD) concentration. Thus, effective and efficient approaches balancing Vth level and leakage current is highly desired towards low-power device and system applications.

In this work, we propose and study the process and device engineering to improve the gate leakage in UHVT devices while maintaining a stable Vth level through gate oxide thickness and LDD doping concentration co-optimization. Both simulated and experimental work have confirmed the reduced leakage current in n-type and p-type devices. Practical MCU testing further confirms the improvement in system performance under various operation modes upon the optimization method.

II. EXPERIMENTAL DETAILS

The front-end process to fabricate CMOS dual-well include layer-zero align, shallow trench isolation (STI), well definition, gate formation, LDD, oxide-nitride-oxide (ONO) sidewall protection and the formation of source/drain. The threshold voltage of the device is largely determined by the well definition and gate formation steps. The well definition involves with the well, channel and Vth implantation, and the gate oxide thickness in the gate formation step significantly influences the device performance like the driving capability, speed, frequency property and reliability. Implantation dose is used to adjust the Vth value while the gate oxide thickness offers an alternative approach to optimize the Vth as well.

The devices are fabricated based on a same dimensional feature but with different channel doping concentration for various Vth level. In the original 55 nm logic process, the doping concentrations of NMOS and PMOS devices of UHVT are 1.3×10^{13} cm^{-3} and 1.76×10^{13} cm^{-3}, respectively. The doping concentration of NMOS and PMOS devices of HVT is 0.94×10^{13} cm^{-3} and 1.32×10^{13} cm^{-3}, respectively. In our work, we have increased the gate oxide thickness by 2 Å (from 26 Å to 28 Å) to optimize the leakage property of the device performance. Meanwhile, the doping concentration during the well definition step is also lowered by 0.1×10^{13} cm^{-3} accordingly, in order to adjust the Vth value of the engineered UHVT device to the same level of the standard HVT device for a comparable device performance [15]–[18].

The INV and DFF standard cells are selected from the library following the baseline 0.2 μm-track to construct the 6T structure, and the width is 0.6 μm and 5.2 μm for the INV and DFF, respectively [19], [20].

III. RESULTS AND DISCUSSION

It is known that Vth is determined by the fabrication materials, oxide thickness (t_{ox}), channel implantation and substrate bias, and can be described by the following equations:

$$V_{th} \approx V_{FB} + \varphi_s + \sqrt{2\varepsilon_{si} q N_A (\varphi_s + V_{BS})}/C_{ox} \quad (1)$$

$$V_{FB} = \varphi_{ms} - (Q_f + Q_m + Q_{ot})/C_{ox} \quad (2)$$

where V_{FB} is the flat-band voltage, φ_s is the surface potential, q is the electron charge, N_A is the doping concentration, φ_{ms} is potential difference, Q_f is the fixed charge in oxide layer, Q_m is the mobile ionic charge, Q_{ot} is the oxide trapped charge. The gate leakage current I_{GIDL} is due to the electron tunneling under the field in the gate/drain overlap. Under low electric field, the tunneling is assisted by the thermal excitation while the direct tunneling occurs under high electric field. Thus, t_{ox} and LDD concentration are the two major factors affecting the leakage level as mentioned above [16], [21]–[22].

We studied the electrical performance of the UHVT devices by optimizing t_{ox} and doping concentration, and compared it to the performance of the standard HVT device. We have used the Sentaurus technology computer aided design (TCAD) tools to simulate the device structure and I-V characteristics by setting the typical parameters of transistors such as Wmin = 0.12/0.15 μm, Lmin = 0.06 μm, t_{ox} = 26 Å, C_{ox} = 13.27 fF/μm which are used as reference data for the analysis of fabricated device performance. The inset of Fig. 2(a) shows the simulated NMOS and PMOS devices by TCAD. The channel length follows the 55 nm technology platform, and t_{ox} and doping concentration are adjusted according to the process optimizations. Fig. 2 shows the simulated and experimental results of the output and

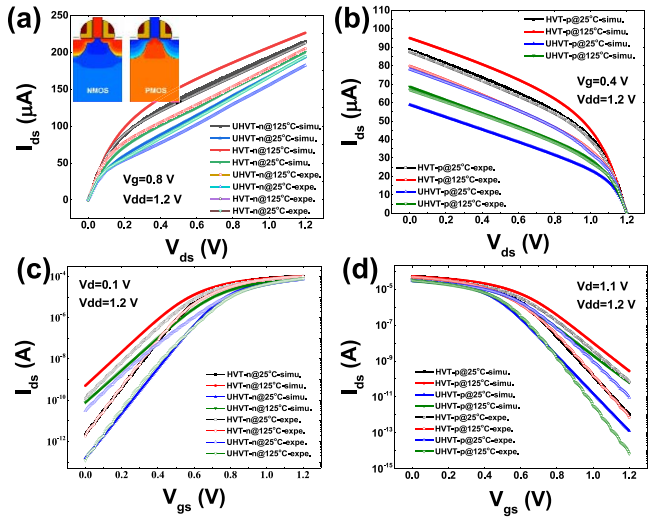

FIGURE 2. Simulated and experimental (a) I_{ds}-V_{ds} and (b) I_{ds}-V_{gs} curves of our optimized n-type UHVT FETs and the standard HVT devices at 25 °C and 125 °C. Simulated and experimental (c) I_{ds}-V_{ds} and (d) I_{ds}-V_{gs} curves of our optimized p-type UHVT FETs and the standard HVT devices at 25 °C and 125 °C.

TABLE 1. Simulated and experimental Vth values of UHVT and HVT devices.

Vth (V)		Simulation				Experimental			
		Vds=0.1 V		Vds=1.2 V		Vds=0.1 V		Vds=1.2 V	
		25°C	125°C	25°C	125°C	25°C	125°C	25°C	125°C
pFET	HVT	0.461	0.46	0.311	0.31	0.37	0.329	0.215	0.179
	UHVT	0.563	0.555	0.474	0.47	0.425	0.425	0.32	0.336
nFET	HVT	0.42	0.41	0.264	0.26	0.34	0.288	0.175	0.132
	UHVT	0.54	0.535	0.396	0.4	0.44	0.402	0.28	0.264

transfer characteristics of the engineered UHVT and standard HVT devices under different temperature. It is noted that the threshold voltage of the UHVT devices have been adjusted by implantation optimization after increasing t_{ox} in order to achieve a comparable Vth value to that of the HVT references and dynamic current characteristics. Table lists and compares the extracted Vth values of the UHVT and HVT devices under different V_{ds} bias and different temperature.

By comparing the results in Table 1, it is clear that by decreasing the doping concentration, the Vth values of both n-type and n-type UHVT devices have been successfully lowered to the same level of the standard HVT devices. This ensures the practical circuit application of the engineered UHVT devices as well as the optimized process. On the other hand, increasing the gate oxide thickness can be expected to significantly lower the leakage current level by presenting a barrier with larger width. We have also extracted the simulated and experimental leakage characteristics of all devices shown in Fig. 2, and the results are shown in Table 2. It is clear that the leakage current level for both n-type and n-type UHVT devices have been greatly lowered with over 10 times smaller at 125°C and ~50 times smaller at room temperature. It should be noted that, the difference observed by comparing the simulated and experimental data is largely due to the process fluctuation of channel doping. In order to

TABLE 2. Simulated and experimental leakage current values of UHVT and HVT devices.

Leakage Current [pA]		Simulation		Experimental	
		25°C	125°C	25°C	125°C
pFET	HVT	38.4	3772	89.74	1478
	UHVT	0.8667	253.3	0.3025	69.25
nFET	HVT	113.4	8182	102.8	3070
	UHVT	4.344	777.6	4.773	492.6

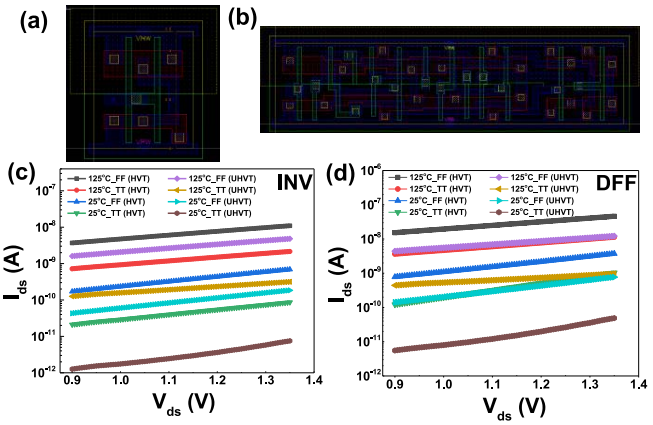

FIGURE 3. Layout of (a) INV and (b) DFF designs. Leakage current level of (c) INV and (d) DFF under different testing conditions.

tune the threshold voltage of the device to a similar level of HVT for optimum response speed of digital circuit, the channel doping concentration is adjusted after increasing the gate oxide thickness. This can lead to process variations in practical implantation step with deviations from the simulated results.

We have further designed and fabricated DFF and inverter logics implementing the optimized UHVT and standard HVT devices for comparative study. Figs. 3(a) and 3(b) show the layout of the INV and DFF, respectively. Focusing on the leakage current level, the INV based on UHVT FETs have shown significantly decreased leakage as compared to that using HVT devices at room temperature as shown in Fig. 3(c) (73.9% under 1.2V_FF and 93.5% under 1.2V_TT). At elevated temperature of 125°C, the leakage level of INV with UHVT is 56.0% lower under 1.2V_FF and 84.4% lower under 1.2V_TT than that of the INV with HVT devices. Similar results have also been observed for the DFF circuits (Fig. 3(d)), with 80.3% under 1.2V_FF and 96.2% under 1.2V_TT at 25°C, and 72.9% under 1.2V_FF and 90.5% under 1.2V_TT at 125°C.

Based on the results shown above, we have tested the electrical performance of MCU under external clock signal with 4M frequency at room temperature. Fig. 4 shows the power-on and power-off process of the MCU and the 4M clock output signal with stable system power under −40°C, 25°C and 85°C temperature.

(1) With active mode, the power consumption is 540~660 μA, which is 23% lower than similar products. With higher frequency of 24M, the power consumption is

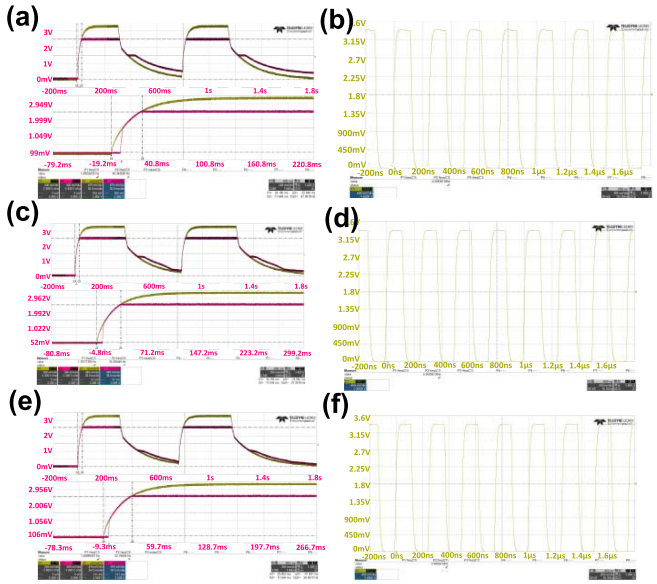

FIGURE 4. **(a) The upper panel shows the test result of power-on and power-off process at −40°C. The yellow curve is the source power signal VDD50 and the red curve is 2.5 V LDO output voltage. With VDD50 < 2.5 V, VCAP well follows the source voltage level, and VCAP is stabilized at 2.5 V with VDD50 > 2.5 V. The lower panel shows the zoomed-in curves. (b) Test results of high-speed 4∼24 MHz oscillator under 3.3 V source power at −40°C. The clock output frequency is 4 MHz. Similar test results obtained at (c)-(d) 25°C and (e)-(f) 85°C.**

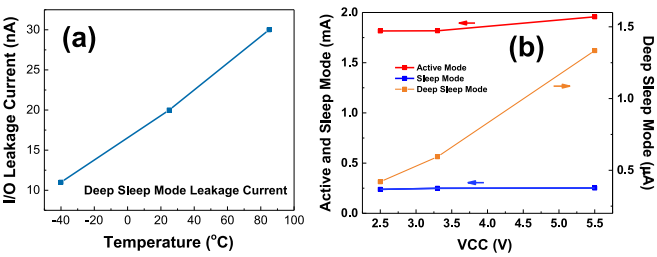

FIGURE 5. **(a) I/O leakage currents tested at different temperature of −40°C, 25°C and 85°C. (b) Power consumptions of active, sleep and deep sleep modes under different VCC power supply conditions of 2.5 V, 3.3 V and 5.5 V.**

still 18% lower. If we test using internal clock, the power consumption is 18% lower for both 4M and 24M frequency.

(2) With sleep mode, the power consumption is 210∼240 μA, which is 14% lower than similar products. The power consumption is 15% lower under 24M frequency. The values are 22% and 19% for 4M and 24M frequency, respectively when using internal clock.

(3) With deep sleep mode, the power consumption can be lowered by 11%∼18.3% within −40∼25°C temperature range, and it can be saved by 14.6%∼21.05% and 10%∼13.33% at 50°C and 85°C, respectively.

In addition, the I/O leakage current tested at −40°C, 25°C and 85°C are 11 nA, 20 nA and 30 nA (Fig. 5(a)), respectively. We have also calculated and compared the power consumption of the MCU under different VCC power supply conditions of 2.5 V, 3.3 V and 5.5 V. The results are illustrated in Fig. 5(b), which are sufficiently small towards low-power applications.

IV. CONCLUSION

To summarize, we have studied the optimization techniques to lower the power consumption in UHVT FET devices focusing on the gate oxide thickness and Vth implantation process. By increasing the gate oxide thickness (from 26 Å to 28 Å) with lowered channel doping concentration (by 0.1×10^{13} cm^{-3}), the leakage current level has been successfully suppressed with optimized threshold voltage. Both simulated and experimental results have shown that n-type and p-type devices employing the engineered UHVT devices exhibit much lower leakage current. Such optimizations have been further utilized in the synthesis of INV and DFF logics as well as MCU testing under different electrical and environmental conditions. Excellent performance improvement is achieved based on the proposed optimization methods shown in this work, which has provided a promising pathway towards low-power MCU applications.

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