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Capacitance Analysis of Transient Behavior Improved Metal-Insulator-Semiconductor Tunnel Diodes With Ultra Thin Metal Surrounded Gate

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ABSTRACT The metal-insulator-semiconductor tunnel diodes with ultra thin metal surrounded gate (UTMSG) have been found to have improved transient current behavior, and the improvement is proportional to the area of the surrounding gate. The resistance induced by the thin metal gate leads to delay of inversion carriers under the surrounding gate. At the same time, the UTMSG devices could read the capacitance under the surrounding gate only in inversion regime, but not in accumulation and depletion regime. This could be explained by a proposed small signal circuit model. The large resistance within the metal gate blocks the AC signal coming from the surrounding gate. On the other hand, the increased inversion carrier density introduces an inversion channel, which will let the AC signal pass through. The successful reproduction of the experimental observed unusual capacitance-voltage characteristics by TCAD simulation proves the proposed model as well. Detailed simulations are implemented by varying different parameters to give a further understanding of the UTMSG device. A rough estimation of the resistance of the inversion channel is also given. The calculation shows the consistency with the proposed small signal circuit model. The UTMSG device could experience a larger change of magnitude of capacitance and hence a larger capacitance window when switching from 1 V to −0.3 V, verified by simulation. The simulation has also shown that the edge thickened oxide will only slightly modulate the capacitance of the UTMSG devices.

INDEX TERMS Metal-insulator-semiconductor (MIS) tunnel diodes, transient characteristics, capacitance analysis.

I. INTRODUCTION

The devices with ultra thin dielectric become more important as the continuous scaling of the modern integrated circuit fabrication. The metal-insulator-semiconductor (MIS) tunnel diodes has already shown their application, such as temperature and strain sensors [1], [2], photodetector [3] and solar cells as well [4]. At the same time, thanks for the ultra thin dielectric, MIS tunnel diodes have a good ability to store more charges as capacitors. This is helpful when implemented as the one-transistor dynamic random access memory (1T DRAM), which reads transient current as the memory states [5], [6].

The lateral non-uniformity has also been found to enhance the transient behavior, using the ultra thin metal surrounded gate (UTMSG) in the Al/SiO_2/Si(p) tunnel diodes [7], [8]. Figs. 1(a) and (b) show the schematic top view and cross section of the UTMSG device. The thick aluminum center gate was first deposited during the fabrication, and a layer of Al_2O_3 with thickness of several nanometers will naturally formed on sidewall during the wet etching process of the

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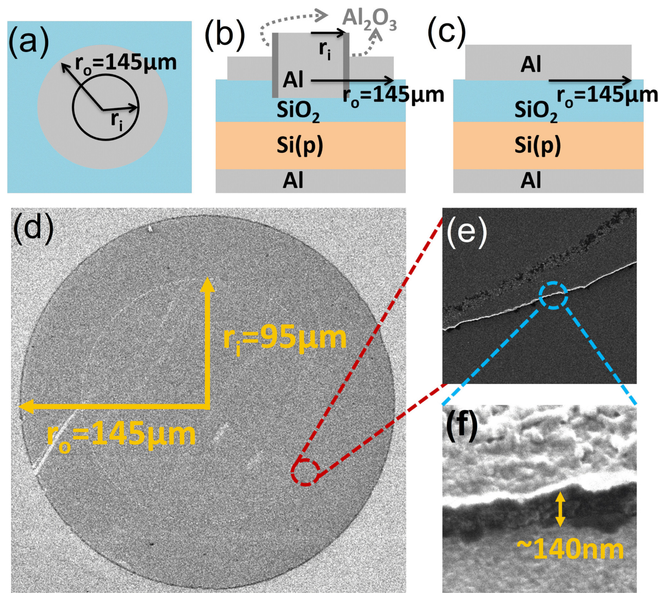

FIGURE 1. Schematic (a) top view and (b) cross section of the UTMSG device with edge thickened oxide. The aluminum oxide formed on the sidewall of the thick metal center gate causes a large resistance connecting to the ultra thin metal surrounding gate. (c) Cross section of the planar device. Both UTMSG and planar devices have a total gate radius of 145 µm. (d) Top view of the whole UTMSG device, (e) enlarged top view of the boundary of thick and thin metal gates, and (f) the boundary of thick and thin metal gates with a viewing angle of 45°, all photographed by He beam.

center gate. This results in a tunneling resistance between the center gate and the surrounding gate. At the same time, the thin aluminum film with thickness of around only 10 nm will be relative resistive, since the average grain size decreases as the film thickness decreases, causing an increased density of grain boundaries which would scatter the carrier transport [9], [10]. These two would cause a delay of signal transmission, which could be understood by the effect of a large resistance. As a consequence, inversion carriers under the surrounding gate would be delayed due to the induced large resistance, and this is the basic idea of the UTMSG device. In this report, the discussion will be focused on the unusual capacitance behavior of the UTMSG device with the planar device shown in Fig. 1(c) as comparison. The understanding of the behavior of the UTMSG devices under AC small signal will pave the way to the fully comprehension of transient behavior.

II. EXPERIMENTAL

A boron-doped p-type (100)-oriented silicon wafer with a resistivity of 1-10 Ω-cm was used as the substrate. After standard Radio Cooperation of America (RCA) cleaning, SiO_2 layer with thickness of 26-33Å was grown by anodic oxidation (ANO) in deionized water at room temperature [11], followed by performing rapid thermal annealing (RTA) under 20 torr N_2 at 950 °C for 15 s. The UTMSG device was then patterned by lithography to define the center region with different radii from 85 µm to 115 µm. Another SiO_2 layer with thickness around 3 Å was grown on UTMSG device by ANO to thicken the oxide under the surrounding gate followed by RTA again. The edge thickened oxide has been found useful to reduce the offsetting leakage current of the MIS tunnel diodes when reading the transient current [12], since the tunneling effect is most intense at edge as a result of the fringing field effect [13]. Afterwards, 140 nm Al films were evaporated and patterned by lithography to define the center gate with radii from 85 µm to 115 µm for UTMSG device, and the gate for planar device with radius of 145 µm. Mixture of dilute nitric acid and dilute phosphoric acid was used for the wet etching process of aluminum gate. Once aluminum was exposed to nitric acid, aluminum was oxidized from the surface with a depth of several nanometers, and phosphoric acid etched the aluminum oxide subsequently. Noted that there would be aluminum oxide remaining on the sidewall of the center gate of the UTMSG devices, since phosphoric acid could not be able to fully etch the aluminum oxide during the wet etching process [14], [15]. Ultra thin Al layer of 10 nm was then evaporated and patterned to define the total gate of the UTMSG device, with a raidus of 145 µm. Finally, after removing back native oxide using buffered oxide etchant (BOE), 140 nm Al films were evaporated on the back side of both devices as the back contacts. Fig. 1(d) shows the top view of the UTMSG device with $r_i = 95$ µm and $r_o = 145$ µm, photographed by He beam. The boundary between the center gate and the surrounding gate could be clearly observed in the enlarged top view in Fig. 1(e). The He beam photograph of this boundary with a viewing angle of 45° in Fig. 1(f) shows that the height difference is around 140 nm. Agilent B1500A semiconductor device analyzer was used for measurement.

III. RESULTS AND DISCUSSION

Fig. 2 (a) shows the current-voltage (I-V) characteristics of the planar device and the UTMSG devices with various r_i, all having the same effective oxide thickness (d_{eff}), which is fitted by the current at −1.8 V. With a sweeping rate of 0.1 V/s, the UTMSG devices have larger displacement currents at 0 V compared to the planar device, implying better transient behaviors when using the transient current reading at 0 V for the memory usage. When the devices switch to 0 V from a positive bias, the inversion carriers will be gradually recombined, leading to a negative discharging current for the gate. At the same time, there will be positive tunneling current from the gate to the silicon, offsetting the negative read current. Since the UTMSG devices have lower saturation currents compared to the planar device, the leakage current will be reduced when reading the transient current. Fig. 2(b) shows the read currents at 0 V with the inset illustrating the voltage setting. The UTMSG devices achieve great improvement, and the magnitude of the read current increases with smaller r_i. This is because a smaller r_i means a larger area of surrounding gate and more inversion carriers under the surrounding gate are delayed, leading to a more negative discharging current. Consequently, larger magnitude

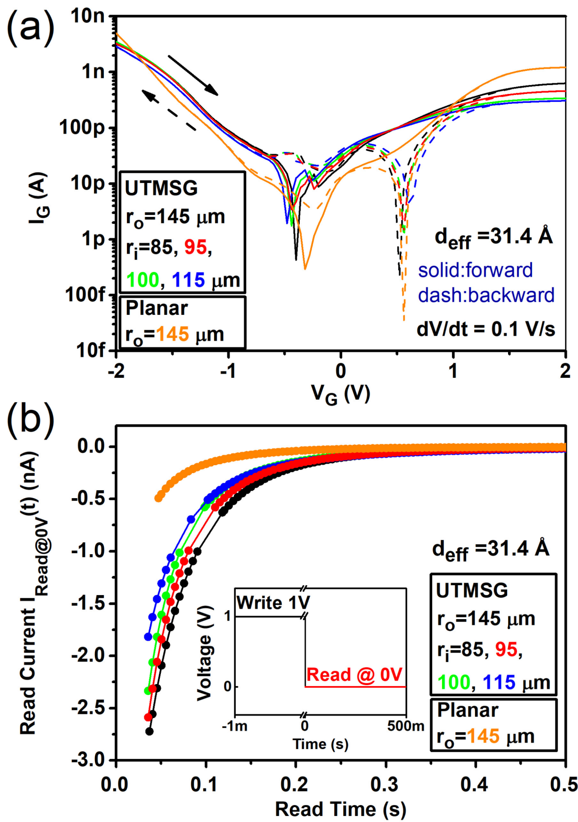

FIGURE 2. (a) Current-voltage characteristics and (b) transient read current at 0 V of the planar device and the UTMSG devices with the same oxide thickness but various r_i. The inset in (b) shows the gate voltage program.

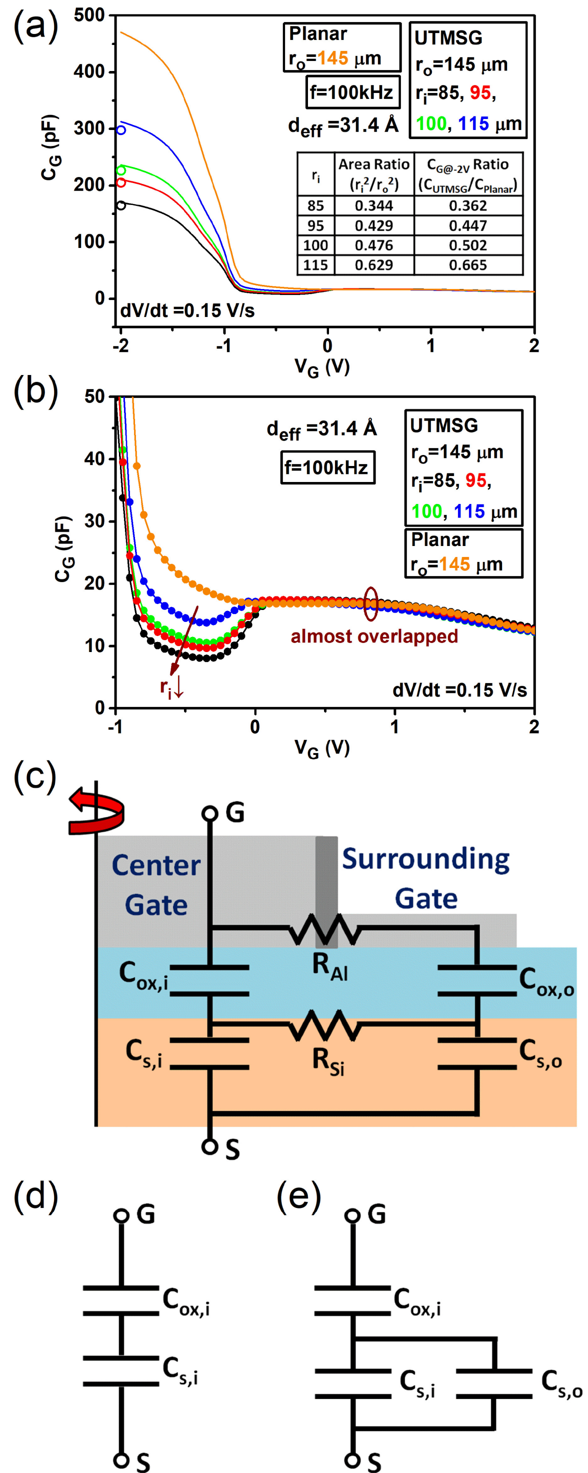

FIGURE 3. (a) High-frequency 100 kHz capacitance-voltage (C-V) characteristics of the UTMSG and planar devices. The circle points are calculated by the capacitance of the planar device at −2 V times the area ratio. (b) The enlarged C-V curves. (c) A proposed small signal model of the UTMSG device. The reduced small signal model when the UTMSG device is in (d) accumulation and depletion regime and (e) inversion regime.

of read current can be observed for the UTMSG device with smaller r_i. The observation above is consistent with the results in [7].

Fig. 3(a) and (b) show the capacitance-voltage (C-V) characteristics of the devices above, with frequency f = 100 kHz. It can be observed that, for the UTMSG device, only the center gate will response to the AC small signal in accumulation and depletion regime. The open circle points in Fig. 3(a) are calculated using the capacitance of the planar device at −2 V, times the area ratio of center gate to the total gate, that is, $C_{Planar} \times r_i^2/r_o^2$, which match quite well with the observed data. The detailed numerical values are listed in the inset table. However, the capacitances of the UTMSG and planar devices become almost the same in inversion regime. The unusual C-V behavior could be explained by the proposed simplified AC small signal circuit model shown in Fig. 3(c). It should be noted that the edge thickened oxide is ignored here in the model, since it has little effect on the C-V, which will be verified in the end by simulation. $C_{ox,i}$ and $C_{s,i}$ represent respectively the capacitance of oxide and silicon under the center gate with radius r_i, while $C_{ox,o}$ and $C_{s,o}$ represent respectively the capacitance of oxide and silicon under the surrounding ring-shaped gate with inner radius r_i and outer radius r_o = 145 μm. R_{Al} accounts for the resistance including 1) the tunneling resistance of aluminum oxide on the connecting of the center gate and the surrounding gate and 2) the sheet resistance of the ultra thin surrounding gate. When R_{Al} is large enough

such that the impedance of R_{Al} is larger than that of $C_{\mathrm{ox,o}}$, that is, when $R_{\mathrm{Al}} > |1/j\omega C_{\mathrm{ox,o}}|$, $C_{\mathrm{ox,o}}$ will contribute little to the gate capacitance C_{G}. From another perspective, this circuit branch could be considered as a RC low-pass filter, with a cutoff frequency of $1/2\pi R_{\mathrm{Al}} C_{\mathrm{ox,o}}$. Accordingly, when the frequency of the AC small signal is high enough, this branch will not response and can be viewed as virtually open. R_{Si} represents the resistance of silicon connecting the regions under center gate and surrounding gate. When the silicon is in accumulation regime, the majority carrier (hole) under the center gate can response rapidly, with the hole carrier supply flow vertically pointing upwards. Under the circumstance, there is no lateral diffusion carriers between the two gates, and R_{Si} could be considered as virtually open, which reduces the circuit model to Fig. 3(d), that is, only the capacitance under the center gate will response to AC small signal in accumulation regime. In contrast, when silicon is in inversion regime, there will be inversion charges under both gates. The inversion charges will extend and form a narrow inversion channel connecting $C_{\mathrm{s,i}}$ and $C_{\mathrm{s,o}}$. The resistance of this inversion channel is expressed by R_{Si}. For simplicity, when the inversion carriers are dense enough, the inversion channel could be considered as a short circuit, which reduces the small signal model to Fig. 3(e). This means C_{G} is $C_{\mathrm{ox,i}}$ in series with $(C_{\mathrm{s,i}} + C_{\mathrm{s,o}})$ in inversion regime, or $1/C_{\mathrm{G}} = 1/C_{\mathrm{ox,i}} + 1/(C_{\mathrm{s,i}} + C_{\mathrm{s,o}})$. Since only the depletion charges of the silicon will follow the high-frequency AC signal, both $C_{\mathrm{s,i}}$ and $C_{\mathrm{s,o}}$ are far smaller than $C_{\mathrm{ox,i}}$, especially for the ultra thin oxide devices. As a result, C_{G} will be majorly determined by $(C_{\mathrm{s,i}} + C_{\mathrm{s,o}})$, which is independent of the value of $\mathrm{r_i}$ and also becomes the same with the C_{G} of the planar device. This could explain the overlapping of the C-V curves in Fig. 3(b) in inversion regime. Finally, in depletion regime, there is still not enough inversion carrier to form the inversion channel. In another word, R_{Si} is still too large to be considered as the short circuit, and the frequency of the AC signal is larger than the cutoff frequency of the R_{Si}-$C_{\mathrm{s,o}}$ low-pass filter. To simplify the circuit model in depletion regime, the circuit path of R_{Si} could be considered as virtually open and the circuit will reduce to Fig. 3(d). C_{G} of the UTMSG devices will be proportional to the area of the center gate, which agrees the experiment results in Fig. 3(b). In summary, the capacitances of UTMSG devices will be $C_{\mathrm{G}} = 1/(1/C_{\mathrm{ox,i}} + 1/C_{\mathrm{s,i}})$ in accumulation and depletion regime, which is proportional to the area of center gate, while $C_{\mathrm{G}} = 1/[1/C_{\mathrm{ox,i}} + 1/(C_{\mathrm{s,i}} + C_{\mathrm{s,o}})] \approx C_{\mathrm{s,i}} + C_{\mathrm{s,o}}$ in inversion regime, regardless of the area of the center gate.

Fig. 4 shows the 1 kHz C-V of the UTMSG and planar devices. In depletion regime, C_{G} decreases when $\mathrm{r_i}$ decreases, as in the 100 kHz C-V shown in Fig. 3(b). However, in inversion regime, C_{G} increases when $\mathrm{r_i}$ decreases, which is different from the 100 kHz C-V. This is because a small fraction of the inversion carriers under the center gate would be able to follow the relative low frequency at 1 kHz, which will increase $C_{\mathrm{s,i}}$ compared with the high frequency case at 100 kHz. At the same time, a smaller $\mathrm{r_i}$ means a larger area

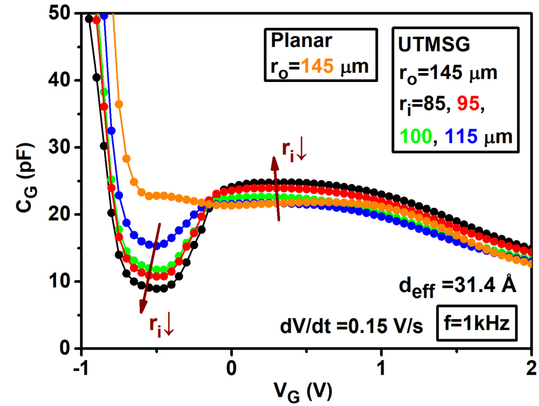

FIGURE 4. 1 kHz C-V of the UTMSG and planar devices. The capacitance of UTMSG devices with smaller $\mathrm{r_i}$ are larger in inversion regime.

of the surrounding gate and more inversion carriers under the surrounding gate could help the inversion carriers under the center gate response to the 1 kHz AC small signal. Therefore, a smaller $\mathrm{r_i}$ leads to a larger $C_{\mathrm{s,i}} + C_{\mathrm{s,o}}$ and then a larger C_{G}. This phenomenon also reveals that the amount of the inversion carriers under the surrounding gate is crucial under the non-static operation, and also proves the transient current improvement in Fig. 3(b), since the influence of the inversion carriers under the surrounding gate will be more significant with a smaller $\mathrm{r_i}$. Besides, compared Fig. 4 with Fig. 3(b), one can observe that 1 kHz C_{G} of the UTMSG devices will come up and enter into the regime that could be described by Fig. 3(e) earlier, despite the fact that the steady states should be totally the same. The reason could be explained again by Fig. 3(c). As V_{G} increases, the inversion carrier density increases and R_{Si} decreases. The cutoff frequency of the R_{Si}-$C_{\mathrm{s,o}}$ low-pass filter $1/2\pi R_{\mathrm{Si}} C_{\mathrm{s,o}}$ will then increase, meaning the AC signal with a lower frequency could pass at a smaller V_{G}.

To further study the unusual C-V behavior of the UTMSG devices, Silvaco TCAD simulation is implemented, with the schematic cross section and the small signal circuit model of the simulated device shown in Fig. 5(a). The center gate and the surrounding gate are represented by G1 and G2 respectively in the simulation. The gap with spacing S = 10 nm between G1 and G2 represents effectively the spatial disconnection of center gate and surrounding gate caused by aluminum oxide. A lumped resistance R_{G2} of 10^{14} Ω is connected to G2 to play the role of R_{Al} in Fig. 3(c). This very large value of R_{Al} is chosen in order to prevent G2 from responding to the applied AC small signal, and it could be seen later that the effect of R_{Al} on capacitance would be without much difference once R_{Al} exceeds 10^5 Ω. V_{G2} is the same with V_{G1} during the whole DC simulation, assuming that in steady state, the voltage of the center gate is able to couple to the surrounding gate in experiments. Noted that the total capacitance read by G1 and G2 will be totally determined by G1 since R_{G2} is too large to let the AC small signal pass through. Fig. 5(b) shows the 100 kHz C-V

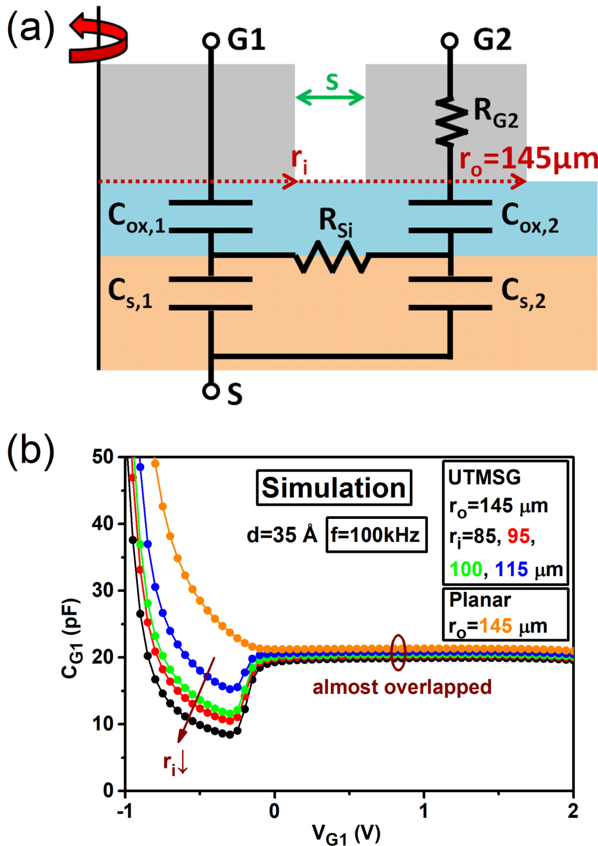

FIGURE 5. (a) The schematic cross section of the UTMSG device in 2D cylindrical TCAD simulation with a proposed small signal model. S and R_{G2} define the spacing between the two gates and the lumped resistance connected to G2, respectively. Unless otherwise specified, S is set to 10 nm and R_{G2} is set to 10^{14} Ω. (b) The simulation results of the C-V curves of the UTMSG and planar devices, with the same oxide thickness of 35 Å. The simulation results match quite well with the experiment results in Fig. 3(b).

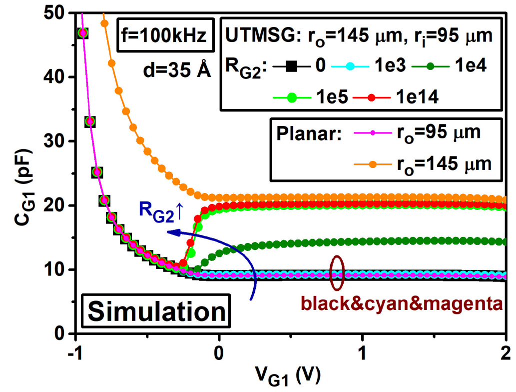

FIGURE 6. Simulation C-V curves of the UTMSG devices with the same $r_i = 95\mu$m but different R_{G2}. Only when R_{G2} is large enough will the C-V curve behaves like the experiment result.

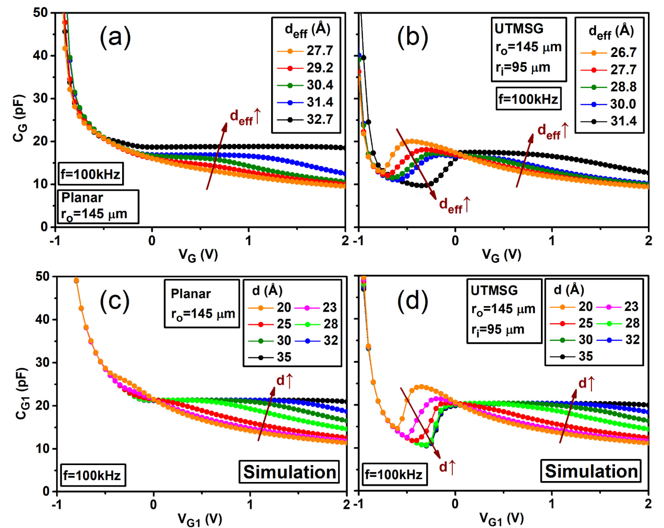

FIGURE 7. The experiment C-V curves of the (a) planar and (b) UTMSG devices with various oxide thickness. The simulation C-V curves of the (c) planar and (d) UTMSG devices with various oxide thickness.

results of the simulated UTMSG and planar devices, with all radius parameters identical to the experiments and the oxide thickness d = 35 Å. The C-V curves basically reproduce the results of Fig. 3(c), with the capacitances dispersing in depletion regime and overlapping in inversion regime. It is not a coincidence, since, if one connects G2 to G1, the TCAD simulation small signal model in Fig. 5(a) will become the same with the experiment small signal model in Fig. 3(c). Specifically, $C_{G1} = 1/(1/C_{ox,1} + 1/C_{s,1})$ in depletion regime and $C_{G1} = 1/[1/C_{ox,1} + 1/(C_{s,1} + C_{s,2})] \approx C_{s,1} + C_{s,2}$ in inversion regime. The successful reproduction of the unusual C-V curve by simulation shows that both the proposed small circuit model of experiment and the set up of TCAD simulation are reasonable.

Next in Fig. 6, C-V curves of UTMSG devices with the same $r_i = 95$ µm and $r_o = 145$ µm but different R_{G2} are shown to reveal the effect of R_{Al} in the experiment device. When R_{G2} is very large, the capacitance of the UTMSG will behave like the planar device with total radius $r_o = 145$ µm in inversion regime. However, if there is no lumped resistance at all, the capacitance of the UTMSG behaves like a normal planar device with $r_o = 95$ µm, since the AC signal could be able to pass through G2, and $C_{s,2}$ will be read out by G2 instead of G1. Therefore, it is important to assign a large enough R_{G2} in the simulation. Specifically, the cutoff frequency of the R_{G2} - $C_{ox,2}$ low-pass filter should not exceed 100 kHz. In this simulation, $C_{ox,2}$ is around 300 pF, deducing that a 10^5 Ω would be sufficient to achieve the desired results.

Fig. 7 shows the experiment and simulation results of C-V of planar and UTMSG devices, with various oxide thickness. The simulation results match well with the experiment results again, for both planar and UTMSG devices. The planar device with thinner oxide will undergo deep depletion earlier (at a lower gate voltage), as described in [16], which is also true for the UTMSG devices. Meanwhile, for UTMSG devices, the capacitances will come up earlier for thinner oxide since thinner oxide divides less gate voltage, and there will be more inversion carriers for thinner oxide.

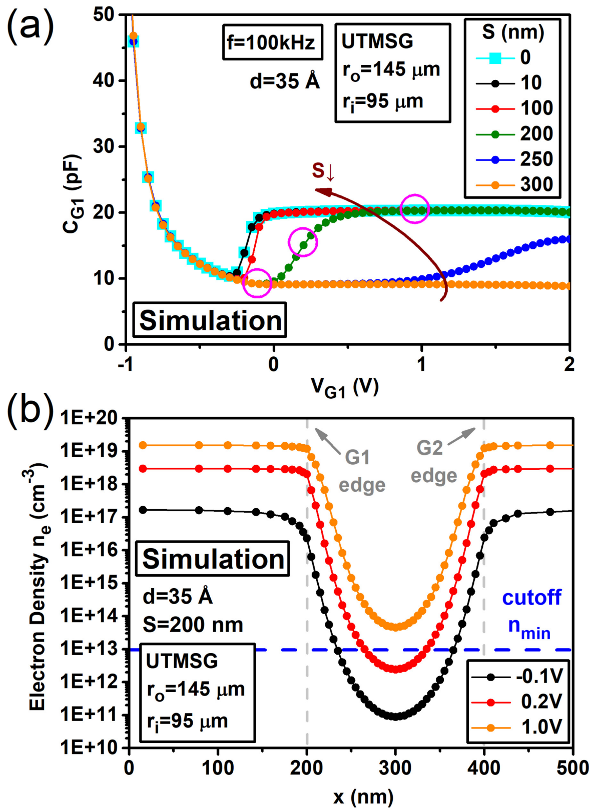

FIGURE 8. (a) The simulation C-V curves of the UTMSG devices with various spacing between the two gates, revealing the effect of R_{Si}. The three highlighted points are under further examination in (b). (b) Electron density of the UTMSG device with S = 200 nm around the gap, under the silicon surface with a depth of 2 nm, with −0.1, 0.2, and 1.0 V gate voltage.

Consequently, R_{Si} will decrease more rapidly and the device will get in inversion regime earlier.

It is assumed in the simulation before that there is a spatially spacing between G1 and G2, which is set to 10 nm. This is only a rough estimation to stand for the effect of aluminum oxide with several nanometers. Indeed, if there is no gap at all, the simulation result is the same, which can be confirmed by the overlapping C-V curves of S = 0 nm and S = 10 nm in Fig. 8(a). However, when S further increases, the inversion carriers can not create an inversion channel in the gap region any more. In the circuit point of view, R_{Si} increases for a larger S, which causes the AC signal become more difficult to pass through. For the case of S = 200 nm, V_{G1} should be as large as 0.5 V to make G1 be able to read the signal of $C_{s,2}$, compared to −0.1 V for S = 10 nm. And when S = 300 nm, $C_{s,2}$ could not be read out by G1 at all. The UTMSG device with S = 200 nm is chosen to further examine the effect of inversion carriers on R_{Si}. The chosen gate voltages of −0.1 V, 0.2 V, and 1 V show the different cases where the 100 kHz AC signal can not pass through, can partially pass through, and can totally pass through the R_{Si}-$C_{ox,2}$ low-pass filter, respectively. Fig. 8(b) shows the electron density around the gap under the silicon surface with the depth of 2 nm. A larger gate voltage gathers more inversion carriers in the gap region, which reduces R_{Si}, and the AC signal can pass more easily. The following gives a very rough estimation of the requirement of electron density for AC signal to pass. Assume that R_{Si} could be considered as the resistance of a ring-shaped inversion channel. To simplify the calculation, the inversion channel is turned into rectangular-shaped, with depth ∼ 1 nm, width ∼ 2π×95 μm, and length along the gap = 200 nm. Since the electron density is much higher than the hole density, the resistivity is determined by the electron density, that is,

$$\rho = \frac{1}{qn\mu_n} \tag{1}$$

where $q = 1.6 \times 10^{-19}$ C is the elementary charge constant and $\mu_n = 600\ \mathrm{cm^2/V \cdot s}$ is the electron mobility in silicon at room temperature. Besides, the electron density varies exponentially along the gap, and R_{Si} are contributed mostly by only a short spatial range with the least electron density. This range is approximated by $\delta x = 10$ nm for simplification. Accordingly, R_{Si} could be estimated by

$$R_{Si} = \int \frac{\rho(x)dx}{\text{width} \times \text{depth}} \tag{2}$$

$$\approx \frac{1}{\text{width} \times \text{depth} \times q\mu_n} \sum \frac{\delta x}{n(x)} \tag{3}$$

$$\approx \frac{1}{2\pi \times 95\ \mu m \times 1\ nm \times 1.6 \times 10^{-19}\ C \times 600\ cm^2/V \cdot s} \times \frac{10\ nm}{n_{min}} \tag{4}$$

$$\approx \frac{10^{19}}{2\pi} \times \frac{1}{n_{min}}\ \Omega \tag{5}$$

where the unit of n_{min} is cm^{-3}. Since $C_{ox,2} \sim 10$ pF $= 10^{-11}$ F, the cutoff frequency of the low-pass filter is of the order of $n_{min} \times 10^{-8}$. For a 100 kHz AC signal to pass through, n_{min} of order 10^{13} is needed, and is defined as the cutoff n_{min}. As illustrated in Fig. 8(b), only n_{min} of the 1 V curve exceed the cutoff n_{min}, matching the result that the AC signal can totally pass at this gate voltage, which indicates the rough calculation above is of reference for R_{Si}.

From another perspective, for the S = 200 nm curve in Fig. 8(a), the proposed AC circuit model with RC low-pass filter inside could be simplified to Fig. 3(d) when $V_G < -0.3$ V and to Fig. 3(e) when $V_G > 0.5$ V. However, there is still a transition region for $-0.3\ V < V_G < 0.5$ V, where R_{Si} could not be easily described by an open circuit or a short circuit. If the RC low-pass filter really presents its effect, its cutoff frequency in this transition region must be comparable to the 100 kHz AC frequency. Also noted that, since R_{Si} mainly depends on n_{min}, which relates to the gate voltage in an exponential form, the cutoff frequency of the low-pass filter would change exponentially with the gate voltage as well. As a result, when comparing the calculated cutoff frequency to 100 kHz AC frequency, it would be sufficient to deduce the correct order of magnitude of R_{Si}. For example, when the gate bias is 0.2 V, $10^{12} < n_{min} < 10^{13}$,

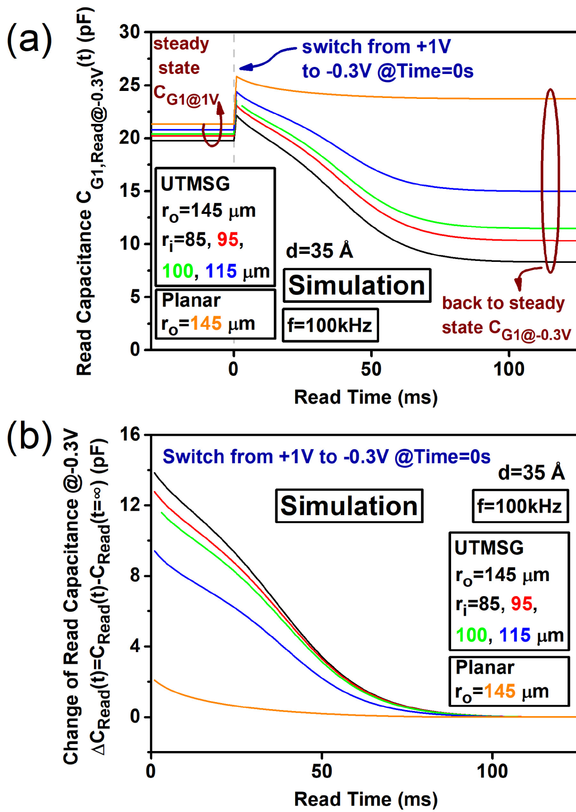

FIGURE 9. (a) Simulation of transient read capacitance of the planar and UTMSG devices when switching to −0.3 V from a 1 V steady state. (b) The change of read capacitance extracted from (a). Noted that for convergence issue, R_{G2} is set to 10^5 Ω in this transient simulation, which is large enough to get the desired result as discussed above.

the cutoff frequency is of the order of $10^4 \sim 10^5$, satisfying the requirement that the cutoff frequency in the transition region is comparable to 100 kHz AC frequency. Therefore, it is considered that the rough calculation of R_{Si} could be able to give an evidence to the proposed AC small signal model.

The unusual C-V of the UTMSG devices could be used to enhance the transient read capacitance window when operated as a dynamic memory. One can find it very straight forward in Fig. 5(b) that if the gate voltage of the device switches to −0.3 V from a positive voltage, for example, 1 V, the capacitance of the UTMSG will suffer from a larger change of value, especially for the UTMSG device with smaller r_i. Due to the limited time resolution of B1500A semiconductor device analyzer used for measurement, TCAD simulation is carried out instead, for a clearer picture of the transient capacitance. Fig. 9(a) shows the read capacitance of the devices in Fig. 5(b), switching from 1 V steady state to −0.3 V at Time = 0 s. Generally, for a MIS capacitor, when performing this voltage program, the inversion charges will not be recombined immediately, and the depletion region will shrink to balance the gate charges, which results in a larger capacitance. For the planar device, the capacitance will finally go to a higher level, since the depletion region is

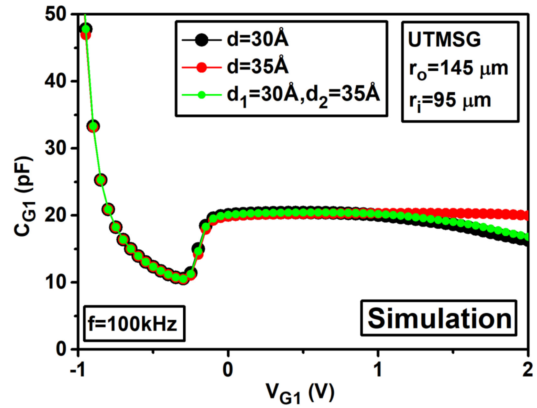

FIGURE 10. The simulation C-V curves of the UTMSG devices with uniform oxide layers and edge thickened oxide. d_1 and d_2 represent the oxide thickness under G1 and G2, respectively. The edge thickened oxide only slightly modulates the C-V curve compared to the original UTMSG device with uniform oxide.

smaller at −0.3 V than that at 1 V. However, the capacitances of the UTMSG devices are relative low at −0.3 V, since only $C_{ox,i}$ under oxide will response, instead of $C_{ox,i} + C_{ox,o}$ at 1 V. Besides, as r_i decreases, the degree of capacitance drop will be more severe. The change of read capacitance at −0.3 V or the capacitance window is shown in Fig. 9(b). By designing the ratio of G1 (center gate) and G2 (surrounding gate), one could be able to produce an improved capacitance window compared to the planar device with the same total gate area.

The effect of the edge thickened oxide is then discussed. Fig. 10 shows the simulated C-V of UTMSG devices with 30 Å and 35 Å uniform oxide, and a UTMSG device with 30 Å oxide under G1 and 35 Å oxide under G2. The introduction of edge thickened oxide only slightly increases the C-V curve in the deep depletion regime. The thicker oxide at edge can hold more inversion carriers and the device will undergo deep depletion later. As a result, $C_{s,2}$ of the edge thickened device will be greater than that of the 30 Å uniform UTMSG device, and the overall C_{G1} will be greater as well. However, the increment is not much and will not affect the correctness of the proposed AC small circuit model in Fig. 3(c), which considers uniform oxide thickness for simplification.

Finally, a simulation is carried out to show the possible potential for the UTMSG device to scale down to sub-micrometer scale. Fig. 11 shows the simulated C-V curves of a planar device with gate radius of 1 μm and UTMSG devices with r_o = 1 μm but different r_i. The circle points show the calculated value of the multiplication of capacitance of planar at −2 V and the area ratio for each UTMSG device, that is, $C_{Planar,-2V} \times r_i^2/r_o^2$, as in Fig. 3(a). It could be observed that the scaling devices preserve the unusual C-V behavior of the simulation results of the large devices as in Fig. 5(b). The success of simulation might provide the basis for the scaling of UTMSG device.

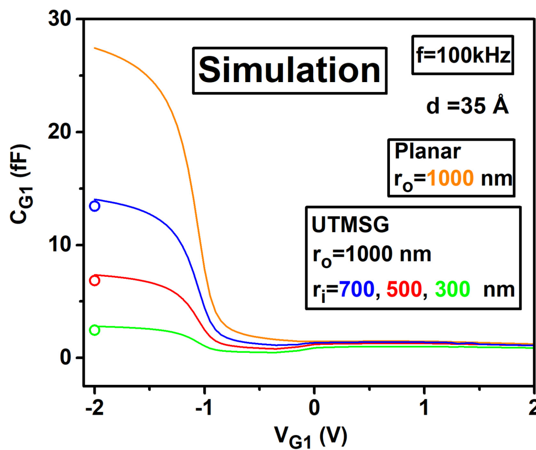

FIGURE 11. The simulation C-V curves of the scaling UTMSG devices. The total gate radius is set to 1 μm while the center gate radii are 300 nm, 500 nm and 700 nm. The circle points are calculated similarly as in Fig. 3(a). From the point of view of C-V characteristics, the UTMSG devices basically retain the properties when scaling.

IV. CONCLUSION

In conclusion, transient current enhancement of the UTMSG devices have been observed, which is a result of the delay of the inversion carriers under the surrounding gate. The unusual C-V behavior of the UTMSG devices could be explained by the proposed AC small signal model, including the resistance caused by the thin metal surrounding gate and the resistance of the inversion channel near the silicon surface. The proposed model could be verified by the reproduction of C-V curves using TCAD simulation. Furthermore, a rough calculation of the resistance of inversion channel from the carrier density solved by TCAD inside the device shows the consistency with the proposed model. The transient simulation has shown an improved capacitance window utilizing the unusual C-V behavior, which would be useful when implemented as memory device.

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