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Enhancement-Mode Characteristics of $Al_{0.65}Ga_{0.35}N/Al_{0.3}Ga_{0.7}N$/AlN/SiC MOS-HFETs

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ABSTRACT Widegap-channel $Al_{0.65}Ga_{0.35}N/Al_{0.3}Ga_{0.7}N$/AlN/SiC metal-oxide-semiconductor heterostructure field-effect transistors (MOS-HFETs) with ultrasonic spray pyrolysis deposition (USPD) grown Al_2O_3 gate-oxide demonstrating enhancement-mode (E-mode) operation are investigated for the first time. The E-mode operation was achieved by using fluorine ions (F^-) implantation. In comparison, conventional Schottky-gate device (sample A) and MOS-HFET (sample B) showing depletion-mode (D-mode) operation were fabricated on the same epitaxial structure. The device characteristics with respect to different gate-to-drain spacings (L_{GD}) of 6 μm and 14 μm have also been studied. The present E-mode $Al_{0.65}Ga_{0.35}N/Al_{0.3}Ga_{0.7}N$/AlN MOS-HFET (sample C) with L_{GD} = 6 (14) μm has demonstrated improved maximum drain-source current density ($I_{DS,max}$) of 206.3 (163.5) mA/mm at V_{DS} = 20 V, maximum extrinsic transconductance ($g_{m,max}$) of 32.9 (22.0) mS/mm, on/off-current ratio (I_{on}/I_{off}) of 3.7×10^9 (1.8×10^9), two-terminal off-state gate-drain breakdown voltage (BV_{GD}) of −370 (−475) V, and three-terminal on-state drain-source breakdown voltage (BV_{DS}) of 330 395 V.

INDEX TERMS Widegap AlGaN channel, MOS-HFET, enhancement-mode, Al_2O_3, non-vacuum ultrasonic spray pyrolysis deposition.

I. INTRODUCTION

Widegap-channel heterostructure field-effect transistors (HFETs) have been pioneered [1]–[3] due to the increasing needs of high-voltage power-switching devices for vehicle electronics and 5G communication applications [4]–[5]. The AlGaN compound semiconductors with wide bandgap, high Johnson's figure-of-merit (JFOM) [6], and high Baliga's figure-of-merit (BFOM) [7] are suitable channel materials. Besides, HFETs with enhancement-mode (E-mode) operation are essential to simplification of circuit implementation for power-switching applications. Various gate engineering techniques have been studied to obtain E-mode operation for nitride-based devices, including gate recess [8]–[9], p^+-AlGaN/GaN barrier [10]–[11], and fluorine plasma treatment [12]–[13]. Our previous works have studied widegap Si-doped AlGaN-channel metal-oxide-semiconductor HFETs (MOS- HFETs) showing depletion-mode (D-mode) operation [14]–[15]. This work reports, for the first time, $Al_{0.65}Ga_{0.35}N/Al_{0.3}Ga_{0.7}N$/AlN/SiC MOS-HFETs with USPD-grown Al_2O_3 gate-oxide showing E-mode characteristics. The fluorine ions (F^-) implantation was employed to increase the threshold voltage (V_{th}) and to achieve E-mode operation. Furthermore, the MOS-gate structure, oxide passivation, and increased gate-to-drain spacing designs were used to suppress the gate leakages, reduce the gate-drain electric filed, and increase the breakdown voltages. Al_2O_3 was formed within the drain-to-source region to serve as high-k gate-dielectric and surface passivation layer at the same time by using a cost-effective non-vacuum ultrasonic spray pyrolysis deposition (USPD) [16]–[17] technique. In comparison, conventional Schottky-gate HFET (sample A) and D-mode MOS-HFET without implanted F^- were fabricated and characterized at the same time. Device characteristics with varied gate-to-drain spacings (L_{GD}) of 6 μm and 14 μm have also been investigated.

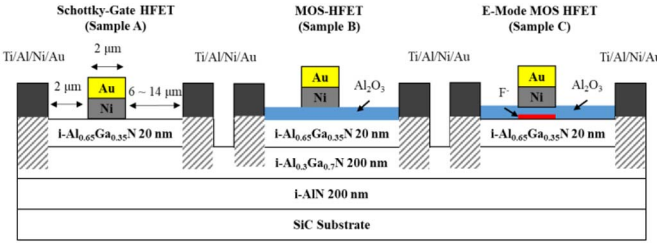

FIGURE 1. **Schematic device structures of (a) conventional Schottky-gate HFET, (b) D-mode MOS-HFET, and (c) the present E-mode MOS-HFET. L_{GD} was varied to be 6 μm and 12 μm.**

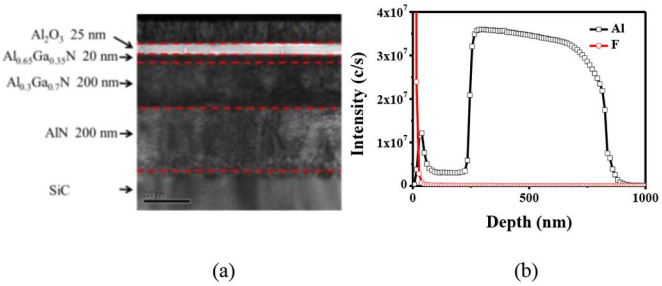

FIGURE 2. **(a) Cross-sectional TEM photo of the epitaxial structure for sample C; (b) the SIMS profiles of Al and F contents under the gate oxide of sample C.**

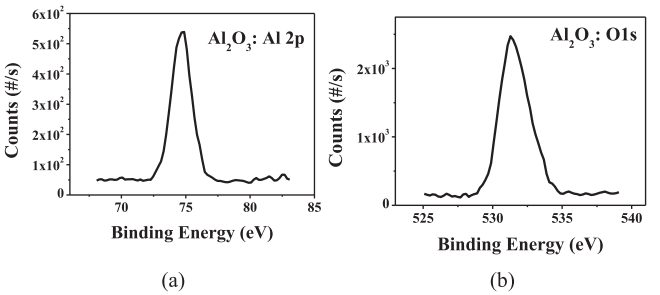

FIGURE 3. **XPS profiles of (a) Al 2p and (b) O 1s for the USPD-grown Al_2O_3.**

II. MATERIAL GROWTH AND DEVICE FABRICATION

Figs. 1(a)–(c) show the schematic device structures of (a) conventional Schottky-gate HFET (sample A), (b) D-mode MOS-HFET (sample B), and (c) the present E-mode MOS-HFET with F^- implantation (sample C). All the three devices were fabricated at the sample time on the identical epitaxial structure. The layer structures was grown on a SiC substrate by using a low-pressure metal-organic chemical vapor deposition (LP-MOCVD) system, including an intrinsic 200-nm AlN buffer, an intrinsic 200-nm $Al_{0.3}Ga_{0.7}N$ channel, and an intrinsic 20-nm $Al_{0.65}Ga_{0.35}N$ barrier. Standard photo- lithography and lift-off techniques were used for device fabrication [18]. For sample C, mesa etching was performed to provide electrical isolation for neighboring devices by using an inductively coupled-plasma reactive ion etcher (ICP-RIE). The etching barrier is 100-nm thick Ni layer. The ICP power is 110 W. The etching gas is BCl_3 with a flow rate of 40 sccm. The dry etching rate is about 36 nm/min. The source/drain electrodes were deposited directly on the $Al_{0.65}Ga_{0.35}N$ barrier. The thickness of Ti/Al/Ni/Au metal stack is 12.5 nm/175 nm/30 nm/40 nm. The source/drain ohmic contacts were formed by annealing the sample for 60 seconds at 900°C by using an ULVAC MILA-5000 rapid thermal annealing (RTA) system. After the gate photography, The F^- ions were implanted into the exposed $Al_{0.65}Ga_{0.35}N$ barrier. The reacting gas is CHF_3 with a flow rate of 50 sccm. The process time was tuned to be 115 seconds. Then, a 25-nm Al_2O_3 oxide was deposited, by using USPD technique, on the barrier within the drain-to-source region to serve as high-k gate dielectric and surface passivation layer simultaneously. Finally, Ni (150 nm)/Au (40 nm) gate electrode was evaporated to complete the device fabrication, as shown in Fig. 1(c). Schottky-gate and MOS-gate were fabricated on the barrier and Al_2O_3, respectively, for samples A and B without conducting F^- implantation. The gate dimensions are $2 \times 100\ \mu m^2$. The gate-to-source spacing is 2 μm. Devices were fabricated at the same time for samples A-C with varied L_{GD} of 6 μm and 14 μm to investigate the electric and deep-UV sensing characteristics. Fig. 2(a) shows the cross-sectional transmission electron microscopy (TEM) photo of the epitaxial structure for sample C. The layer thicknesses were verified as designed. The thickness of the USPD-grown Al_2O_3 was determined to be 25 nm. Besides, Fig. 2(b) shows the secondary ion-mass spectroscopy (SIMS) profiles of both Al and F contents under the gate oxide of sample C. The F^- ions were successfully implanted within the surface of $Al_{0.65}Ga_{0.35}N$ barrier.

III. EXPERIMENTAL RESULTS AND DISCUSSION

Hall measurement was performed for the epitaxial sample under a magnetic field of 5000 G at 300 K. The electron mobility (μ_n) and the two-dimensional electron gas concentration (n_{2DEG}) were determined to be 266.6 cm^2/V-sec and $1.37 \times 10^{13}\ cm^{-2}$, contributing to the μ_n-n_{2DEG} product of 3.65×10^{15} $(V\text{-}sec)^{-1}$ and the equivalent conductivity of 1.95×10^2 $(\Omega\text{-}cm)^{-1}$. The 2DEG was formed due to the polarization effect [19] and confined in the widegap channel of the $Al_{0.65}Ga_{0.35}N$/ $Al_{0.3}Ga_{0.7}N$ heterostructure. The X-ray photo-electron spectroscopy (XPS) was measured for the USPD-grown Al_2O_3 oxide. Figs. 3(a)–(b) show the characterized Al 2p and O 1s profiles with respect to binding energy. The Al 2p peak was found to be 74.9 eV, which is identical to that [20] of Al_2O_3 grown by atomic layer deposition (ALD). The O 1s peak associated with Al-O bonds was located at 531.2 eV, which is closer to the binding energy peak at 531.1 eV [21] of sapphire than the characterized 531.5 eV [20] of ALD-grown Al_2O_3. The USPD-grown Al_2O_3 has shown similar binding energies to those in an ALD-deposited Al_2O_3. Forming low contact resistances (R_C) are challenges for AlGaN channel devices, since it is difficult to form good ohmic contact on high Al-ratio AlGaN barrier with low electron affinity. Heavily-doped AlGaN barrier with graded channel [22] and graded $Al_xGa_{1-x}N$ barrier with x = 0 on the surface [23] have been used to reduce R_C. Fig. 4 shows the measured resistance characteristics by using the transfer length method (TLM) [24]

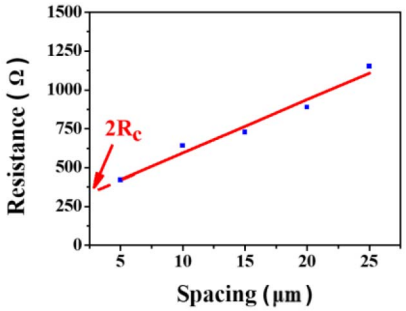

FIGURE 4. The measured TLM resistance characteristics at 300 K.

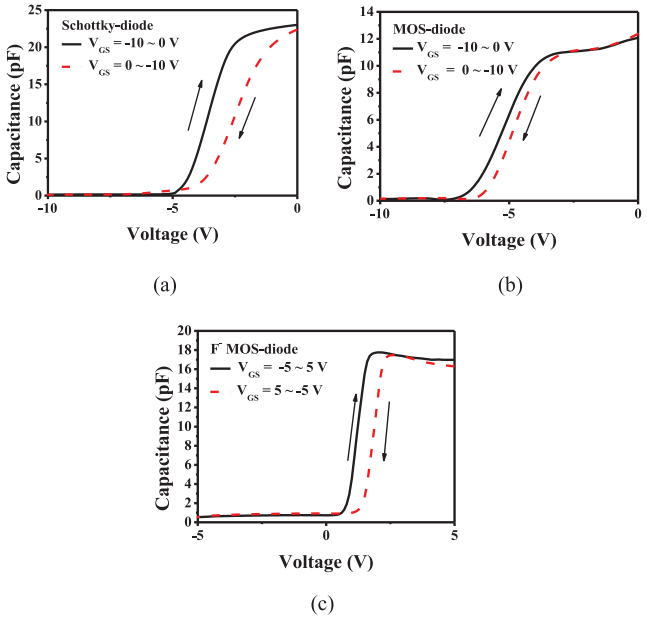

FIGURE 5. The measured C-V hysteresis characteristics for (a) Schottky-diode, (b) MOS-diode, and (c) F^- MOS-diode at 300 K.

at spacings of 5 μm, 10 μm, 15 μm, 20 μm, and 25 μm. The specific contact resistivity (ρ_c) and R_C were determined to be 4.7×10^{-4} Ω-cm^2 and 252.4 Ω-mm, which are comparable to our previous work [15] by using source/drain recess etching and, yet, higher than 140 Ω-mm [22] and 14 Ω-mm [23]. This indicated the undoped $Al_{0.65}Ga_{0.35}N$ barrier was too high for proper electron injection at the semiconductor/metal interface.

Figs. 5(a)–(b) show the measured C-V hysteresis characteristics for the Schottky-diode, MOS-diode, and F^- implanted MOS-diode (F^- MOS-diode) at 300 K, which are corresponding to the gate structures of samples A-C. The diode area is 8000 μm^2. The bias was increased from −10 (−5) V to 0 (5) V for samples A-B (C) and, then, decreased back to the starting voltage immediately. The hysteresis voltage (ΔV) calculated by the voltage difference between the mid-points of the C-V curves are 1.2 V, 0.5 V, and 0.6 V for the Schottky-diode, MOS-diode, and F^- MOS-diode. ΔV was mainly caused by the acceptor-like states in the Al_2O_3 or at the Al_2O_3/AlGaN interface [25]. Lower ΔV of MOS-diodes in samples B-C than Schottky-diode in sample A indicated the improved interface property by USPD-grown Al_2O_3 passivation, since the trapping and detrapping phenomena [26] were effectively reduced.

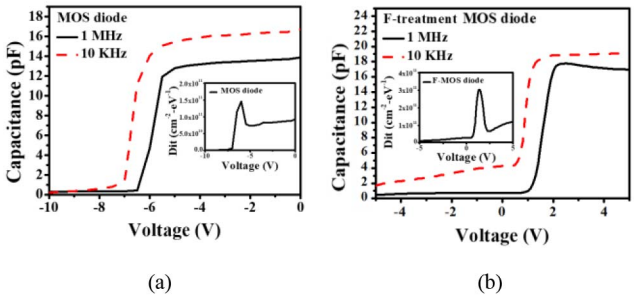

FIGURE 6. C-V curves measured at 1 MHz and 10 kHz for (a) MOS-diode and (b) F^- MOS-diode at 300 K; the insets show the extracted D_{it} profiles.

Though the F^- implantation has slightly increased ΔV in sample C, comparable interface property is maintained. Besides, the equivalent oxide capacitance (C_{ox}) was extracted [17] to be 27.3 pF. The permittivity of the deposited $Al_2O_3$was determined to be $k = 9.6$. Figs. 6(a)–(b) show the C-V curves measured at 1 MHz and 10 kHz for the MOS-diode and F^- MOS-diode at 300 K. In addition to the shifted C-V curve caused by the implanted F^- ions, higher capacitance of F^- MOS-diode than MOS-diode was due to the barrier etching effect [27] accompanied by the CHF_3 plasma treatment. Decreased separation to the 2DEG channel has increased the capacitance. The interface density (D_{it}) can be characterized by using the high/low-frequency method [28]. The extracted D_{it} profiles were shown in the insets of Fig. 6. The averaged D_{it} values of the MOS-diode and F^- MOS-diode are 8.24 $\times$ 10^{10} cm^{-2}-eV^{-1} and 9.31 $\times$ 10^{10} cm^{-2}-eV^{-1}. The D_{it} ranges are about $\sim 10^{11}$ cm^{-2}-eV^{-1} for both diodes, which are approximately 1 order lower than those in ALD-deposited Al_2O_3 [29], ALD-deposited ZrO_2 [30], and SiN grown by plasma-enhanced chemical vapor deposition (PECVD) [31].

Figs. 7(a)–(c) show the common-source current-voltage (I_{DS}-V_{DS}) characteristics (left) at 300 K and the transfer extrinsic transconductance (g_m) and saturated drain-source current (I_{DS}) density as functions of V_{GS} for samples A-C biased at $V_{DS} = 20$ V with $L_{GD} = 6$ μm and 14 μm, respectively. The devices were measured by using a KEITHLEY 4200 analyzer. The V_{GS} voltage was varied from −8/−10/0 V to 2/10/10 V at 1 V/step for samples A/B/C, as indicated in Figs. 7(a)–(c). Good pinch-off was observed in the studied devices. The maximum I_{DS} ($I_{DS,max}$) densities for samples A-C with L_{GD} = 6 (14) μm were found to be 134.3 (117.3) mA/mm, 413.4 (348.9) mA/mm, and 206.3 (163.5) mA/mm at V_{DS} = 20 V, with the maximum extrinsic transconductance ($g_{m,max}$) of 31.9 (24.9) mS/mm, 32.1 (28.5) mS/mm, and 32.9 (22.0) mS/mm. The dynamic turn-on resistances (R_{on}) samples A-C with $L_{GD} = 6$ (14) μm were calculated to be 74.1 (118.3) Ω, 57.5 (92.4) Ω, and 61.6 (95.0) Ω. The corresponding field mobility (μ_{fe}) were 71.1 (63.1) cm^2/V-sec, 88.9 (79.4) cm^2/V-sec, and 86.4 (74.0) cm^2/V-sec. The threshold voltages (V_{th}) for the D-mode devices were determined by the extrapolated intercept of the $(I_{DS})^{1/2}$ line to the V_{GS}-axis, while V_{th} of the E-mode device is the corresponding V_{GS} bias where I_{DS} =

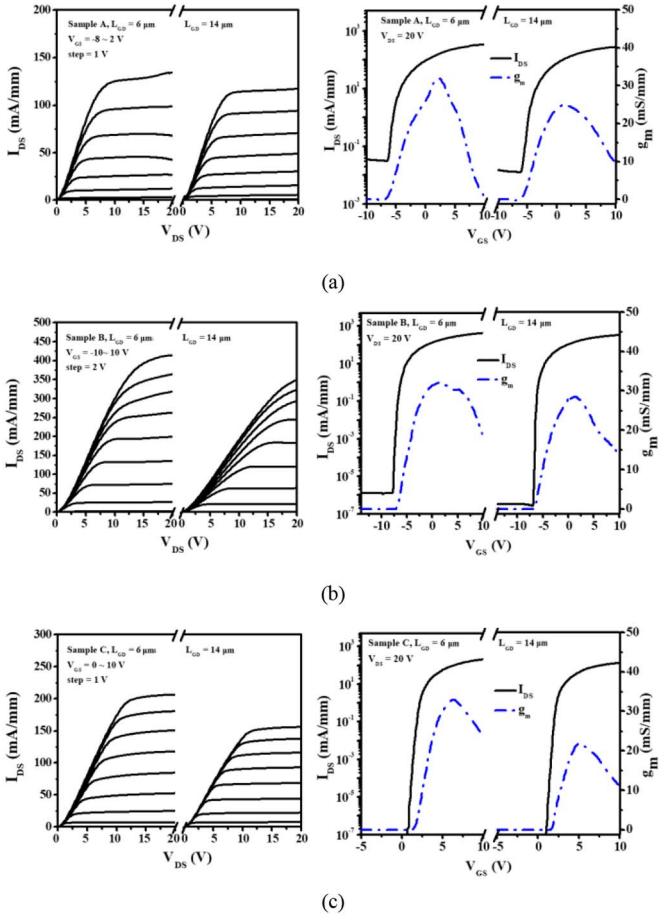

FIGURE 7. **Common-source I_{DS}-V_{DS} characteristics (left) at 300 K and the transfer g_m and I_{DS} as functions of V_{GS} (right) for samples (a)A, (b) B, and (c) C with L_{GD} = 6 μm and 14 μm, respectively.**

1 μA/mm. The respective V_{th} values were determined to be −5.5 (−4.7) V, −7.0 (−6.3) V, and 1.2 (1.6) V for samples A-C with L_{GD} = 6 (14) μm. The V_{th} values of samples B-C approximately agree with the C-V threshold of MOS-diode and F^--implanted MOS-diode, as shown in Fig. 5 (b)–(c). Sample B has demonstrated enhanced D-mode characteristics than the control sample A. Improved I_{DS} and reduced R_{on} are mainly resulted from the reduced channel depletion [32] due to passivated interface by the USPD-grown Al_2O_3 covering the barrier surface between the drain/source electrodes. Higher $g_{m,max}$ of sample B than sample A is due to the enhanced gate modulation capability by the high-k gate oxide of Al_2O_3. Besides, E-mode operation has been successfully achieved in sample C by the F^- implantation. The obtained high V_{th} value is favorable to noise immunity for circuit switching application. The on/off-current ratios (I_{on}/I_{off}) for samples A-C with L_{GD} = 6 (14) μm were determined to be 1.1 × 10^4 (2.4 × 10^4), 7.3 × 10^8 (1.2 × 10^9), and 3.7 × 10^9 (1.8 × 10^9). The subthreshold slope (SS) was defined to be the required V_{GS} difference to obtain 10 times increase/decrease in the I_{DS} density. It represents the device switching performance for transistor operation. The corresponding SS are 481.0 (522.2) mV/dec, 105.0 (94.4) mV/dec, and 87.3 (91.7) mV/dec. Sample B has shown improved I_{on}/I_{off} and SS characteristics than sample A due to enhanced gate insulation, $g_{m,max}$ gain, and I_{DS} density. It can also been that the all devices with large L_{GD} has shown degraded $g_{m,max}$, I_{DS}, and SS characteristics. It is due to the increased channel resistance and reduced gate-drain electric field with large L_{GD}. Nevertheless, higher I_{on}/I_{off} was observed in both D-mode samples A-B with larger L_{GD}, since I_{off} was decreased significantly. Though the I_{on}/I_{off} ratio of sample C was slightly decreased at L_{GD} = 14 μm, superior I_{on}/I_{off} and SS performances in E-mode operation are achieved, which are beneficial to circuit switching applications. Fig. 8 shows the I_{DS}-V_{DS} curves at V_{GS} = 10 V for sample C with L_{GD} = 6 μm at 300-450 K. I_{DS} was observed to decrease with temperature. It is possibly due to the degraded transport property by the carrier-carrier scattering, since more electrons were thermally generated at higher temperature. Besides, V_{th} was characterized to be 0.8 V, 0.4 V, and −0.3 V at 350 K, 400K, and 450 K. The present sample C can maintain E-mode operation up to 400 K and has returned to D-mode at 450 K due to thermal diffusion of F^- ions [33].

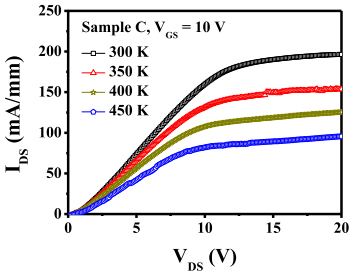

FIGURE 8. **I_{DS}-V_{DS} curves at V_{GS} = 10 V for sample C with L_{GD} = 6 μm at 300-450 K.**

Figs. 9–10 show the two-terminal off-state gate-drain breakdown voltage (BV_{GD}) and three-terminal on-state drain-source breakdown voltage (BV_{DS}) characteristics at 300 K for samples A-C with L_{GD} = 6 μm and 14 μm, respectively. BV_{GD} and BV_{DS} were defined to be the corresponding biases where the I_{GD} and I_{DS} densities reached 1 mA/mm. V_{GS} was biased at −20 (−10) V when characterizing BV_{DS} for samples A-B (C). The measured BV_{GD} for samples A-C at L_{GD} = 6 (14) μm are −325 (−360) V, −355 (−480) V, and −370 (−475) V. The corresponding BV_{DS} are 330 (375) V, 340 (400) V, and 330 (395) V. All three devices have shown good breakdown characteristics due to the effective reduction in gate/substrate leakages by the devised widegap $Al_{0.65}Ga_{1-x}N$/AlN barrier/buffer layers. Enhanced breakdown performance at large L_{GD} spacing were expected due to decreased gate-drain electric field. Both samples B and C with different D-mode and E-mode operations have exhibited superior BV_{DS} and BV_{GD} performance as compared to sample A. It is attributed by the MOS-gate design to further suppress the gate leakage due to reduced thermionic emission and passivated surface states. The breakdown performance and lateral electric field were strongly related to the gate/drain

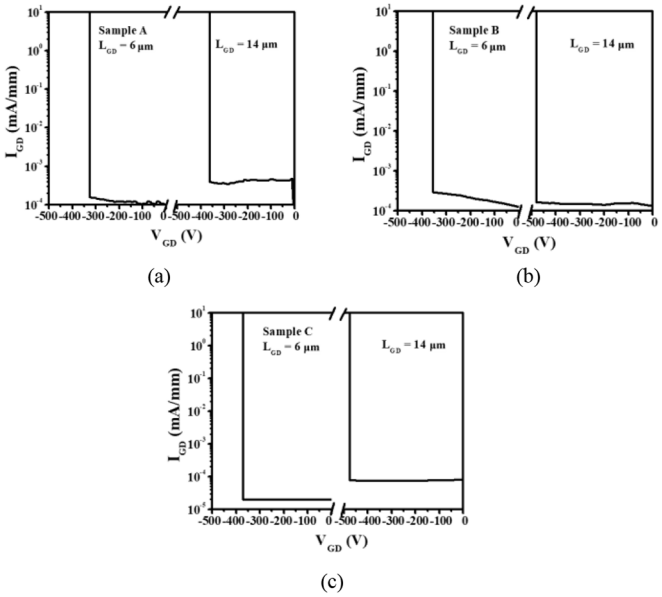

FIGURE 9. ***BV_{GD}*** **characteristics at 300 K of samples (a) A, (b) B, and (c) C with L_{GD} = 6 μm and 14 μm, respectively.**

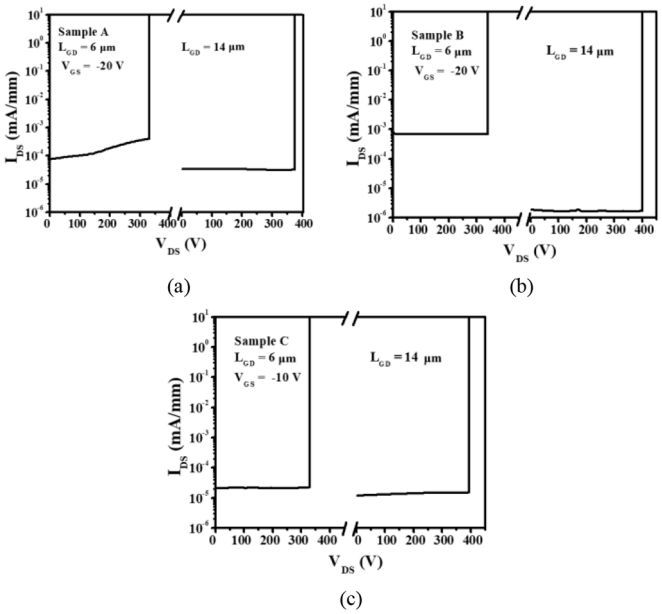

FIGURE 10. ***BV_{DS}*** **characteristics at 300 K of samples (a) A, (b) B, and (c) C with L_{GD} = 6 μm and 14 μm, respectively.**

isolation designs, including gate dielectric, field-plate, gate-drain recess, or composite passivation. Besides, the reduction of the source/drain contact resistance is essential to the breakdown characteristics for widegap channel devices. Sample B has shown improved D-mode characteristics as compared to other high-Al content AlGaN devices [22]–[23] with $I_{DS,max}$ = 126 mA/mm and 350 mA/mm, $g_{m,max}$ = 4.6 and 9 mS/mm, I_{on}/I_{off} = 10^4 and 10^7, BV_{GD} = −375 V, and BV_{DS} = 116 and 275 V. Besides, the present sample C is also superior to other E-mode devices [34]–[35] showing $I_{DS,max}$ = 102 mA/mm and 90 mA/mm, $g_{m,max}$ = 32 mS/mm and 13 mS/mm, and I_{on}/I_{off} = 10^7 and 10^8. Tables 1–3 summarizes the device characteristics for samples A-C with complete L_{GD} variation of 6 μm, 8 μm, 10 μm, 12 μm, and 14 μm. It can be seen that both $I_{DS,\ max}$ and $g_{m,max}$ decreased with L_{GD} for all devices, which are mainly caused the increased channel resistance since the drain-to-source distances were also increased. V_{th} was observed to increase with L_{GD}. It is because that more negative V_{GS} bias was needed to turn off higher I_{DS} conduction for the D-mode operation samples A-B with smaller L_{GD}. On the other hand, more positive V_{GS} bias was required to initiate I_{DS} conduction for the E-mode sample C with lower g_m gain at larger L_{GD}. The I_{on}/I_{off} dependences on L_{GD} are similar to the V_{th} variations. For samples A-B, the decrease in I_{off} at large

TABLE 1. Device characteristics of sample A.

L_{GD}	6 μm	8 μm	10 μm	12 μm	14 μm
$I_{DS,\ max}$ (mA/mm)	134.3	131.3	129.9	127.1	117.3
$g_{m,\ max}$ (mS/mm)	31.9	33.0	25.9	24.1	24.9
V_{th} (V)	-5.5	-5.2	-4.9	-4.8	-4.7
I_{on}/I_{off} ($\times 10^4$)	1.1	1.1	1.3	2.0	2.4
BV_{GD} (V)	-325	-330	-350	-355	-360
BV_{DS} (V)	330	340	350	360	375

TABLE 2. Device characteristics of sample B.

L_{GD}	6 μm	8 μm	10 μm	12 μm	14 μm
$I_{DS,\ max}$ (mA/mm)	413.4	411.4	397.0	381.4	348.9
$g_{m,\ max}$ (mS/mm)	32.1	31.5	30.9	30.5	28.5
V_{th} (V)	-7.0	-6.6	-6.4	-6.4	-6.3
I_{on}/I_{off} ($\times 10^8$)	7.3	8.5	9.1	10.5	12
BV_{GD} (V)	-355	-380	-400	-420	-480
BV_{DS} (V)	340	350	360	370	400

TABLE 3. Device characteristics of sample C.

L_{GD}	6 μm	8 μm	10 μm	12 μm	14 μm
$I_{DS,\ max}$ (mA/mm)	206.3	185.3	173.1	169.8	163.5
$g_{m,\ max}$ (mS/mm)	32.9	26.7	23.3	22.8	22.0
V_{th} (V)	1.2	1.4	1.4	1.5	1.6
I_{on}/I_{off} ($\times 10^9$)	3.7	2.8	2.7	2.0	1.8
BV_{GD} (V)	-370	-400	-420	-460	-475
BV_{DS} (V)	330	345	380	390	395

L_{GD} has dominated the I_{on}/I_{off} performance. Higher I_{on} at smaller L_{GD} has resulted in higher I_{on}/I_{off} ratio in the E-mode sample C. Besides, both BV_{GD} and BV_{DS} performance were improved with L_{GD}. It is mainly caused by the relieved electric field by the increased L_{GD} separation.

IV. CONCLUSION

E-mode characteristics of $Al_{0.65}Ga_{0.35}N/Al_{0.3}Ga_{0.7}N$/AlN/SiC MOS-HFETs with USPD-grown high-k Al_2O_3 gate-oxide are investigated. The E-mode operation has been successfully achieved by F^- implantation into the $Al_{0.65}Ga_{0.35}N$ barrier surface. Improved gate insulation, enhanced gate modulation, and effective surface passivation are obtained at the same time by using the cost-effective USPD technique. Devices with Schottky-gate and MOS-gate structures showing D-mode operation were fabricated in comparison. The present E-mode MOS-HFET design with $L_{GD} = 6$ (14) μm has demonstrated superior $I_{DS,max}$ of 206.3 (163.5) mA/mm, $g_{m,max}$ of 32.9 (22.0) mS/mm, I_{on}/I_{off} of 3.7×10^9 (1.8×10^9), SS of 87.3 (91.7) mV/dec, BV_{GD} of −370 (−475) V, and BV_{DS} of 330 (395) V with $V_{th} = 1.2$ (1.6) V and. The present E-mode widegap-channel MOS-HFET are suitable for high-voltage power-switching applications.

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