Received 3 August 2021; revised 28 September 2021 and 14 October 2021; accepted 15 October 2021. Date of publication 19 October 2021; date of current version 1 November 2021. The review of this article was arranged by Editor C.-M. Zetterling.

Digital Object Identifier 10.1109/JEDS.2021.3121212

4H-SiC-Based ESD Protection Design With Optimization of Segmented LIGBT for High-Voltage Applications

KYOUNG-IL DO (Graduate Student Member, IEEE), SEUNG-HOO JIN (Graduate Student Member, IEEE), BYUNG-SEOK LEE (Graduate Student Member, IEEE), AND YONG-SEO KOO (Member, IEEE)

Department of Electronics and Electrical Engineering, Dankook University, Yongin 16890, Gyeonggi, Republic of Korea

CORRESPONDING AUTHOR: Y.-S. KOO (e-mail: yskoo@dankook.ac.kr)

This work was supported in part by the Korea Institute for Advancement of Technology (KIAT) Grant funded by the Korea Government (MOTIE) under Grant P0017011 (HRD Program for Industrial Innovation), and in part by the Ministry of Science and ICT (MSIT), South Korea, through the Information Technology Research Center (ITRC) Support Program under Grant IITP-2018.

ABSTRACT 4H-SiC is a wide-bandgap material that exhibits excellent high-temperature conductivity and high operating voltage. These characteristics can provide high electrostatic discharge (ESD) robustness in high voltage applications. However, a considerably wide range of snapback phenomena is triggered for 4H-SiC-based ESD protection devices owing to a high critical electric field. In this study, an ESD protection device based on a lateral insulated-gate bipolar transistor (LIGBT) with a new structure that creates an internal silicon-controlled rectifier (SCR) path is proposed. The proposed ESD protection device minimizes the effective base region of the NPN parasitic bipolar transistor to the gate length based on the internal SCR operation of the LIGBT. It also adjusts the emitter injection efficiency of the PNP parasitic bipolar transistor by introducing a segment topology and inserting an additional implant area. Consequently, the proposed ESD protection device significantly improves the wide range of snapback phenomena occurring in the 4H-SiC materials. A conventional SCR, the LIGBT, and the proposed protection device were fabricated using the 4H-SiC process under the same condition, and their electrical characteristics were comparatively analyzed using a transmission-line pulse system. Moreover, its high-temperature reliability was evaluated at 300–500 K to examine the compatibility with 4H-SiC devices and circuits that require a relatively high-temperature operation.

INDEX TERMS Electrostatic discharge, holding voltage, snapback, silicon-controlled rectifier, lateral insulated-gate bipolar transistor.

I. INTRODUCTION

Silicon carbides (SiC) are wide-bandgap (WBG) semiconductor materials that exhibit excellent performance in high-power, high-voltage applications [1], [2]. Various studies that utilize 4H-SiC are being conducted because 4H-SiC has a better bulk electron mobility in horizontal and vertical directions than 3C and 6H-SiC [3]–[5]. Moreover, 4H-SiC exhibits excellent high-temperature conductivity [6]. Therefore, it is suitable for fields that require high operational temperature, such as avionics, automobiles, earth drilling, and space exploration. In addition, several studies have reported that 4H-SiC has excellent high-temperature operating regions that exceed the maximum operating temperatures (150 °C) of silicon [7], [8]. Furthermore, 4H-SiC has a very high current density compared to the operating voltage; therefore, it is possible to implement high-voltage devices with a smaller area, which significantly improves the area efficiency of power electronic devices [9]. However, because 4H-SiC-based devices and circuits have a high operating voltage, high current density, and high-frequency characteristics in a small area, a severe electrical stress may occur owing to surges that flow in from the outside, such as a high electrostatic discharge (ESD) [10], [11]. Consequently, this may lead to thermal runaway and cause critical damage to the electronic devices. The failure mechanism of 4H-SiC devices was

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

analyzed based on the recent ESD standards, and research was conducted on the junction of 4H-SiC power devices and ESD sensitivity of the oxide [12], [13]. However, few studies have been reported that implement the existing protection devices using SiC materials to incorporate the high robustness, low resistance, and excellent high-temperature characteristics of 4H-SiC materials into ESD protection devices. The silicon-controlled rectifier (SCR) and lateral insulated-gate bipolar transistor (LIGBT) are common ESD protection devices [14]. They both operate via a double-injection mechanism and have excellent current density based on the latch-mode operation of NPN and PNP parasitic bipolar transistors. Consequently, several engineers select the SCR and LIGBT as high-voltage ESD protection devices, and various studies have been conducted to optimize their electrical characteristics [15]–[17]. However, because the critical electric field (E_C) is significantly high compared to the forward voltage drop in 4H-SiC, a strong snapback phenomenon occurs [18], [19]. In this snapback phenomenon, the difference between the trigger and holding voltages becomes larger than when silicon is used for fabrication. This could be a serious problem in the optimization of the electrical characteristics for the ESD design window for practical applications [20], [21]. However, a few studies have been reported to improve the strong snapback phenomenon occurring in the 4H-SiC materials [22].

This study proposes an LIGBT-based protection device to improve the snapback phenomenon occurring in 4H-SiC. Using a transmission-line pulse (TLP) system, the electrical characteristics were analyzed and compared with a conventional silicon-controlled device and LIGBT. Thermal reliability experiments were conducted to verify the stable operation of the device at high temperatures.

II. NEW 4H-SIC-BASED ESD PROTECTION DEVICE

A. DEVICE STRUCTURE AND DESCRIPTION

Figs. 1 (a) and (b) show the cross-section of a conventional SCR and LIGBT implemented using the 4H-SiC process, where both the SCR and LIGBT use a double-injection mechanism in the ESD mode. Owing to a positive feedback of parasitic NPN and PNP bipolar transistors, SCR and LIGBT create an internal SCR path to discharge the ESD current. Moreover, the LIGBT structure is used with the gate grounded and comprises a relatively long drift region. Therefore, it is actively used in high-voltage SCRs. Although the two traditional devices have a relatively wide range of snapback characteristics, they have excellent current-driving capability. Therefore, various studies have been conducted in a silicon environment to utilize them actively [14]–[17]. However, when these devices are fabricated using the 4H-SiC materials, the difference between the trigger voltage (V_{t1}) and holding voltage (V_h) becomes even larger. These voltages depend on the following latch-mode equations for the double-injection ESD protection devices [11], [20].

$$V_{h,} = V_{EB,Qp} + V_{CE,Qn,sat} + \text{or } V_{BE,Qn} + V_{EC,Qp,sat} \quad (1)$$

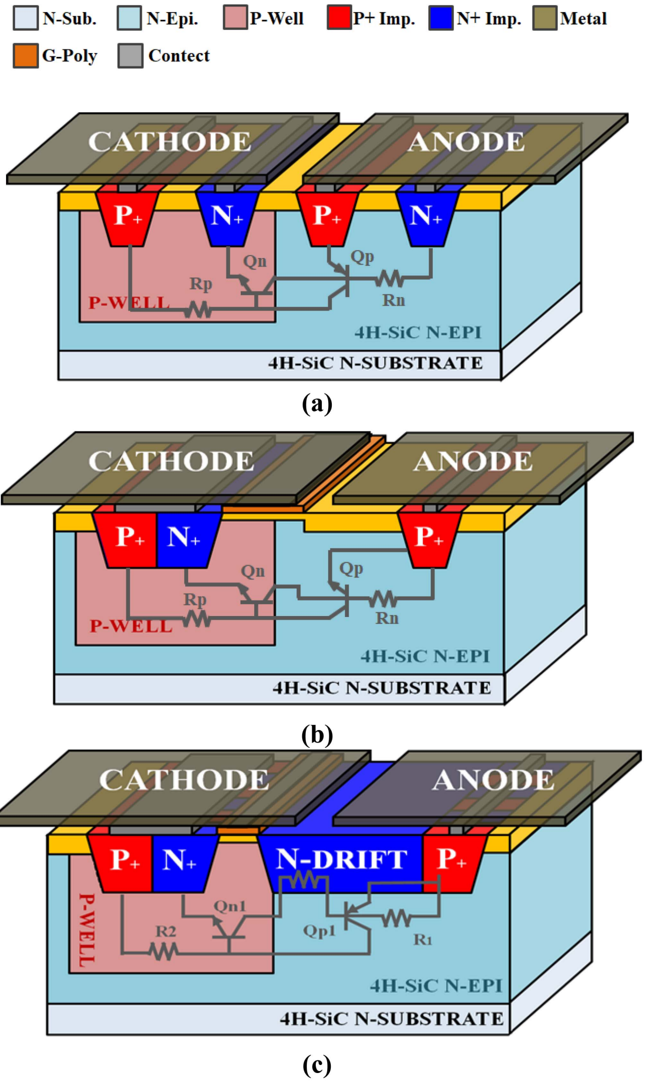


FIGURE 1. Cross-section of the 4H-SiC-based (a) conventional SCR, (b) gate -grounded LIGBT, and (c) proposed ESD protection devices.

$$V_{t1,} = BV_{A'K'} \approx BV_{AK} + V_{rep} + V_{ren} \quad (2)$$

As shown in Equation (1), the holding voltage (V_h) depends on the forward voltage drop ($V_{EB,Qp}$, $V_{BE,Qn}$) of the PNP parasitic bipolar transistor and the NPN parasitic bipolar transistor. Further, as shown in Equation (2), the trigger voltage (V_{t1}) depends on the breakdown voltage (BV_{AK}) across the device and the voltage drop of parasitic resistance at the emitter after avalanche breakdown (V_{rep}, V_{ren}). The built-in potential of 4H-SiC, which is approximately three times that of silicon, induces an increase in V_h. However, because the E_C of 4H-SiC is ten or more times that of silicon, 4H-SiC has a significantly large BV_{AK}, which denotes the reverse breakdown voltage in proportion to the E_C. In addition, the values of V_{rep} and V_{ren} depend on the resistance of N-type and P-type after the avalanche breakdown. The electron and hole mobility values of 4H-SiC are approximately three times and ten times lower, respectively, than those of silicon. Consequently, a strong snapback phenomenon

with a considerable difference between V_{t1} and V_h occurs in 4H-SiC, and it significantly reduces the compatibility with the actual ICs. Therefore, a snapback control technology that is more powerful than silicon is required to utilize 4H-SiC materials in double-injection-based ESD protection devices, such as SCRs and LIGBTs, for practical applications. Moreover, an additional N-drift region and a modified segment topology based on the LIGBT are applied to the proposed device as shown in Fig. 1 (c). If an ESD event occurs at the anode, the potential of the N-drift region increases, and an avalanche breakdown occurs at the junction between the P-wells. Owing to the avalanche breakdown at a high doping concentration, BV_{AK} reduces significantly compared to the reduction in the conventional SCR and LIGBT. The generated electron current flows through the N-drift region, switches on the P+ anode and junction, and operates the parasitic NPN bipolar transistor (Q_{n1}). Q_{n1} supplies the base current ($I_{b,Qp1}$) for the PNP parasitic bipolar transistor (Q_{p1}), and Q_{n1} and Q_{p1} switch to a latch-mode and form the SCR path. R_{ep}, along with the lowered BV_{AK}, is minimized to the bottom of the gate region, and R_{en} is reduced because of the high doping concentration of the N-drift. In addition, Q_{p1} forms the base region in N-drift and has a relatively low current gain (B); therefore, it has a relatively high holding voltage characteristic. Moreover, the modified segment topology is applied to the anode and cathode of the proposed structure to bias in the N-drift region and significantly reduces the emitter injection efficiency of Q_{n1} and Q_{p1} [23], [24]. Owing to the application of the segment topology, the emitters of Q_{n1} are segmented, and half of them are replaced by P+. In addition, the emitters of Q_{p1} are segmented, and half of them are replaced by N+. Owing to the PN junction and depletion region formed in each emitter area, the effective base of the two parasitic bipolar transistors (Q_{n1}, Q_{p2}) is reduced, thus reducing the emitter injection efficiency and increasing the holding voltage of proposed device. Consequently, the proposed device enhances the trigger characteristics by reducing BV_{AK}, V_{rep}, and V_{ren}, in addition to achieving a high holding voltage owing to its structural characteristics.

B. FABRICATION OF EXPERIMENTAL DEVICES AND THE 4H-SIC PROCESS

The conventional SCR, LIGBT, and proposed devices were fabricated on the N+ substrate of a 4H-SiC wafer, and the gate oxide thickness was 600 Å. The depth of the P-well region was approximately 0.9 μm, and the doping concentration was 5.0E18 cm^{-3}. Moreover, the P-type implant region was formed by injecting aluminum and had a depth of approximately 0.25 μm and concentration of 1.0E20 cm^{-3}. The N-type implant region used nitrogen, which has a higher energy and lower atomic weight than phosphorus, and had a depth of approximately 0.3 μm and concentration of 2.0E19 cm^{-3}. Each implantation process step was activated for 30 min at 1600 °C to 1700 °C using nitrogen

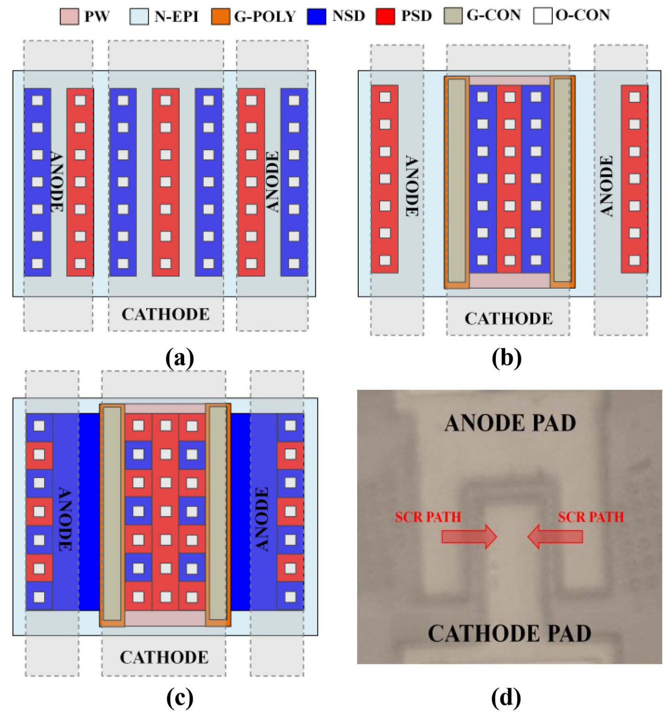


FIGURE 2. Layout of (a) conventional SCR, (b) LIGBT, and (c) proposed ESD protection devices, and (d) 50 times magnified image of the proposed device implemented using the 4H-SiC process.

TABLE 1. Summarized ion implantation energy and depth of layers.

Layer	Ion Implantation	Junction Depth	Doping Concentration
P-Well	580 keV	0.9 µm	5.0E18 cm^{-3}
N+ Implant	230 keV	0.3 µm	2.0E19 cm^{-3}
P+ Implant	190 keV	0.25 µm	1.0E20 cm^{-3}
N-epitaxial	-	13 µm	5E15 cm^{-3}

and aluminum sources. In addition, to form an ohmic contact with N+ and P+, a silicide process using NiV metal was employed and treated with heat at 1000 °C/2 min in the rapid thermal annealing (RTA). The high temperature oxide (HTO) was heat-treated at Thermal 100A + HTO ~600 A, 1230 °C/4 h, N_2O gas ambient. For a fair comparison of the electrical characteristics, all experimental devices were designed with a finger structure and had the same implant width of 200 µm [25]. Table 1 summarizes the ion implantation energy, junction depth, and doping concentration of the fabricated devices, and Fig. 2 shows the device layout according to this process.

III. MEASUREMENT RESULTS AND DISCUSSION

A. OPTIMIZATION OF ELECTRICAL CHARACTERISTICS THROUGH DESIGN VARIABLES

A TLP system with a rise time of 10 ns and a pulse width of 100 ns was used to verify the electrical characteristics of the proposed device [26]. In the TLP experiment, most ESD protection devices fabricated with a width of 200 um did not

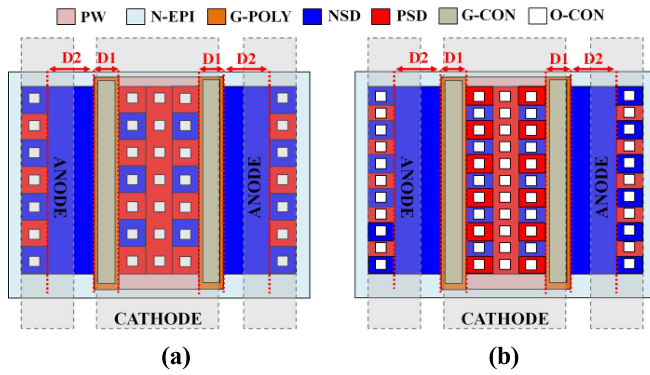
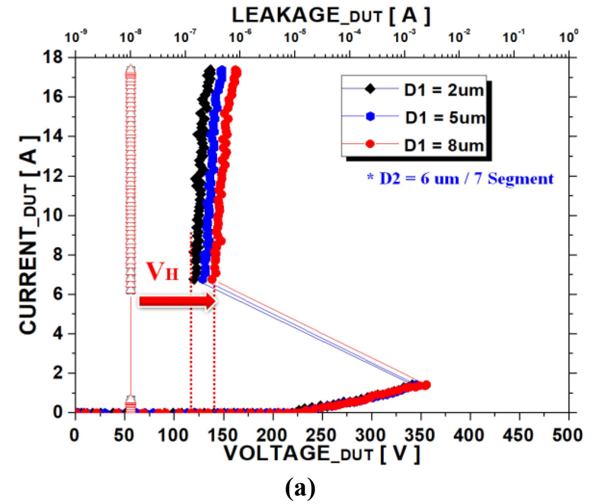
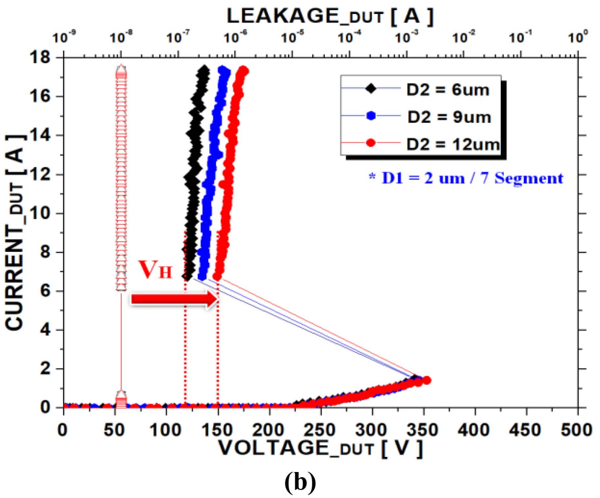


FIGURE 3. Layout of the proposed 4H-SiC ESD protection device including design variables D1 and D2 (a) 7 segments (b) 11 segments.

reach thermal breakdown (I_{t2}) in the TLP system used for measurement owing to the characteristics of 4H-SiC with very high thermal conductivity. Therefore, the current value was limited to 17 A, and a change in snapback characteristics was observed. Fig. 3 shows the layout, including the design variables for optimizing the electrical characteristics of the proposed device. The number of segments, length of the gate region (D1), and length of the N implant region (D2) were selected as the design variables, and a 1:1 segment ratio, which has the best efficiency, was applied. As the number of segments increases, the depletion region formed at the boundary of the emitter region decreases the effective emitters of the two parasitic bipolar transistor (Q_{p1}, Q_{n1}) and reduces the emitter injection efficiency, thereby inducing an increase in the holding voltage. As the design variable D1 increases, the base region of Q_{n1} increases, thereby inducing an increase in the holding voltage. The design variable D2 controls the effective base region of Q_{p1}.

Figs. 4 (a) and (b) show the TLP curves for which the design variables D1 and D2 of the proposed ESD protection device have been increased by 3 μm, respectively. As D1 increases by 6 μm at the maximum, the holding voltage of the proposed protection device increases to 138 V. In the case of D2, a significant increase in the holding voltage is induced with a maximum value of 148 V. This phenomenon is due to the doping concentration of each base region, and it occurred because the increase in the base current ($I_{b,Qn1}$) of Q_{p1} was larger as it had a relatively high concentration region. D1 affects the length of the P-well under the gate, and D2 affects the length of the high concentration N-drift. When the same length is achieved, the base with a higher doping concentration induces a significantly greater recombination in the base region compared to the base with a lower doping concentration. Moreover, the changes in the electrical characteristics of the proposed device according to the number of segments can be observed in Fig. 4 (c). In this experiment, given the device width and 4H-SiC process, the maximum number of segments was selected as 11, and the number of segments was increased by 2 from 7 to 11 in order to observe the electrical characteristics. According to the experimental results, the holding voltage of the proposed





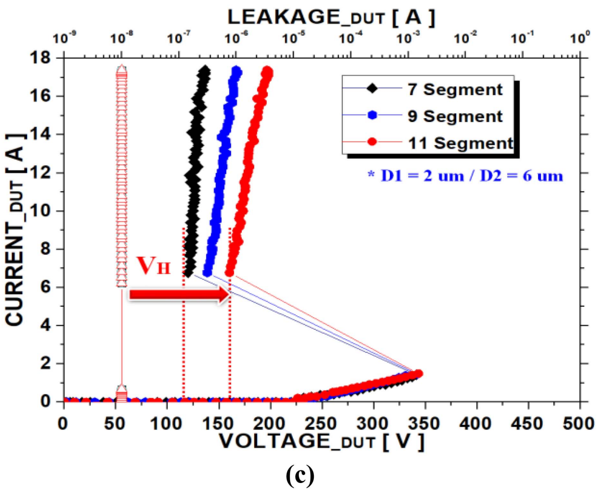


FIGURE 4. TLP curve measurement results based on the changes in the design variables (a) D1, (b) D2, and (c) number of segments.

device increased to a maximum of 162 V when the number of segments was 11. This indicates that the adjustment in the number of segments is highly effective in optimizing the holding voltage of the proposed device. Fig. 5 shows the V_{t1} and BV_{AK} of the proposed device resulting from the increase

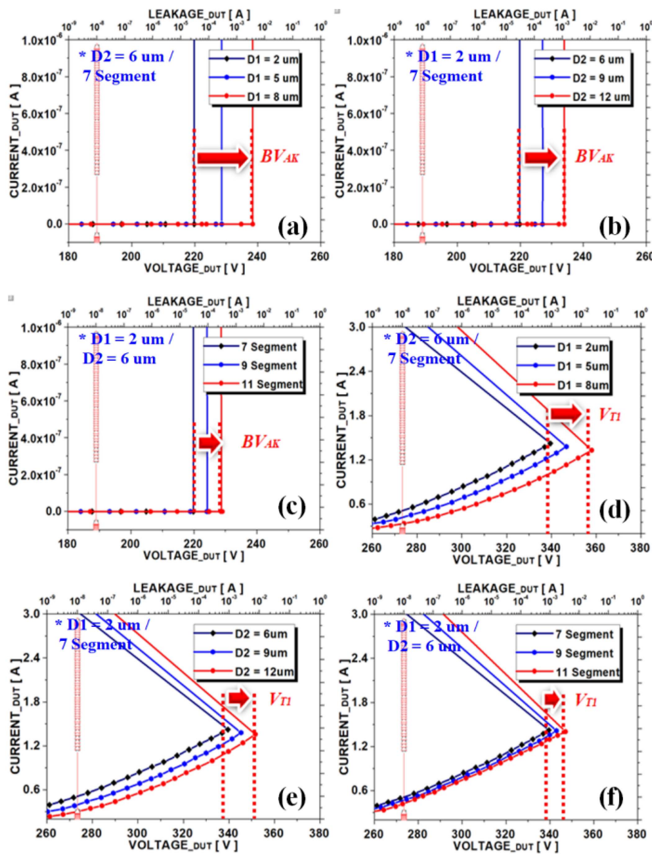


FIGURE 5. **Changes in the breakdown voltage according to each design variable: (a) D1, (b) D2, and (c) number of segments. Changes in the trigger voltage according to each design variable: (d) D1, (e) D2, and (f) number of segments.**

in each design variable. In 4H-SiC, while a number of EHP accumulated due to the very high breakdown voltage, the barrier of forward voltage drop that traps the carriers is about three times that of Si, and thus, the proposed device has a relatively high trigger current (I_{t1}) of 1.5 A. In addition, an increase in the length of the design variables leads to an increase in BV_{AK} and V_{t1} due to increasing the resistance across the device. As D1 increases, V_{t1} and BV_{AK} increase by 18 and 19 V, respectively. Moreover, as D2 increases, V_{t1} and BV_{AK} increase by 11 and 14 V, respectively. This occurs because the hole mobility of 4H-SiC is significantly low compared to the electron mobility. In contrast, the trigger voltage increases by 5 V according to the number of segments, whereas BV_{AK} increases by 9 V. These gains are small compared with the gains caused by adjusting the length of D1 and D2, indicating that the increase in resistance across the device is relatively small. Therefore, the proposed device can effectively improve the powerful snapback characteristics of the 4H-SiC environment by inducing a slight increase in the trigger voltage and a large increase in the holding voltage using the segment topology.

B. COMPARISON WITH CONVENTIONAL STRUCTURES

Fig. 6 compares the electrical characteristics of the conventional SCR, LIGBT, and proposed ESD protection

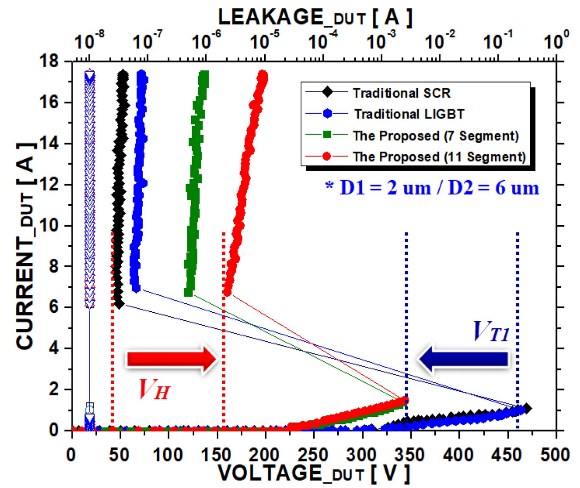


FIGURE 6. **Structures of the conventional SCR and LIGBT devices fabricated through the 4H-SiC process and TLP I–V curve of the proposed protection device.**

devices implemented using the 4H-SiC process. In this experiment, 7 and 11 segments—which result in the maximum holding voltage—were applied to the proposed device. The proposed device has a D1 of 2 μm and a D2 of 6 μm. It also has a relatively high on-resistance owing to the increased resistance in the ESD discharge path caused by the relatively wide drift length and the narrow emitter area resulting from the application of the segment topology. However, the existing devices have wide strong snapback waveforms because of the significantly large E_C and built-in potential difference in 4H-SiC. In contrast, owing to its structural features, the proposed device exhibits a reduction in BV_{AK} due to the low avalanche breakdown voltage and V_{t1} of approximately 340 V, according to the reduction in the OA region. Moreover, the proposed device has relatively high holding voltage characteristics—a holding voltage of 119 and 162 V for 7 and 11 segments, respectively. Therefore, the proposed device significantly overcomes the powerful snapback phenomenon occurring in 4H-SiC. In addition, considering the large operating area of SiC devices and circuits, the stacked proposed device with N-stack, shown in Fig. 7, can reach 620 V with four stacks and improved snapback [27]. Therefore, the proposed device can acquire a safe operating area required for high voltage applications with its relatively excellent area efficiency. Table 2 summarizes the electrical characteristics of the fabricated devices.

C. THERMAL RELIABILITY MEASUREMENT

4H-SiC semiconductors require operating voltage and high-temperature operations. To examine compatibility with 4H-SiC chips, the thermal reliability characteristics were evaluated. Particularly, a high-temperature environment is crucial because it reduces the mobility of carriers and significantly affects the snapback characteristics of the ESD protection device [28]. Changes in the electrical characteristics of the

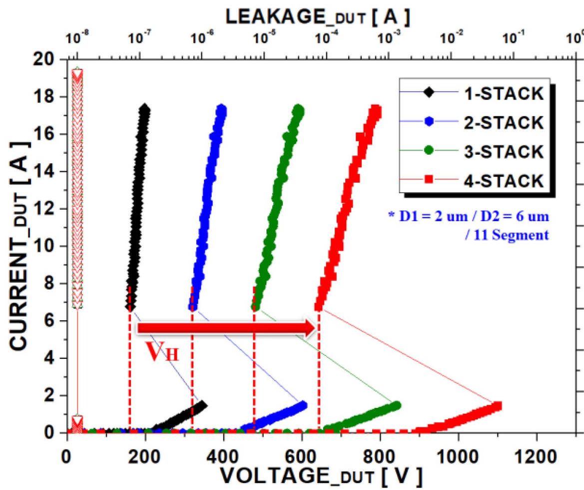


FIGURE 7. TLP measurement results for the proposed structures with N-stack numbers 1 to 4. The proposed device has 11 segmented anodes and cathodes with D1 and D2 of 2.0 and 6.0 μm, respectively.

TABLE 2. Summary of the snapback characteristics of all the fabricated experimental devices.

	Structure		Holding Voltage (V_h)	Holding Current (I_h)	Trigger voltage (V_{t1})	Breakdown Voltage (BV)
	SCR		42 V	6.22 A	421 V	310 V
	LIGBT		64 V	6.91 A	401 V	309 V
The Proposed	D1 (μm)	2	119 V	6.77 A	341 V	219 V
		5	128 V	6.75 A	345 V	228 V
		8	138 V	6.76 A	359 V	238 V
	D2 (μm)	6	119 V	6.77 A	341 V	219 V
		9	134 V	6.73 A	345 V	227 V
		12	148 V	6.70 A	352 V	233 V
	Segment No. (1:1)	7	119 V	6.77 A	341 V	219 V
		9	138 V	6.74 A	343 V	224 V
		11	162 V	6.70 A	346 V	228 V
	N-Stack	1	162 V	6.71 A	346 V	228 V
		2	314 V	6.71 A	609 V	445 V
		3	488 V	6.82 A	867 V	662 V
		4	622 V	6.88 A	1105 V	896 V

proposed device based on the temperature reliability experiment (300–500 K) can be observed in Fig. 8. In this experiment, 11 segments were used for the proposed device. According to the experimental results, the heat loss rate of the holding characteristics of the proposed device at a high temperature of 500 K is significantly low at >2%, and the holding voltage is considerably high at over 157 V. Moreover, the change rate of the trigger characteristics is significantly low at approximately 3%. Therefore, it was verified that the proposed ESD protection device has a stable high-temperature reliability owing to the material properties of 4H-SiC.

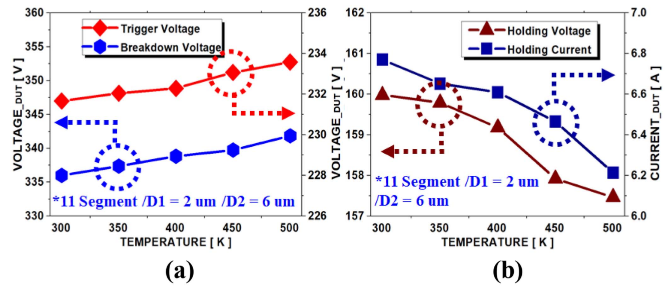


FIGURE 8. High temperature (300–500 K) experimental results for 1:1 segmented proposed device versus the (a) trigger voltage and breakdown voltage and (b) holding voltage and holding current.

IV. CONCLUSION

In this work, an LIGBT-based ESD protection device with a double-injection mechanism and enhanced trigger and holding characteristics was proposed to solve the issue of a wide range of snapbacks occurring in 4H-SiC. In addition, an operation analysis and optimization of the electrical characteristics were performed. The ESD protection devices in the 4H-SiC environment generate a wide range of snapback waveforms because of the significantly large critical electric field. Thus, a wide range of snapback greatly limits the practical application of ESD protection devices. In contrast, the proposed device significantly improves the snapback characteristics by structurally inducing an avalanche breakdown at low voltage and forming the effective base region of the parasitic bipolar transistor at a high doping concentration. Furthermore, the segment topology that has been modified appropriately for the proposed device can effectively optimize the holding voltage. Stable operation at a high temperature of 500 K was verified through a thermal reliability experiment. Moreover, the electrical characteristics of the stacked structure were evaluated, considering the large operational area of the SiC semiconductor. Low on-resistance and excellent thermal reliability can be achieved using the proposed device owing to the excellent material properties of 4H-SiC, along with the significantly-improved snapback characteristics. Therefore, it is expected that the proposed device will considerably improve the semiconductor reliability for high-voltage applications.

REFERENCES

[1] J. Zhang, Z. Chen, Y. Tu, X. Deng, and B. Zhang, "A novel SiC asymmetric cell trench MOSFET with split gate and integrated JBS diode," *IEEE J. Electron Devices Soc.*, vol. 9, pp. 713–721, 2021, doi: 10.1109/JEDS.2021.3097390.

[2] S. Ji, Z. Zhang, and F. Wang, "Overview of high voltage sic power semiconductor devices: Development and application," *CES Trans. Elect. Mach. Syst.*, vol. 1, no. 3, pp. 254–264, Sep. 2017, doi: 10.23919/TEMS.2017.8086104.

[3] C. Codreanu, M. Avram, E. Carbunescu, and E. Iliescu, " Comparison of 3C–SiC, 6H–SiC and 4H–SiC MESFETs performances," *Mater. Sci. Semicond. Process.*, vol. 3, nos. 1–2, pp. 137–142, 2000, doi: 10.1016/S1369-8001(00)00022-6.

[4] W.-C. Lien, N. Damrongplasit, J. H. Paredes, D. G. Senesky, T.-J. K. Liu, and A. P. Pisano, "4H-SiC N-channel JFET for operation in high-temperature environments," *IEEE J. Electron Devices Soc.*, vol. 2, pp. 164–167, 2014, doi: 10.1109/JEDS.2014.2355132.

[5] J. An and S. Hu, "Experimental and theoretical demonstration of temperature limitation for 4H-SiC MOSFET during unclamped inductive switching," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 206–214, Mar. 2020, doi: 10.1109/JESTPE.2019.2944167.

[6] L. Yang *et al.*, "Analysis of mobility for 4H-SiC N/P-channel MOSFETs up to 300 °C," *IEEE Trans. Electron Devices*, vol. 68, no. 8, pp. 3936–3941, Aug. 2021, doi: 10.1109/TED.2021.3084908.

[7] J. Qi *et al.*, "Temperature dependence of dynamic performance characterization of 1.2-kV SiC power mosfets compared with Si IGBTs for wide temperature applications," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 9105–9117, Sep. 2019, doi: 10.1109/TPEL.2018.2884966.

[8] M. Alexandru *et al.*, "SiC integrated circuit control electronics for high-temperature operation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 3182–3191, May 2015, doi: 10.1109/TIE.2014.2379212.

[9] J. Wei, S. Liu, X. Zhang, W. Sun, and A. Q. Huang, "Modeling avalanche induced degradation for 4H-SiC power MOSFETs," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11299–11303, Nov. 2020, doi: 10.1109/TPEL.2020.2984650.

[10] P. Denis *et al.*, "Robustness of 4H-SiC 1200 V Schottky diodes under high electrostatic discharge like human body model stresses: An in-depth failure analysis," *Diam. Related Mater.*, vol. 44, pp. 62–70, 2014, doi: 10.1016/j.diamond.2014.02.002.

[11] O. Semenov, H. Sarbishaei, and M. Sachdev, *ESD Protection Device and Circuit Design for Advanced CMOS Technologies*. Dordrecht, The Netherlands: Springer, 2008.

[12] S. S. Chowdhury and F. Arifin, "The effects of the substrate doping concentrations on 6H-SiC nano-scale ggNMOS ESD protection device," in *Proc. Int. Conf. Robot. Elect. Signal Process. Techn.*, 2021, pp. 329–333, doi: 10.1109/ICREST51555.2021.9331030.

[13] T. Phulpin *et al.*, "Contribution to silicon-carbide-MESFET ESD robustness analysis," *IEEE Trans. Device Mater. Rel.*, vol. 18, no. 2, pp. 214–223, Jun. 2018, doi: 10.1109/TDMR.2018.2817255.

[14] F. Du *et al.*, "Novel symmetrical dual-directional SCR with p-type guard ring for high-voltage ESD protection," *IEEE Trans. Electron Devices*, vol. 68, no. 8, pp. 4164–4167, Aug. 2021, doi: 10.1109/TED.2021.3091658.

[15] R.-K. Chang, B.-W. Peng, and M.-D. Ker, "Schottky-embedded silicon-controlled rectifier with high holding voltage realized in a 0.18-μm low-voltage CMOS process," *IEEE Trans. Electron Devices*, vol. 68, no. 4, pp. 4164–4167, Apr. 2021, doi: 10.1109/TED.2021.3059193.

[16] K. I. Do, B. S. Lee, and Y. S. Koo, "LIGBT-based ESD protection device with high holding voltage for 15 V power IC applications," *J. Semicond. Technol. Sci.*, vol. 19, no 5, pp. 470–476, 2019, doi: 10.5573/JSTS.2019.19.5.470.

[17] R. Ye *et al.*, "Influence of latch-up immunity structure on ESD robustness of SOI-LIGBT used as output device," *IEEE Trans. Device Mater. Rel.*, vol. 18, no. 2, pp. 284–290, Jun. 2018, doi: 10.1109/TDMR.2018.2829550.

[18] P. Lai *et al.*, "Investigation of ESD protection in SiC BCD process," in *Proc. IEEE 7th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, 2019, pp. 405–409, doi: 10.1109/WiPDA46397.2019.8998959.

[19] K.-I. Do, B.-S. Lee, and Y.-S. Koo, "Study on 4H-SiC GGNMOS based ESD protection circuit with low trigger voltage using gate-body floating technique for 70-V applications," *IEEE Electron Device Lett.*, vol. 40, no. 2, pp. 283–286, Feb. 2019, doi: 10.1109/LED.2018.2885846.

[20] A. Amerasekera, C. Duvvury, W. Anderson, H. Gieser, and S. Ramaswamy, *ESD in Silicon Integrated Circuits*. Chichester, U.K.: Wiley, 2002.

[21] W.-Y. Chen, M.-D. Ker, and Y.-J. Huang, "Investigation on the validity of holding voltage in high-voltage devices measured by transmission-line-pulsing (TLP)," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 762–764, Jul. 2008, doi: 10.1109/LED.2008.2000910.

[22] K.-I. Do, B. Lee, S. G. Kim, and Y.-S. Koo, "Design of 4H-SiC-based silicon-controlled rectifier with high holding voltage using segment topology for high-voltage ESD protection," *IEEE Electron Device Lett.*, vol. 41, no. 11, pp. 1669–1672, Nov. 2020, doi: 10.1109/LED.2020.3022888.

[23] X. Huang, J. J. Liou, Z. Liu, F. Liu, J. Liu, and H. Cheng, "A new high holding voltage dual-direction SCR with optimized segmented topology," *IEEE Electron Device Lett.*, vol. 37, no. 10, pp. 1311–1313, Oct. 2016, doi: 10.1109/LED.2016.2598063.

[24] Z. Liu, J. J. Liou, and J. Vinson, "Novel silicon-controlled rectifier (SCR) for high-voltage electrostatic discharge (ESD) applications," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 753–755, Jul. 2008, doi: 10.1109/LED.2008.923711.

[25] L. Zhu, T. P. Chow, K. A. Jones, and A. Agarwal, "Design, fabrication, and characterization of low forward drop, low leakage, 1-kV 4H-SiC JBS rectifiers," *IEEE Trans. Electron Devices*, vol. 53, no. 2, pp. 363–368, Feb. 2006, doi: 10.1109/TED.2005.862704.

[26] A. Z. H. Wang, *On-Chip ESD Protection for Integrated Circuits: An IC Design Perspective*. Boston, MA, USA: Kluwer Acad. Publ., 2002.

[27] F. Ma *et al.*, "High holding voltage SCR-LDMOS stacking structure with ring-resistance-triggered technique," *IEEE Electron Device Lett.*, vol. 34, no. 9, pp. 1178–1180, Sep. 2013, doi: 10.1109/LED.2013.2272591.

[28] F. Hou *et al.*, "New diode-triggered silicon-controlled rectifier for robust electrostatic discharge protection at high temperatures," *IEEE Trans. Electron Devices*, vol. 66, no. 4, pp. 2044–2048, Apr. 2019, doi: 10.1109/TED.2019.2900052.