Received 2 July 2021; revised 23 September 2021 and 8 October 2021; accepted 15 October 2021. Date of publication 19 October 2021; date of current version 1 November 2021. The review of this article was arranged by Editor S. Reggiani.

Digital Object Identifier 10.1109/JEDS.2021.3121132

An RF Stress-Based Thermal Shock Test Method for a CMOS Power Amplifier

SHAOHUA ZHOU [1,2] (Student Member, IEEE), AND JIAN WANG [1,2]

1 School of Microelectronics, Tianjin University, Tianjin 300072, China
2 Qingdao Institute for Ocean Technology, Tianjin University, Qingdao 266200, China

CORRESPONDING AUTHOR: J. WANG (e-mail: wangjian16@tju.edu.cn)

This work was supported in part by the National Natural Science Foundation of China under Grant 62031008, and in part by the Qingdao National Laboratory for Marine Science and Technology of China under Grant QNLM2016ORP0411.

ABSTRACT To accelerate the degradation of critical specifications of CMOS power amplifiers (PAs), this paper proposes a new measurement method that introduces radio frequency (RF) stress in the thermal shock test of CMOS PAs. The experimental results show that the proposed method is effective. The degradation of key PA specifications such as output power and power-added efficiency can accelerate under RF stress. Its degradation speed is faster than that under no RF stress. Possible reasons for the degradation of crucial PA specifications accelerated by RF stress are discussed and analyzed in detail in this paper. The method proposed in this paper can effectively reduce the measurement time and cost to study the degradation of critical specifications of the CMOS-based PA. This method can be used for scientific research on the performance degradation of microwave/RF circuits and devices and aging experiments of electronic products before they leave the factory.

INDEX TERMS Thermal shock test, radio frequency stress, CMOS power amplifier, performance degradation.

I. INTRODUCTION

The CMOS power amplifier (PA) is one of the critical components in the wireless transmitter [1], which is widely used by multiple applications, such as commercial and military radars, phased-array systems, and communication satellites [2]. As the wireless world continues to expand, applications above are more likely to be exposed to severe environments such as low, high-temperature conditions [3]. The reliable operation of PAs in harsh environments such as high or low temperatures is critical to the above applications since the performance of PAs has a significant temperature dependence [4]. Performance variation of a PA in harsh environments such as high or low temperatures can adversely affect the reliability and stability of the overall radio system [5]–[6]. Therefore, there is a strong motivation to provide temperature-robust power amplifiers in low-cost silicon technologies [7]. To achieve a temperature-robust power amplifier, it is necessary to understand the performance of the PA concerning temperature.

The relationship between PA performance and temperature has been a hot topic of research. Previous research has focused on PA performance at specific typical temperature points such as 23°C [8], 25°C [7], 125°C [9], etc., or PA performance in a specific temperature range such as −20 to 120°C [10], −40 to 125°C [11], 10 to 100°C [4], etc. However, there is limited experimental analysis data in the literature reporting on the performance of PA concerning sharp temperature changes since the PA may work not only in low or high-temperature environments but also in environments with rapid temperature changes such as deserts, coastal areas, Mars (Tianwen-1 and Curiosity Mars Rovers), etc. When the temperature changes drastically, the performance of PA will be seriously affected or even fail [10]. Therefore, there is an urgent need to study the performance of PAs concerning sharp temperature changes, to understand the degradation mechanism of PA performance specifications under abrupt changes in external temperature, and to develop design guidelines for temperature-robust PAs

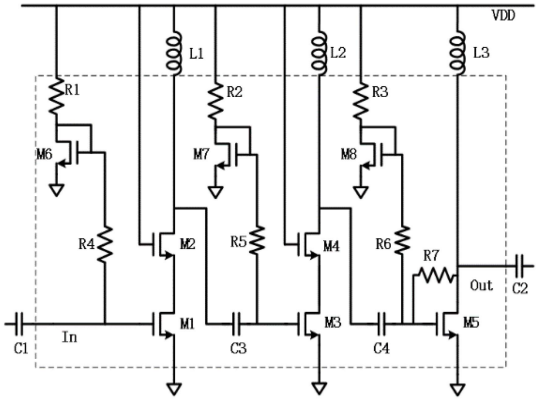

FIGURE 1. A detailed schematic diagram of the CMOS PA.

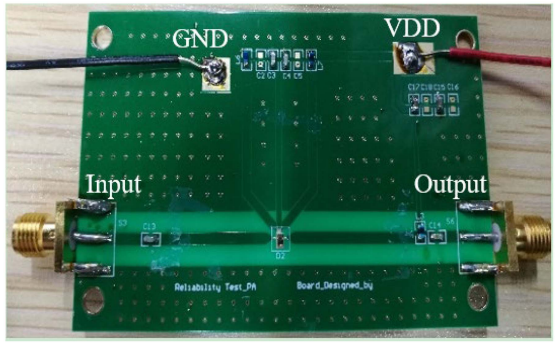

FIGURE 2. The photograph of the 0.1-1.2 GHz CMOS PA.

TABLE 1. The key specifications of the PA.

Items	Specifications
DC Current	87.2 mA@400 MHz (Pin=-10 dBm)
Gain	16.27 dB@400 MHz (Pin=-10 dBm)
Saturation output power	19.35 dBm@400 MHz

so that temperature-robust PAs can be realized using low-cost silicon technology [12].

In this paper, a 0.1-1.2 GHz CMOS PA has been fabricated and tested under thermal shock test with RF stress from −40°C to 125°C. The thermal shock test can well evaluate the performance of PA under extreme temperature changes [13], but the testing time of the thermal shock test is prolonged [14]–[15]. In this paper, RF stress is introduced into the thermal shock test, which can well evaluate the performance of PA under extreme temperature change and dramatically shortens the testing time of the thermal shock test. The experimental results show that when the number of thermal shock cycles is the same, the degradation of PA specifications under RF stress is greater than that of PA specifications without RF stress. This indicates that the time required under RF stress is less than that needed without RF stress to achieve the same degradation effect. This indicates that RF stress can effectively shorten the test time of the thermal shock test and thus reduce the test cost.

The remainder of this paper has been organized as follows: Section II describes the designed power amplifier and the experimental setup. The experimental results and discussion are detailed in Section III. Finally, the conclusions are summarized in Section IV.

II. DESIGNED PA AND EXPERIMENTAL SETUP

A. THE DESIGNED PA

Here, a 0.1-1.2 GHz CMOS PA first has been designed and fabricated as the sample for the thermal shock test [16]. A detailed schematic of this CMOS PA is shown in Fig. 1. The input and output capacitors C1 and C2 and all the RF-choke inductors (L1-L3) are off-chip. This PA employs a cascode topology at the first two stages and a common-source structure with resistive shunt feedback at the last stage. The on-chip DC blocking capacitors C3 and C4 at the inter-stage are set to 20 pF to extend the bandwidth down to 100 MHz. The first stage is a driver stage with a cascode structure for high gain and good input matching. This topology consists of two transistors M1 and M2. Transistor M2 is stacked on M1, providing good isolation because of its high output impedance. Inductor L1 is chosen large enough to feed DC power to the drain as an RF choke. This CMOS PA is fabricated in a 0.18 μm CMOS process, and the chip is directly bonded on the PCB. Fig. 2 shows the photograph of the 0.1-1.2 GHz CMOS PA, which is self-developed.

The PA with a 3.3 V supply voltage was tested at room temperature (25°C) using the DC Current Source (R&S HMP4040), Signal Source (Agilent E8257D), and Spectrum Analyzer (Agilent E4440A) before the thermal shock test. The key specifications of the PA operated at room temperature are shown in Table 1.

B. THERMAL SHOCK TEST

To study the performance of PAs concerning sharp temperature changes, a thermal shock test was conducted in Vötsch VT^3 7006 S2 test chamber, as shown in Fig. 3. In the test chamber, the temperature conditioning of the hot zone is from +50°C to +220°C (Optional to +250°C) and the temperature conditioning of the cold zone from −80°C to +70°C. And the Vötsch VT^3 7006 S2 test chamber has a large port for the supplied measurement of specimens. The temperature range of the cables used in this experiment is −55°C to 125°C, according to the datasheet of GORE cables. While the maximum temperature in the hot zone of the chamber can reach 250°C, the minimum temperature in the cold zone can reach −80°C. Therefore, to ensure the validity of the experimental data and protect the cable from damage. Thus, the temperature range of the thermal shock experiment is set to −40°C to 125°C in the experimental setup. The specific revisions are as follows.

The 0.1-1.2 GHz CMOS PA was cycled from −40°C to +125°C by dwelling at each temperature extreme for 15 min, as shown in Fig. 4a. Each cycle is completed in 30 min. As shown in Fig. 4b, the input power is 15 dBm during each thermal cycle and returns to −20 dBm. After five thermal

FIGURE 3. Thermal shock test environment.

cycles for preparation, and then the actual measurement begins. This temperature profile is chosen to mimic the environmental conditions that a typical chip will experience in service. RF measurements are performed every 5 thermal cycles, for up to a maximum of 280 thermal cycles. All measurements are performed at room temperature.

The configuration of experimental equipment for measuring the critical specification degradation of the PA under the Thermal-shock test is shown in Fig. 5. This experiment uses an R&S HMP4040, Agilent E8257D, and Agilent E4440A as DC power supply, RF generator, and analyzer. In addition, we added a 30 dB attenuator between the PA's output and the input of the spectrum analyzer to avoid damage to the spectrum analyzer due to excessive power.

III. EXPERIMENTAL RESULTS AND DISCUSSION

A. DC CURRENT

The change in the DC Current of the PA under thermal-shock test with and without RF stress, as a function of thermal cycling and input power, is shown in Fig. 6.

From Fig. 6, the measured DC Current degraded with thermal cycling. For instance, at an input power of 12 dBm, the DC Current changed from an original value of 124.8 mA to 121.6 mA after 25 thermal cycles without RF stress. Upon further cycling to 105 thermal cycles without RF stress, the DC Current deteriorated further to 116.4 mA. However, when the input power is also 12 dBm, the DC current of PA degrades to 120.1 mA and 112.6 mA after 25 and 105 thermal cycles under RF stress, respectively. This shows that the magnitude of the degradation of the DC current of the PA under RF stress is relatively increased by 45.2% compared to that without RF stress. This illustrates that the introduction of RF stress in the thermal shock test can effectively accelerate the degradation of the DC current of the PA.

One possible reason RF stress can accelerate the DC degradation of the PA is that the carriers in the channel receive more energy under RF stress, making their average energy greater, thus leading to more hot-carrier injection [17]. As a result, the threshold voltage will increase with hot carrier injection [18].

The drain currents in the linear and nonlinear regions, respectively, can be expressed by (1) and (2) [19]:

$$I_{ds} = \frac{W_g \mu_n C_{ox}}{2L_g}\left[2(V_{gs} - V_{th})V_{ds} - V_{ds}^2\right] \tag{1}$$

$$I_{ds} = \frac{W_g \mu_n C_{ox}}{2L_g}(V_{gs} - V_{th})^2 \tag{2}$$

where W_g is the gate width, μ_n is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, L_g is the gate length, V_{gs} is the gate voltage, V_{th} is the threshold voltage, and V_{ds} is drain voltage.

According to (1) and (2), the drain current of PA degrades with the increase of threshold voltage. That is, the drain current of the PA degrades with the injection of hot carriers. This means that degradation of the DC current is accelerated under RF stress, which is also consistent with the results reported in [17].

B. OUTPUT POWER

Figure 7 shows the measured output power of the PA operating at 433 MHz as a function of thermal cycling. At an input power of 15 dBm, before thermal cycling, the output power of the PA is 18.91 dBm. Upon cycling to 25 thermal cycles without RF stress, the output power was 18.54 dBm, representing a degradation of 0.37 dBm. After 105 thermal cycles without RF stress, the output power degraded to 18.06 dBm.

However, when the input power is also 15 dBm, the output power of the PA degrades to 18.41 dBm and 17.52 dBm after 25 and 105 thermal cycles under RF stress, respectively. This shows that after 105 thermal cycles, the output power of the PA degrades by 1.39 dBm and 0.85 dBm with and without RF stress, respectively. It means that the PA's output power degradation under RF stress is relatively increased by 63.5% compared to without RF stress. Like DC current, RF stress can likewise accelerate the degradation of the PA's output power. The cause of the accelerated degradation of the output power of the PA is also the RF stress that leads to more hot-carrier injection.

The channel resistance may be approximated as [20]:

$$R_{DS} \approx \frac{L_g}{\mu_n C_{ox} W_g (V_{gs} - V_{th})} \tag{3}$$

It is evident from Section III-A that RF stress will increase the threshold voltage. According to (3), the channel resistance will increase as the threshold voltage increases. The literature shows that the power consumption of the power amplifier will increase as the channel resistance increases, resulting in a decrease in the output power of the power amplifier [21]. As a result, the output power of the PA degrades more quickly under RF stress than without RF stress.

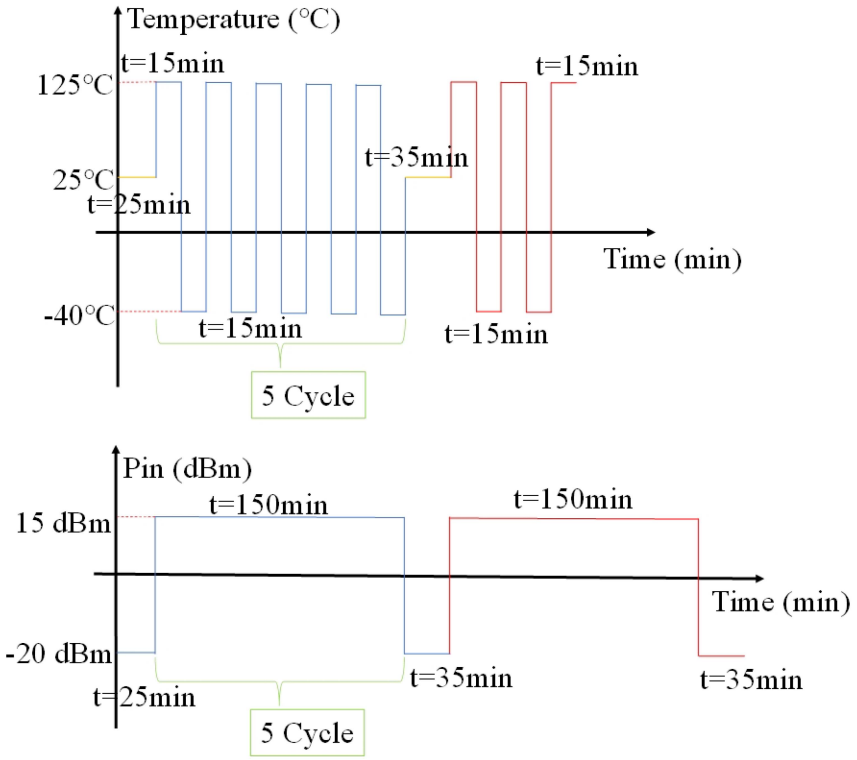

FIGURE 4. Schematic representation and diagram of the input power curve used during the thermal cycle.

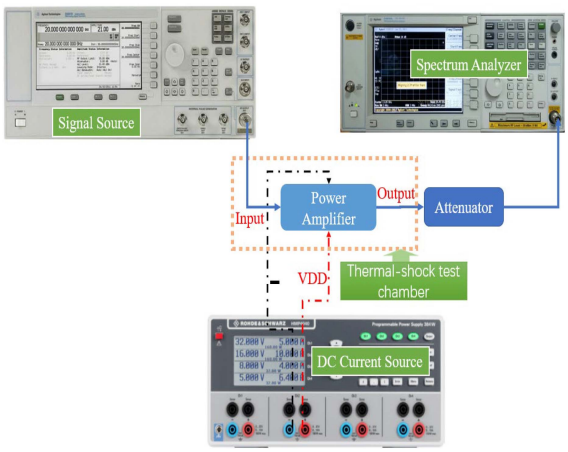

FIGURE 5. Configuration of experimental equipment for measuring the specification degradation of the PA under Thermal-shock test.

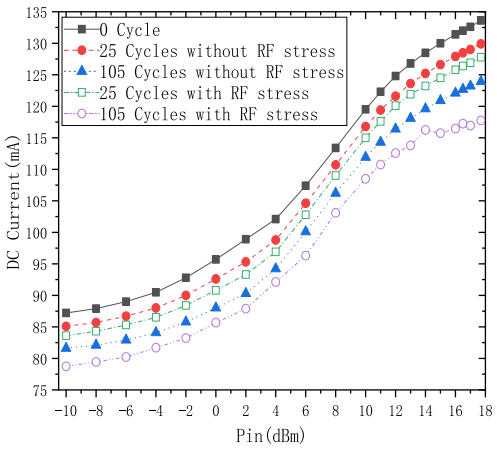

FIGURE 6. Effect of thermal cycling on the DC Current.

C. GAIN

The Gain of the PA operating at 433 MHz is presented in Fig. 8. Figure 8 shows the measured Gain of the PA as a function of thermal cycling and input power.

At input powers of −6 dBm and 13 dBm, the Gain of the PA degrades by 1.46 dB and 0.81 dB after 105 thermal cycles without RF stress, respectively. Under the same input power of −6 dBm and 13 dBm, the Gain of the PA decreased by 3.3 dB and 1.63 dB after 105 thermal cycles under RF stress, respectively. Under the action of RF stress, the PA gain degradation amplitude relatively increased by 126% (Pin = −6 dBm) and 101.2% (Pin = −13 dBm) when compared with no RF stress effect. Like DC current and output power, the Gain of the PA degrades more under RF stress than without RF stress. This degradation also occurs due to more hot-carrier injection caused by RF stress. The Gain of PA can be expressed as [21]:

$$Gain = P_{out} - P_{in} \tag{4}$$

where P_{out} is the output power, P_{in} is the input power.

In Section III-B, it has been discussed and analyzed that the output power of the PA degrades with more hot-carrier injection. From (4), it is known that the Gain of the PA degrades with the degradation of the output power.

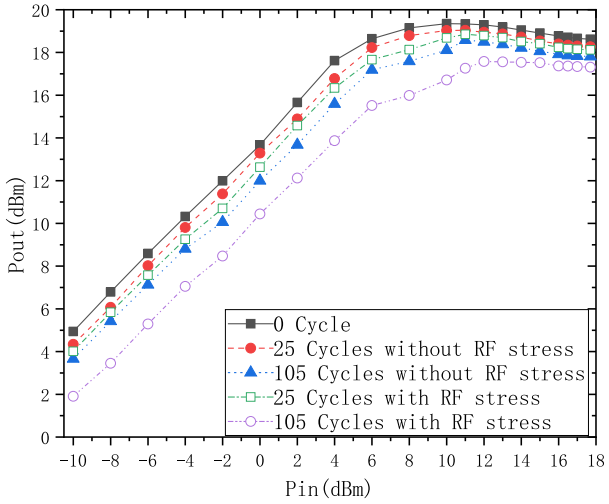

FIGURE 7. Effect of thermal cycling on the output power.

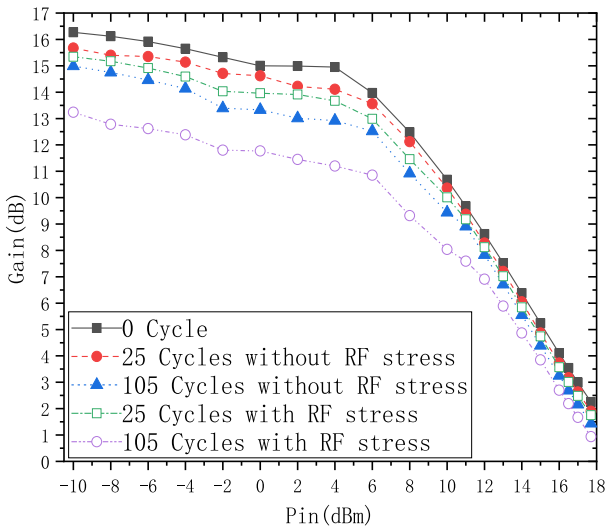

FIGURE 8. Effect of thermal cycling on the Gain.

Therefore, it also follows that the Gain of the PA degrades with more hot-carrier injection.

D. POWER ADDED EFFICIENCY

The power added efficiency of the PA operating at 433 MHz under thermal-shock test with and without RF stress is performed and shown in Fig. 9. When the input power of the PA is 6 dBm, after 105 thermal cycles, with and without RF stress, the PA of the PA degrades by 9.5% and 4.8%, respectively. However, when the input power of the PA is 11dBm, after 105 thermal cycles, with and without RF stress, the PA of the PA degrades by 7% and 2.3%, respectively. Thus, under the action of RF stress, the degradation of PAE of PA is relatively increased by 35.7% (Pin = 6 dBm) and 108.7% (Pin = 11 dBm) compared to the absence of RF stress.

The PAE of PA is not only related to the thermal cycle but also the input power. In addition, the PAE of PA degrades more with the increase of thermal cycling under RF stress.

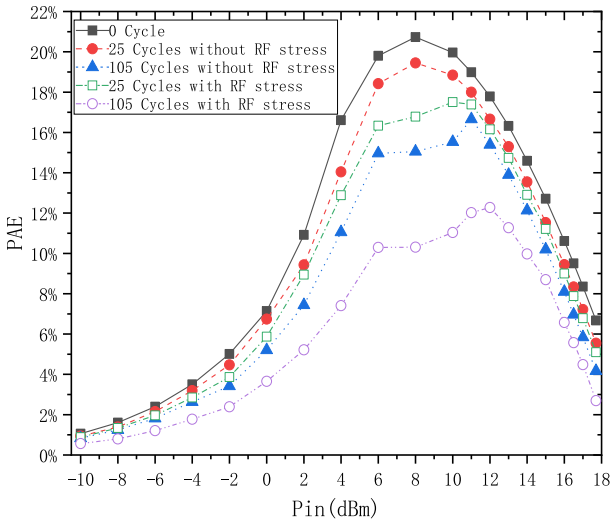

FIGURE 9. Effect of thermal cycling on the PAE.

Therefore, the cause of accelerated PAE degradation of PAs is also due to more hot-carrier injection caused by RF stress.

For a typical class A PA, the expression for the PAE is [22]:

$$PAE = \frac{P_{out} - P_{in}}{V_D I_D} \times 100\% \leq \left(\frac{1}{2} - \frac{P_{in}}{V_D I_D}\right) \times 100\% \quad (5)$$

where V_D is the DC voltage, I_D is the DC current.

Through the discussion and analysis in Section III-A, it is already known that the DC current of the PA degrades with the injection of more hot carriers. Furthermore, according to (5), it is known that the PAE of PA will degrade with the degradation of DC current. Therefore, this also explains that RF stress can accelerate the degradation of PAE of PA.

Through the previous discussion and analysis, we know that the critical specifications of the PA, such as DC current, output power, PAE, and gain, also degrade with the increase of the number of thermal shocks without adding RF stress. However, after introducing the RF stress equipped with the same number of shocks, the degradation of the critical specifications of the PA is significantly greater than that without adding RF stress. This indicates that the introduction of RF stress can dramatically improve the degradation of the critical specifications of PA.

Almost all electronic products (such as various microwave/mm-wave devices and circuits) must be subjected to aging experiments before leaving the factory to achieve a satisfactory product qualification rate. So, how can manufacturers improve their efficiency without compromising the aging effect? The method proposed in this paper can be directly used for the aging testing of electronic products to reduce and shorten the cost and time problems caused by the aging process. Therefore, it is of great significance for the improvement of manufacturers' economic efficiency.

Besides the earlier discussion and analysis, we believe that one of the main reasons for the degradation of the critical specifications of the PA due to the introduction of RF stress is the hot carrier injection, which is also consistent with

the results reported in the literature [17]. However, there is another possible cause in addition to the hot carrier injection caused by the introduction of RF stress. This cause is the formation of cracks at the solder joint interface (as shown in Figure 2) due to the mismatch of the coefficient of thermal expansion of the material under the high and low-temperature impact, which makes the resistance of the solder joint increase [23]. The increase in the resistance of the solder joint will increase the Joule heat generated by the solder joint and a decrease in the current, which will eventually reduce the output power, gain, and PAE of the PA.

This means that after the introduction of RF stress, there are two main reasons for the degradation of the critical specifications of the PA-(1) the hot carrier injection caused by RF stress, and (2) the added resistance at the solder joints mainly due to the variable thermal shocks.

In the absence of RF stress, the main cause of degradation of the critical specifications of the PA (which is normally powered) is the increase in solder joint resistance due to high and low-temperature shock. However, suppose the PA is not powered, and a high or low-temperature shock is applied. In that case, the critical specifications of the PA will still degrade, and the cause of this degradation is the increase in solder joint resistance caused by the high and low-temperature thermal shocks. In this case, it may be noted that the magnitude of degradation is relatively small. This is because, without power, the joint will only form a few microcracks at the interface during the high and low-temperature shock [23].

IV. CONCLUSION

In this paper, the effect of thermal cycling on the critical specifications of PA is investigated using the thermal shock test with RF stress. The experimental results show that introducing RF stress in thermal shock tests can accelerate the degradation of crucial PA specifications such as output power and power-added efficiency. There are two possible causes for the degradation of PAs' critical specifications. One is hot carrier injection due to RF stress, and the other is the enhanced resistance at the solder joints mainly due to the variable thermal shocks.

At the same thermal cycle, the present method accelerates the degradation of the critical specifications of PA and significantly reduces the measurement time. Thus, the applications of the proposed method are two-fold. First, it can be used for scientific research based on the degradation of RF/microwave circuit performance, which would reduce the time required for measurements. Second, it can be used in the aging experiments of the electronic products before they leave the factory, reducing and shortening the cost and time problems caused by the aging process.

REFERENCES

[1] C.-Y. Li, T. Yoshida, K. Katayama, M. Motoyoshi, and M. Fujishima, "Evaluation of temperature dependence and lifetime of 79 GHz power amplifier," in *Proc. IEEE Int. Meeting Future Electron Devices*, 2013, pp. 100–101.

[2] A. Alizadeh, M. Yaghoobi, M. Meghdadi, A. Medi, and S. Kiaei, "A 10-W X-band class-F high-power amplifier in a 0.25-μm GaAs pHEMT technology," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 1, pp. 157–169, Jan. 2021.

[3] T. Y. Kang and D. Seo, "The effect of temperature on performance of a RF CMOS power amplifier and bond wires," in *Proc. IEEE 24th Elect. Perform. Electron. Packag. Syst.*, 2015, pp. 69–72.

[4] M. Motoyoshi, K. Takano, T. Yoshida, K. Katayama, S. Amakawa, and M. Fujishima, "79 GHz CMOS power amplifier using temperature compensation bias," in *Proc. 9th Eur. Microw. Integr. Circuit Conf.*, 2014, pp. 49–52.

[5] F. L. Pour and D. S. Ha, "A temperature compensated 5 GHz GAN on SiC power amplifier," in *Proc. IEEE 63rd Int. Midwest Symp. Circuits Syst. (MWSCAS)*, 2020, pp. 549–553.

[6] M. A. Alim, A. A. Rezazadeh, and C. Gaqiere, "Temperature dependence of the threshold voltage of AlGaN/GaN/SiC high electron mobility transistors," *Semicond. Sci. Technol.*, vol. 31, no. 12, Nov. 2016, Art. no. 125016.

[7] D. del Rio, I. Gurutzeaga, A. Beriain, H. Solar, and R. Berenguer, "A compact, wideband, and temperature robust 67–90-GHz SiGe power amplifier with 30% PAE," *IEEE Microw. Wireless Compon. Lett.*, vol. 29, no. 5, pp. 351–353, May 2019.

[8] Q. Lin, Q.-F. Cheng, J.-J. Gu, Y. Zhu, C. Chen, and H.-P. Fu, "Design and temperature reliability testing for A 0.6–2.14 GHz broadband power amplifier," *J. Electron. Test.*, vol. 32, no. 2, pp. 235–240, Feb. 2016.

[9] S. H. Zhou, "Experimentally investigating the degradations of the GaN PA indexes under different temperature conditions," *Microwave Opt. Technol. Lett.*, vol. 63, no. 3, pp. 758–763, Mar. 2021.

[10] Q. Lin, H. Wu, and X. Li, "Study of temperature reliability for a parallel high-efficiency class-E power amplifier," *Circuit World*, vol. 43, no. 3, pp. 111–117, Aug. 2017.

[11] J. G. Ma and S. Zhou, "Experimentally investigating the performance degradations of power amplifiers against temperatures," in *Proc. Int. Conf. Microwave Millimeter Wave Technol. (ICMMT)*, Shanghai, China, 2020, pp. 1–3.

[12] X. Liu, C. Qiao, V. Sundaram, R. T. Rao, and S. K. Sitaraman, "Failure analysis of through-silicon vias in free-standing wafer under thermal-shock test," *Microelectron. Rel.*, vol. 53, no. 1, pp. 70–78, Jan. 2013.

[13] J. Pippola, T. Marttila, and L. Frisk, "Protective coatings of electronics under harsh thermal shock," *Microelectron. Rel.*, vol. 54, nos. 9–10, pp. 2048–2052, Aug. 2014.

[14] C. Okoro, P. Kabos, J. Obrzut, K. Hummler, and Y. S. Obeng, "Accelerated stress test assessment of through-silicon via using RF signals," *IEEE Trans. Electron Devices*, vol. 60, no. 6, pp. 2015–2021, Jun. 2013.

[15] M. Tsai, C. Chen, and W. Tsai, "Thermal resistance and reliability of high-power LED packages under WHTOL and thermal shock tests," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 33, no. 4, pp. 738–746, Dec. 2010.

[16] H.-F. Wu, L.-G. Wang, P. Zhou, and J.-G. Ma, "A 0.1–1.2 GHz CMOS ultra-broadband power amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2014, pp. 1–3.

[17] C. Liu, R. Wang, Y. Su, C. Tu, and Y. Juang, "Degeneration of CMOS power cells after hot-carrier and load mismatch stresses," *IEEE Electron Device Lett.*, vol. 29, no. 9, pp. 1068–1070, Sep. 2008.

[18] T. Quémerais *et al.*, "Hot-carrier stress effect on a CMOS 65-nm 60-GHz one-stage power amplifier," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 927–929, Sep. 2010.

[19] D. A. Neamen, *Semiconductor Physics and Devices: Basic Principles*. New York, NY, USA: McGraw-Hill, 2011, pp. 387–410.

[20] J. S. Yuan and J. Ma, "Evaluation of RF-stress effect on class-E MOS power-amplifier efficiency," *IEEE Trans. Electron Devices*, vol. 55, no. 1, pp. 430–434, Jan. 2008.

[21] S. H. Zhou, "Experimental investigation on the performance degradations of the GaN class-F power amplifier under humidity conditions," *Semicond. Sci. Technol.*, vol. 36, no. 3, Feb. 2021, Art. no. 035025.

[22] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*. 2nd ed. Boston, MA, USA: Artech House, 2006.

[23] H. Hao, Y. Zuo, Y. Lu, Y. L. Song, and H. Guo, "Failure mechanism of the lead-free solder joints during the coupling effect between electromigration and high and low temperature impact," *Electron. Compon. Mater.*, vol. 31, no. 8, pp. 77–79, Aug. 2012.