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Ferroelectric-Like Non-Volatile FET With Amorphous Gate Insulator for Supervised Learning Applications

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ABSTRACT We experimentally demonstrate ferroelectric-like non-volatile field-effect transistor (NVFET) with the amorphous Al_2O_3 gate insulator for artificial synapse applications. The switchable polarization (P) is attributed to the voltage modulation of mobile ions in the gate insulator. The ferroelectric-like NVFETs integrated with 3 nm and 6 nm-thick Al_2O_3 dielectrics demonstrate the capability to mimic various synaptic behaviors including long-term potentiation (LTP), long-term depression (LTD), and spike-timing-dependent plasticity (STDP), under different types of electrical stimuli to the gate electrode. To verify the application of the ferroelectric-like transistors in the Spike Neural Network (SNN), the online training has been carried out based on the synaptic characteristics of the devices, and a decent accuracy ($>$80%) is achieved for fixed-amplitude $\pm$3 V/100 ns potentiation/depression pulses.

INDEX TERMS Amorphous, FET, oxygen vacancy, LTP, LTD, STDP.

I. INTRODUCTION

Energy efficiency and parallel information processing make the human brain a model computing system for unstructured data handling [1], [2]. For the past few years, ferroelectric field-effect transistor (FeFET) has been proposed as an attractive non-volatile field-effect transistor (NVFET) candidate to emulate synaptic functions in bio-inspired neuromorphic systems [3], [4], owing to their non-destructive read-out operation, gradually changed conductance, low power consumption and the potential for high-density 3D integration. The recent discoveries of polycrystalline doped-HfO_2 FeFETs have provided promising candidates for synaptic applications in artificial neural networks (ANNs) [5]–[7]. To date, the synaptic functions including long-term potentiation (LTP), long-term depression (LTD), and spike-timing-dependent plasticity (STDP), have been implemented with FeFETs.

NVFETs integrated with amorphous gate dielectrics (e.g., Al_2O_3, ZrO_2) were reported and systematically characterized [8]–[12]. The ferroelectric-like behaviors in NVFETs were attributed to the voltage-driven dipoles consisting of oxygen vacancy and negative charge in the gate insulator. The amorphous dielectric NVFETs are more compatible with the gate-last processing of CMOS compared to the reported polycrystalline doped-HfO_2 devices and do not require the additional annealing crystallization process [9]. Using the lower dielectric constant amorphous film as the gate insulator can effectively reduce the operation voltage of the NVFETs [10]. In addition, the amorphous dielectric NVFETs exhibited significantly better linearity and larger dynamic range for multi-threshold voltage operation [10],

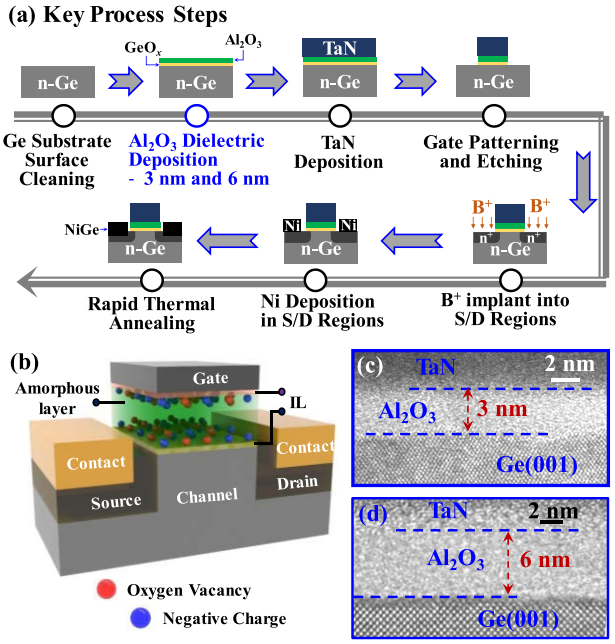

FIGURE 1. **(a) Key process steps for the fabrication of ferroelectric-like NVFET with amorphous Al_2O_3 gate insulator. (b) 3D schematic of the amorphous Al_2O_3 ferroelectric-like NVFET. HRTEM of TaN/Al_2O_3/Ge stack showing (c) 3 nm and (d) 6 nm-thick amorphous Al_2O_3 layer.**

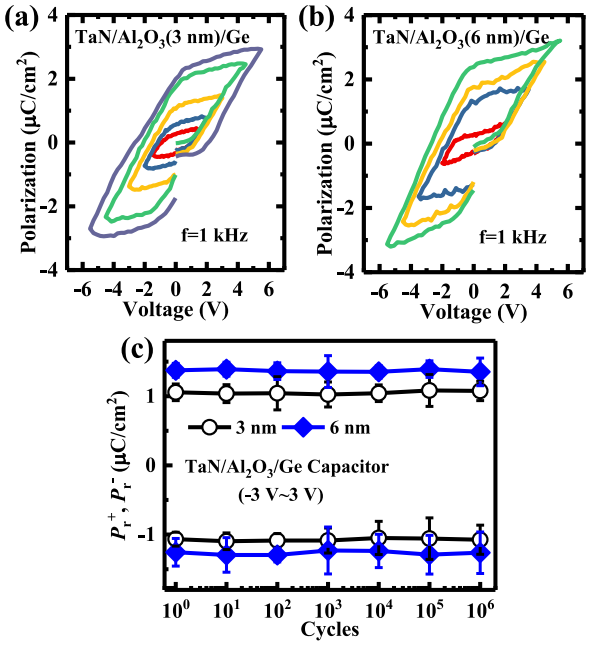

FIGURE 2. **Measured P–V curves of (a) TaN/Al_2O_3(3 nm)/Ge and (b) TaN/Al_2O_3(6 nm)/Ge capacitors at 1 kHz. (c) Endurance test showing no degradation of P_r after 10^6 sweeping cycles' sweeping.**

having a high potential for low-power neuromorphic devices to closely mimic biological behaviors. However, the systematic investigation of mimic biological synaptic behavior for amorphous dielectric NVFET and their application in spiking neural network computing has not been explored yet.

In this work, we report the synapse plasticity, including LTP, LTD, and STDP performance of the NVFET with an amorphous Al_2O_3 gate insulator to mimic the memory activity of the brain. In addition, the accuracy of the network above 80% is achieved based on the spiking neural network (SNN) architecture utilizing a Multi-ReSuMe algorithm [15], [16].

II. DEVICE FABRICATION

Ferroelectric-like NVFETs with amorphous Al_2O_3 gate insulators were fabricated on 4-inch n-Ge(001) substrates a bulk resistivity of 0.088-0.14 Ω·cm, which were purchased from AXT, Inc. [17]. The key process steps for fabricating amorphous NVFET are shown in Fig. 1(a). The Ge wafers were cleaned by acetone, methanol, and isopropanol successively to remove possible organic impurities on their surfaces, followed by hydrofluoric acid (HF) aqueous solution (HF:H_2O = 1:50) to remove the native oxide, and then Ge wafers were loaded into an atomic layer deposition (ALD) chamber. Al_2O_3 was deposited at 250°C, with TMA and H_2O vapor as the Al and O precursor, respectively. After that, a 100 nm-thick TaN gate electrode was deposited by reactive sputtering. 3 and 6 nm Al_2O_3 films were utilized for the comparative study of the devices with different Al_2O_3 thicknesses. After the gate electrode formation, the source/drain (S/D) regions were implanted by BF_2^+ at a dose of 1×10^{15} cm^{-2} and an energy of 20 keV. 20 nm nickel (Ni) S/D metal electrodes were formed by a lift-off process. Finally, the rapid thermal annealing (RTA) at 350°C was carried out to improve the interface quality and form the nickel germanide (NiGe) S/D contacts.

Fig. 1(b) shows the 3D schematic of the fabricated ferroelectric-like NVFET with an amorphous Al_2O_3 gate dielectric. The high-resolution transmission electron microscope (HRTEM) images in Figs. 1(c) and (d) show the gate stack on the Ge channel with 3 and 6 nm amorphous Al_2O_3 layers, respectively. Note that an interfacial layer (IL) of GeO_x exists between the Al_2O_3 and Ge channel, though which is too thin to be observed in the HRTEM images.

III. RESULTS AND DISCUSSION

The switchable polarization (P) *vs.* voltage (V) curves for the TaN/Al_2O_3/Ge stacks with 3 nm and 6 nm-thick Al_2O_3 are shown in Figs. 2(a) and (b), respectively, which were measured based on an axiACCT TF Analyzer 2000 system at a frequency of 1 kHz and room temperature. The P-V loops were obtained with the different ranges of sweeping V. It is clear to see that the P of amorphous Al_2O_3 capacitor increases slightly with the increase of the Al_2O_3 thickness, which may be due to the increase in the number of oxygen vacancies.

Fig. 2(c) exhibits the extracted evolution of the remnant polarization (P_r) for the device during the endurance test. P_r is the polarization value of being polarized ferroelectric material without the effect of an external electric field. The error bars were calculated to show the mean standard deviation of the results obtained from five devices for each Al_2O_3 thickness. No P_r degradation is observed after 10^6 cycles' sweeping. Compared to the polycrystalline doped-HfO_2 FE film, the

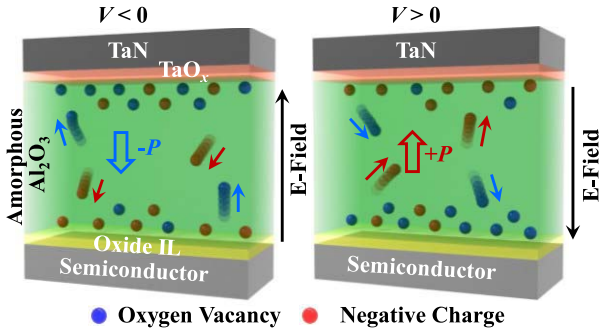

FIGURE 3. Schematics of the dynamic process mechanism for the ferroelectric-like properties in TaN/Al_2O_3/Ge capacitors. Switchable *P* is due to the migration of V_O^+ and negative charges to form dipoles.

amorphous Al_2O_3 device can behave ferroelectric-like characteristics at a thinner insulator thickness [18], [19]. The dynamic process of ferroelectric-like behavior in the amorphous Al_2O_3 capacitor is attributed to the voltage-modulated V_O^+ and negative-charge dipoles, as shown in Fig. 3. The formation of TaO_x between TaN and Al_2O_3 can induce V_O^+ into Al_2O_3 [20], [21]. This is the so-called scavenging effect, – i.e., the out-diffusion of oxygen atoms from Al_2O_3 to TaO_x IL, which introduce oxygen vacancies in Al_2O_3 layer [21]. With the mobile ions at the condition of $V<0$ ($V>0$), the ferroelectric-like $-P$ ($+P$) was achieved.

A synapse is a basic unit of the human neural network [22]. The ability of electric conductivity (synaptic weight) modulation is defined as synaptic plasticity [23], [24]. For the operation of ferroelectric-like NVFET as an artificial synapse, the synaptic weight is modulated independently via the gate terminal [22]. To examine the biological functionalities of the ferroelectric-like synaptic FET with an amorphous gate insulator, pulse measurements were performed on the device.

Fig. 4(a) shows the shift of drain current (I_{DS}) versus gate voltage (V_{GS}) curves for the ferroelectric-like FET with a 3 nm-thick amorphous Al_2O_3 gate insulator under a series of pulses. The $I_{DS} - V_{GS}$ curves shift to lower $|V_{TH}|$ with a series of fixed-amplitude negative voltage pulses (−3 V, 100 ns), *i.e.,* LTP (left), and to higher $|V_{TH}|$ with a series of fixed-amplitude positive voltage pulses (+3 V, 100 ns), *i.e.,* LTD (right), respectively. Similarly, Fig. 4(b) depicts how the $I_{DS} - V_{GS}$ curves of the 6 nm-thick Al_2O_3 device shift with a series of fixed-amplitude pulses. The synaptic weight is defined as channel conductance. It should be noted that the weights of synapses are updated in a parallel manner for online learning, and hence the identical potentiation/depression (PD) pulses are utilized. In addition, both 3 and 6 nm-thick Al_2O_3 devices can exhibit a continuous and adjustable synaptic weight updating process.

To further investigate the long-term plasticity of the Al_2O_3 synaptic device, Fig. 5(a) shows how the synaptic weight of 3 nm Al_2O_3 ferroelectric-like device is updated with ±3 V, 100 ns PD pulses. Conductance values are extracted at $V_{DS} = -0.05$ V and read gate voltage ($V_{GS,r}$) of −0.3, −0.2,

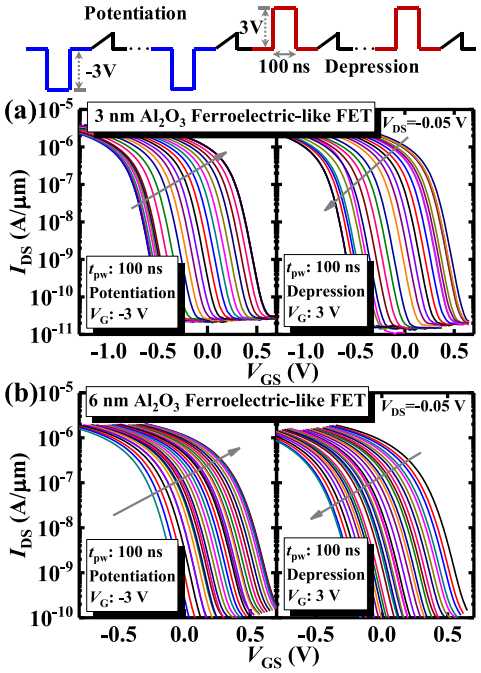

FIGURE 4. Analog synaptic behaviors of Al_2O_3 ferroelectric-like FET: gradual tuning of $I_{DS} - V_{GS}$ curves (a) 3 nm, (b) 6 nm under ±3 V, 100 ns voltage pulses for (left) potentiation and (right) depression operations.

−0.1, and 0 V. Here, we defined the potentiation and depression non-linearity coefficient (α_p and α_d) according to the extracted synaptic weight to characterize the weight change of the Al_2O_3 ferroelectric-like device. The α_p and α_d parameters are extracted based on the method in Reference [25]. The asymmetry is defined as $|\alpha_p - \alpha_d|$. At a V_{read} of −0.2 V, an asymmetry $|\alpha_p - \alpha_d|$ for only 0.05 with 32 PD steps for the ferroelectric-like FET synapse at ±3 V, 100 ns pulses is achieved. When we further increased the thickness of Al_2O_3 to 6 nm (Fig. 5(b)), the synaptic weights at V_{read} of 0.3, 0.2, 0.1, and 0 V are collected. At a V_{read} of 0 V, an asymmetry $|\alpha_p - \alpha_d|$ for only 0.17 is achieved.

The ferroelectric-like NVFET can exhibit excellent linearity, which is an important factor affecting the accuracy of ANNs computing [3], [6]. The change of the synaptic weight is larger compared to the 6 nm Al_2O_3 transistor, which indicates that the capability for modulating polarization in the device is not proportional to the thickness of Al_2O_3. $I_{DS} - V_{GS}$ curves for the 3 nm device are more uniform. Moreover, the 3 nm device achieves an improved linearity performance (i.e., smaller $|\alpha_p - \alpha_d|$) in comparison with the 6 nm Al_2O_3 NVFET.

In addition to the LTD and LTP characteristics, the transmission behavior is also a key factor affecting the biological synapses [22]. Here, we apply a series of negative input V_{GS} pulses (Fig. 6(a)) and a V_{DS} of −0.5 V to mimic the excitatory synaptic transmissions in the Al_2O_3 based synaptic transistor. Two types of 1 μs V_{GS} waveform pulses are utilized: $0 \sim -3$ V and $-2.5 \sim -3$ V. The dynamic response of the 3 and 6 nm Al_2O_3 based synaptic transistors are shown

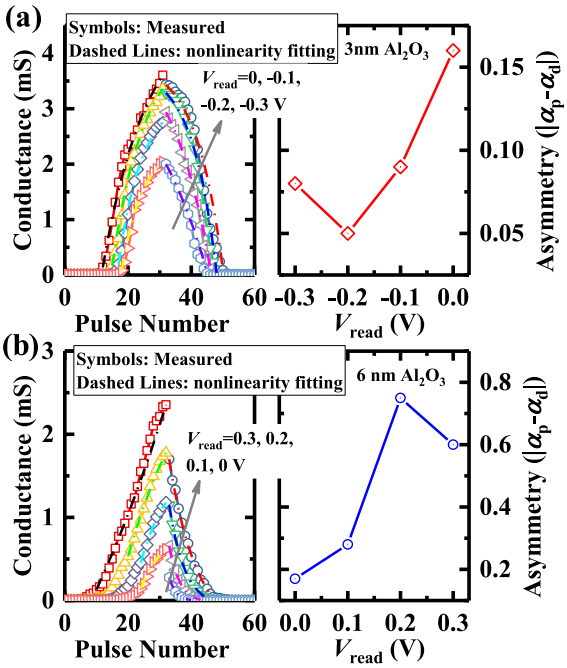

FIGURE 5. Synapse weight (conductance) tuning of the Al_2O_3 ferroelectric-like devices using fixed voltage pulses of ±3 V/100 ns for (a) 3 nm at the V_{read} of 0, −0.1, −0.2, and −0.3 V and (b) 6 nm at the V_{read} of 0, 0.1, 0.2, and 0.3 V. Here, the asymmetry ($|\alpha_p - \alpha_d|$) *vs.* V_{read} for the Al_2O_3 transistors were calculated according to [25].

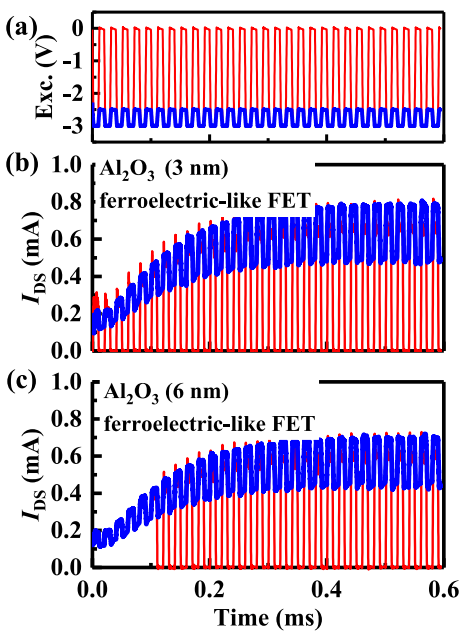

FIGURE 6. (a) The waveform of different excitatory input pulses. Measured the dynamic response of the amorphous Al_2O_3-based synapses (b) 3 nm and (c) 6 nm with different excitatory input pulses.

in Figs. 6(b) and (c), respectively. Note that the post synaptic I_{DS} of the device increases with the V_{GS} pulses number, and the synaptic plasticity of the amorphous Al_2O_3 based synapse can be the transition from short-term memory (STM)

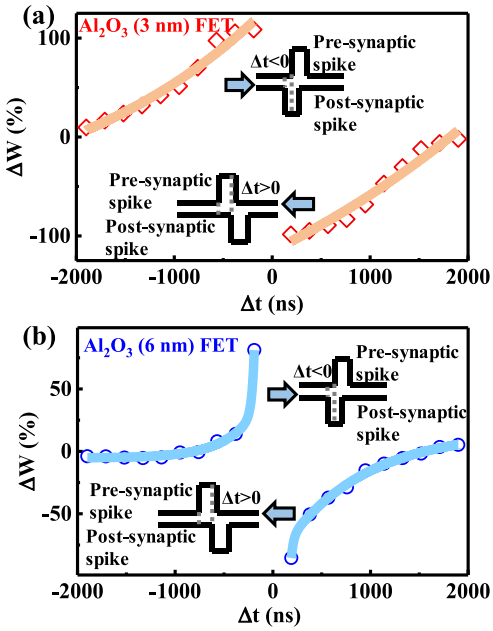

FIGURE 7. Measured STDP curves of (a) 3 nm and (b) 6 nm-thick amorphous Al_2O_3 synaptic transistors with a spike period of 190 ns.

to long-term memory (LTM) by adjusting the input waveform. The stable I_{DS} values of 3 and 6 nm Al_2O_3 devices are 8 and 7 μA/μm, respectively, under a series V_{GS} pulses (−2.5∼−3 V). The values of stable I_{DS} values decrease with the increase of Al_2O_3 thickness due to the larger equivalent oxide thickness.

The temporal relationship of the activity between the pre- and post-synaptic neurons is also important for the synapse [26], [27]. Here, t_{PRE} and t_{POST} are defined as the arrival times of the pre-spike and the post-spike, respectively. The change in synaptic weight Δw is a function of the $\Delta t(\Delta t = t_{PRE} - t_{POST})$ between pre- and post-synaptic activity. $\Delta w = (w_1 - w_0)/w_0 \times 100\%$, w_1 and w_0 are the final and initial conductance, respectively. Moreover, the change of synaptic weight is a function of the Δt between pre- and post-synaptic activity, which is defined as STDP. By utilizing the waveforms adopted in [28], [29], the STDP curves for the amorphous Al_2O_3-based synapse are measured with 100 ns spikes. As is shown in Fig. 7, the amorphous Al_2O_3-based synapse can stimulate the STDP learning rule successively for a given stimulation, the LTD will occur if $\Delta t > 0$, while LTP will occur if $\Delta t < 0$. High symmetry characteristics were obtained in both 3 nm and 6 nm-thick Al_2O_3 ferroelectric-like FETs. Compared to the 6 nm device, the synaptic weight of the 3 nm Al_2O_3 transistor varies more evenly with time.

SNN artificial algorithm was used here for its high biological reality, strong computing capability and lower power consumption. To explore the potential of amorphous Al_2O_3 ferroelectric-like NVFET for low-power neuromorphic computing, a three-layer fully connected SNN based on the leaky integrate and fire (LIF) model is used to recognize handwritten digits [19]. Fig. 8(a) shows the network structure.

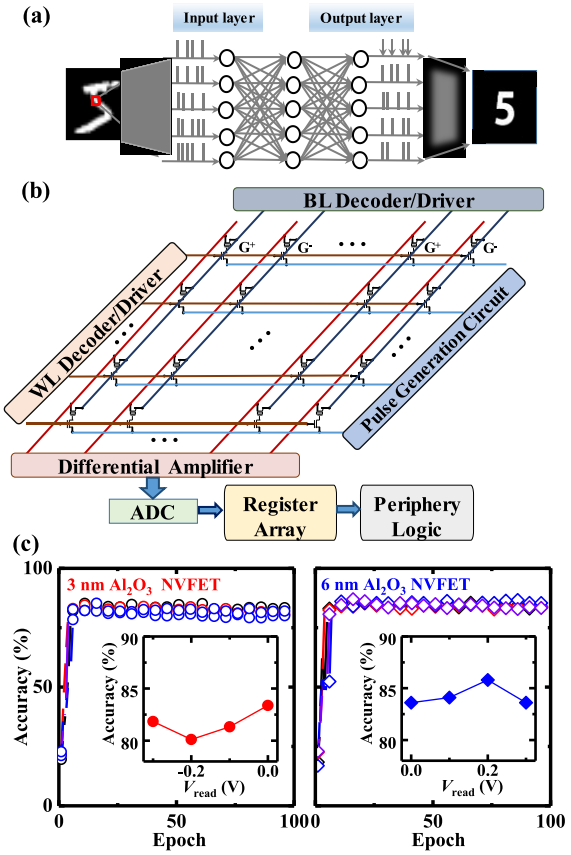

FIGURE 8. **(a) Architecture of the SNN includes a three-layer fully connected and based on the LIF model to recognize handwritten digits. (b) Circuit implementation simulation using SNN synapse arrays. (c) Accuracy above 80% can be achieved in SNN based on Al_2O_3 transistors under various V_{read}.**

Here, the input, hidden, and output layers include 784, 1000, and 10 neurons, respectively. The membrane time constant of neurons is 2 μs, and the resting potential is 0 V. The operation of the LIF neurons can be given as:

$$\tau \frac{dU}{dt} = RI - (U - E_{rest}),$$

where τ, U, R, E_{rest}, and I represent the membrane time constant, the membrane potential, the resistance of ion channel, the rest potential, and the input signal, respectively. The product of R and I can be realized by the Al_2O_3 ferroelectric-like FET array. If U exceeds the threshold voltage (V_{th}) of the neuron, the neuron spikes, and its voltage is reset to E_{rest}. The calculation of membrane voltage can be performed in the peripheral circuit.

A signed weight is mapped to the differential conductance of a pair of Al_2O_3 ferroelectric-like FETs. In this manner, all the weights from the same output neuron are mapped to two conductance columns: one column for positive weights with positive pulse inputs and the other for negative weights with equivalent negative pulse inputs. After inputting the encoded pulses into the bit lines, the output currents through the two differential source lines are sensed and accumulated. The differential current is the weighted sum corresponding to the input feature. The weights of different layers are mapped to different pairs of differential rows, and the entire Al_2O_3 ferroelectric-like FET array operates in parallel under the same inputs. All the desired weighted-sum results are obtained concurrently, as shown in Fig. 8(b).

TABLE 1. **Performance benchmarking of the ferroelectric-like NVFET in this work against the reported NVFETs synapse devices.**

Device	Dielectric	Max P_r,	Best speed	$\lvert\alpha_p$-$\alpha_d\rvert$	NN architecture	Acc. (%)
FE-FinFET[30]	HZO(8.5nm)/ SiO_2(1.5 nm)	~22μc/cm²	100μs	9.15	MLP	~80
FeFET[3]	HZO(10 nm)/ SiO_2(0.8 nm)	~16μc/cm²	75ns	13.62	MLP	~90
NV-FeFET[6]	HZO(10 nm)/ Al_2O_3(2 nm)	~11μc/cm²	50ns	2.92	MLP	~88
Al_2O_3 FET[10]	Al_2O_3(3.6nm)	3μc/cm²	100 ns	0.04	CNN	>94
This work	Al_2O_3(3 nm)	2μc/cm²	100 ns	0.05	SNN	>80
	Al_2O_3(6 nm)	2.4μc/cm²		0.17		>80

$P_{r,\,max}$: maximum P_r; Acc.: accuracy of online training; MLP: Multilayer perceptron; CNN: convolutional neural network

The SNN online training simulations parameterized by the Al_2O_3-based synapses are carried out, where the weight change is calculated based on the STDP property and the Multi-ReSuMe algorithm, and translated into the number of pulses [16]. Firstly, the conductance was normalized between zero and one for the simulation of online training. For initialization, the conductivity of each device is set to a random value of about 0.8. And then, the conductance change calculated by multi-ReSuMe algorithm is transformed into the number of pulses to achieve weight modulation. Fig. 8(c) shows the in-situ training accuracy of the device in this work. A decent learning accuracy (>80%) can be achieved in SNN based on our Al_2O_3-based synapses under different V_{read}.

We benchmark the ferroelectric-like NVFETs in this work with the reported FeFET synapse devices in Table 1. The lower non-linearity, asymmetry coefficients, and the higher SNN online training accuracy are achieved.

IV. CONCLUSION

In this work, the synaptic transistors are experimentally realized based on the ferroelectric-like FET integrated with amorphous Al_2O_3 insulator. By applying different V_{GS} pulse, we systematically demonstrated that the amorphous Al_2O_3 synaptic device can successfully mimic the synaptic plasticity in organisms, including LTP, LTD, the transition from STM to LTM, and STDP behaviors. In addition, the accuracy of the online learning of the amorphous Al_2O_3 synaptic device based on the SNN architecture utilizing a Multi-ReSuMe algorithm was realized. An accuracy above 80% was achieved. All these results indicate that the amorphous Al_2O_3 synaptic device has high application potential in neuromorphic computing.

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