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Modeling and Design of FTJs as Multi-Level Low Energy Memristors for Neuromorphic Computing

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ABSTRACT An in-house modeling framework for Ferroelectric Tunnelling Junctions (FTJ) is here presented in details. After a precise calibration against experiments, the model is exploited for an insightful study of the design of FTJs as synaptic devices for neuromorphic networks. Our analysis explains and addresses the tradeoff between the reading efficiency and the effects of the depolarization field during the retention phase. The reported results show that a moderately low- κ tunnelling dielectric (e.g., SiO₂) can increase the read current and the current dynamic range. The study shows also how the contribution of trapped charge may favor the stabilization of the polarization inside the FTJ, but also reduces the maximum read current.

INDEX TERMS Ferroelectric tunnelling junctions, depolarization field, charge trapping, tunneling electron resistance, neuromorphic computing.

I. INTRODUCTION

The huge interest in the field of neuromorphic computing pushed a lot the research for synaptic devices capable of non volatile, multi-level adjustments of the resistance [1]. Indeed, for the neural network hardware, low programming energy and high reading-impedance are crucial [2] and the proper design of novel synaptic devices can improve by orders of magnitude the energy efficiency of the system [3].

In this respect, Ferroelectric Tunneling Junction (FTJ) is a promising candidate as synaptic device with high energy efficiency. A four level operation has been already experimentally reported in a Metal-Ferroelectric-Insulator-Metal (MFIM) architecture (Fig. 1(a)) [4]. However, the design of a MFIM FTJ has a delicate trade-off between the read operation and the retention condition. Indeed, during reading in the low resistance state, the voltage drop V_D across the dielectric layer should be large enough to induce a tunneling limited by the thin oxide, namely $qV_D > [\Phi_{MD} - \chi_F]$ (see Fig. 2(a)).

This requires a small dielectric capacitance $C_D = \epsilon_D/t_D$. The retention condition requires, instead, a large C_D/C_F ratio (with $C_F = \epsilon_F/t_F$ being the capacitance due to background polarization of the ferroelectric), so as to minimize the depolarization field E_{DEP} and prevent the backswitching of the ferroelectric layer [2] (see Fig. 2(b)). Furthermore the dielectric thickness t_D and its electron affinity χ_D have a large impact on the read tunnelling current.

Due to this complex trade-off and the many material and device options, there is an urgent need for a simulation driven optimization of the FTJs. However the modeling of FTJs is challenging, as it entails the ferroelectric dynamics for a three dimensional (3D) electrostatics and the tunnelling through the dielectric stack. Furthermore, since the non idealities of the different materials in the stack and/or at the interfaces can play an important role in the operation and in the performance of the FTJs [5]–[8], modeling strategies to include these effects are needed.

In this work, we extended the modeling framework for FTJs reported in [9], that accounts for the 3D treatment of the ferroelectric dynamics and electrostatics. The tunnelling through the MFIM stack is also modeled, including possible charge trapping mechanisms. After reporting a validation and calibration of the model against experiments [4], [10], we used the simulator to investigate some of the design trade-off implied by the operation of FTJs, also accounting for the possible contribution of the charge trapping to the overall performance of the devices.

II. MODELING APPROACH

We here concisely describe the in house developed modeling framework employed in this work, consisting of the ferroelectric dynamics, the tunnelling currents, and the charge injection and trapping models.

A. FERROELECTRIC DYNAMICS AND DEVICE ELECTROSTATICS

The starting point is the multi-domain Landau, Ginzburg, Devonshire (LGD) model for a MFIM capacitor presented in [11]–[13]. The dynamic equations for the domains polarization, P_i , ($i = 1, 2 \dots n_D$, with n_D being the number of domains) read:

$$\begin{aligned} t_F \rho \frac{dP_i}{dt} = & - \left(2\alpha_i P_i + 4\beta_i P_i^3 + 6\gamma_i P_i^5 \right) t_F \\ & + - \frac{t_F k}{dw} \sum_n (P_i - P_n) \\ & + - \frac{1}{2} \sum_{j=1}^{n_D} \left(\frac{1}{C_{i,j}} + \frac{1}{C_{j,i}} \right) P_j + \frac{C_D}{C_0} V_T \end{aligned} \quad (1)$$

where α_i , β_i , γ_i are the domain dependent ferroelectric anisotropy constants, $C_0 = (C_D + C_F)$, d is the side of the square domain, k and w are the coupling constant and the inter-domain region width for the domain wall energy (Fig. 1(b)), while the capacitances $C_{i,j}$ provide a three dimensional description of the depolarization energy and obey the sum rules $\sum_{j=1}^{n_D} (1/C_{i,j}) \simeq \sum_{i=1}^{n_D} (1/C_{i,j}) \simeq 1/C_0$ [11]. Equation (1) provides at each time t and bias $V_T(t)$ all the domain polarizations $P_i(t)$, so that the dielectric, $V_{D,i}$, and ferroelectric, $V_{F,i}$, voltage drops are given by [11]:

$$\begin{aligned} V_{D,i} &= \frac{1}{d^2} \int_{D_i} V_D(\vec{r}) d\vec{r} = \sum_{j=1}^{n_D} \frac{1}{C_{i,j}} P_j + \frac{C_F}{C_0} V_T, \\ V_{F,i} &= V_T - V_{D,i} = - \sum_{j=1}^{n_D} \frac{1}{C_{i,j}} P_j + \frac{C_D}{C_0} V_T \end{aligned} \quad (2)$$

As it can be seen, the resistivity ρ sets a time scale $t_\rho = \rho / (2|\langle \alpha \rangle|)$ of the ferroelectric dynamics, where $\langle \alpha \rangle$ is the average α across the domains. In this respect, a slow $V_T(t)$ bias compared to t_ρ results in a quasi static behavior.

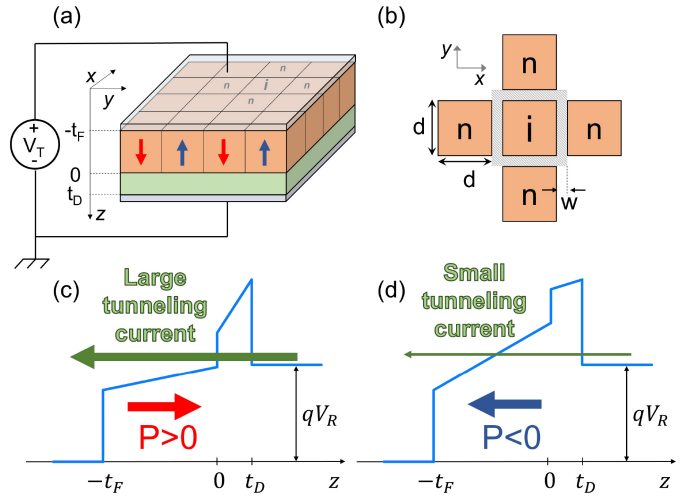


FIGURE 1. (a) Sketch of a MFIM based FTJ, where *MF*, *MD* are the electrodes contacting respectively the ferroelectric and the dielectric, while t_F , t_D , ε_F and ε_D are the ferroelectric and dielectric thickness and permittivity, respectively. A positive ferroelectric polarization points towards the dielectric (red arrow). (b) Zoom on ferroelectric domains where d is the side of the square domain and w is the width of the domain-wall region used for the domain wall energy in LGD (Eq. (1)) [11]. Throughout the work we used $d = 5 \text{ nm}$, $w/d = 0.1$ and the domain wall coupling factor in Eq. (1) was set to $k/w = 2 \times 10^{-3} \text{ [m}^2/\text{F]}$. V_T is the external bias. (c), (d) Qualitative band diagram across the dielectric stack through the read operation, where V_R denotes the read voltage. (c) Positive polarization and low resistance state; (d) Negative polarization and high resistance state.

B. READ OPERATION AND TUNNELLING CURRENT

We assume in the model that the current in the read operation, I_R , is dominated by the tunnelling through the dielectric stack, which is estimated as the sum of the $I_{R,i}$ in each domain. The $I_{R,i}$ is in turn expressed by using a Landauer model as [14]:

$$I_{R,i} = \frac{q}{\pi \hbar} \int_{-\infty}^{\infty} \sum_{k_x, k_y} T_i(E_\perp) \Delta f_w(E_\perp) dE_\perp \quad (3)$$

where $\Delta f_w(E_\perp) = [f_{0,MD}(E_\perp + \varepsilon(k)) - f_{0,MF}(E_\perp + \varepsilon(k))]$ identifies the Fermi window, and the transverse energy is $\varepsilon(k) = (\hbar^2/2m_\parallel)(k_x^2 + k_y^2)$. The Fermi functions in Eq. (3) are defined as $f_{0,MD(F)}(E) = [1 + \exp(E - E_{f,MD(F)})]^{-1}$, with $E_{f,MD}$, $E_{f,MF}$ being the Fermi levels of the electrodes. Equation (3) assumes an effective mass approximation and an energy separability $E = E_\perp + \varepsilon(k)$, with the transverse energy $\varepsilon(k)$ being conserved in the tunnelling process [15]. For a tunnelling transmission, $T_i(E_\perp)$, independent of (k_x, k_y) , the sum over (k_x, k_y) can be evaluated analytically for each electrode $M = MD$ or MF as [16]

$$\begin{aligned} \sum_{k_x, k_y} f_{0,M}(E_\perp + \varepsilon(k)) &= \frac{A}{(2\pi)^2} \int_k f_{0,M}(E_\perp + \varepsilon(k)) dk \\ &= \frac{AK_B T m_\parallel}{2\pi \hbar^2} \ln[1 + \exp(\eta_{f,M})] \end{aligned} \quad (4)$$

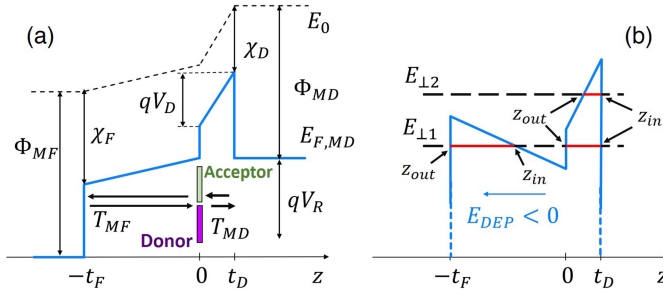


FIGURE 2. Energy band diagram across the MFIM stack. E_0 , Φ_{MF} and Φ_{MD} are respectively the vacuum level, and the work function of the MF and MD electrodes. χ_F , χ_D are the electron affinity of the ferroelectric and dielectric, $E_{f,MD}$, $E_{f,MF}$ are the Fermi levels in MD and MF. (a) Read condition with a voltage $V_T = V_R = qV_D$ should be larger than the ferroelectric tunnelling barrier [$\Phi_{MD} - \chi_F$], so that the ferroelectric conduction band profile can drop below $E_{f,MD}$; (b) Retention condition for $V_T = 0$ V: the depolarization field $E_{DEP} \approx P_r[\epsilon_F(C_D/C_F + 1)]^{-1}$ should be minimized to prevent backswitching (P_r is the remnant polarization).

where $\eta_{f,M}$ is defined as $\eta_{f,M} = (E_{f,M} - E_{\perp})/K_B T$. Hence the expression for $I_{R,i}$ simplifies as

$$I_{R,i} = \frac{AK_B T m_{\parallel} q}{2\pi^2 \hbar^3} \int_{-\infty}^{+\infty} T_i(E_{\perp}) \Delta f_L(E_{\perp}) dE_{\perp} \quad (5)$$

where $\Delta f_L(E_{\perp}) = \ln[1 + \exp(\eta_{f,MD})] - \ln[1 + \exp(\eta_{f,MF})]$. For a read voltage V_R applied to the MF electrode, we have $E_{f,MF} = E_{f,MD} - qV_R$. Finally, $T_i(E_{\perp})$ is calculated accordingly with a WKB approximation and an effective oxide mass m_{ox} . Here we notice that the m_{\parallel} in Eq. (5) corresponds to an effective mass for the density of states of the metal electrodes. In the lack of a better determination of m_{\parallel} , we used the popular assumption $m_{\parallel} \approx m_0$ [17].

For the purpose of WKB calculations the conduction band profile $E_{CD,i}(z)$, $E_{CF,i}(z)$ in the oxide and ferroelectric is assumed to be linear and set by the $V_{D,i}$ and $V_{F,i}$ given by Eq. (2); this simplifies the determination of the extrema z_{in} , z_{out} of the tunnelling paths illustrated in Fig. 2(b). Depending on the specific polarization condition, two tunnelling paths may be involved in the WKB calculation at a given E_{\perp} (see Fig. 2(b)), in which case $T_i(E_{\perp})$ is obtained as the product of the two tunnelling transmission probabilities. This approach neglects the influence on $T_i(E_{\perp})$ of interference effects, which is a reasonable approximation also in virtue of the empirical calibration of some modeling parameters discussed below.

C. CHARGE INJECTION AND TRAPPING MODEL

It has been recently pointed out that in ferroelectric–dielectric systems the charge injection through the thin dielectric and the charge trapping can play an important role [5]–[8]. Hereafter we will assume that tunnelling is the dominant conduction mechanism across the Al_2O_3 layer, even if additional mechanisms assisted by defects are also possible in thin oxides [18]. Moreover, we describe the trap density and trapped charge in terms of areal densities at the ferroelectric–dielectric interface. However, it is acknowledged that these

TABLE 1. Material parameters used in simulations. The work function Φ_M of Al and TiN were taken as 4.08 eV and 4.55 eV, respectively.

	HZO	Al_2O_3	SiO_2
χ_D, χ_F [eV]	2.1	1.4	0.95
$m_{ox(F,D)}$ [m_0]	0.4	0.3	0.5
ϵ_D, ϵ_F [ϵ_0]	30	10	3.9

TABLE 2. The acceptor and donor traps are located 0.4 eV and 2.4 eV below the conduction band minimum at the ferroelectric–dielectric interface, respectively, and they both extend for 2 eV wide range in the energy gap.

σ_E [meV]	σ_T [cm ²]	m_D [m_0]	m_F
7	$5 \cdot 10^{-14} - 1 \cdot 10^{-15}$	0.23 – 0.3	0.4

figures should be considered as equivalent areal densities possibly including also a charge trapping in the ferroelectric and dielectric films.

A first order dynamic equation for a trap level at the ferroelectric–dielectric interface having an energy E_T and an occupation f_T can be written as

$$\frac{\partial f_T}{\partial t} = c_{MD}(1 - f_T) - e_{MD}f_T + c_{MF}(1 - f_T) - e_{MF}f_T \quad (6)$$

where c_M and e_M ($M = MD$ or MF) denote capture and emission rate of each trap. When f_T is equal to the Fermi function at the electrode MD or MF, a detailed balance must be satisfied between the capture and emission rate towards the electrodes, which we enforced through the conditions

$$\begin{aligned} c_{MD}(1 - f_{0,MD}) - e_{MD}f_{0,MD} &= 0 \\ c_{MF}(1 - f_{0,MF}) - e_{MF}f_{0,MF} &= 0. \end{aligned} \quad (7)$$

Equations (7) can be readily used to substitute e_{MD} , e_{MF} in terms of c_{MD} , c_{MF} in Eq. (6). The capture rates at a given trap energy E_T are described in terms of the tunnelling transmission from the electrodes, and they are proportional to the Fermi functions at the electrodes. More precisely, we write $c_{MD} = c_{MD0} \times f_{0,MD}(E_T)$ and $c_{MF} = c_{MF0} \times f_{0,MF}(E_T)$, with c_{MD0} , c_{MF0} defined as:

$$c_{M0}(E_T) = \sigma_T \sigma_E \frac{m_{\parallel}}{2\pi^2 \hbar^3} \int_0^{+\infty} T_M(E_T - \varepsilon) d\varepsilon, \quad (8)$$

where σ_T [cm²], σ_E [eV] are respectively an area and an energy cross section of the traps. As discussed above, the tunnelling transmission $T_{MD}(E_T - \varepsilon)$ and $T_{MF}(E_T - \varepsilon)$ were calculated through the WKB approximation, by using the effective tunnelling masses m_D , m_F , and the energy barriers $\Phi_D = (\Phi_{TiN} - \chi_D)$, $\Phi_F = (\Phi_{TiN} - \chi_F)$ in Tabs. 1 and 2.

By using Eq. (7) and the capture rates c_{MD0} , c_{MF0} defined in Eq. (8), the dynamic equation in Eq. (6) can be rearranged in the equivalent form

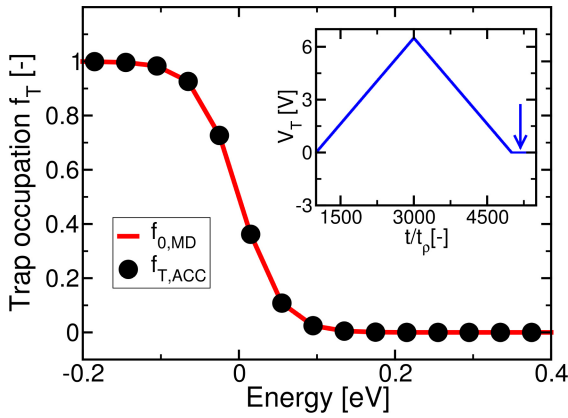


FIGURE 3. Steady state equilibrium occupation (i.e., at $V_T = 0$ V) for acceptor-type traps after a SET pulse. The trap energy on the x -axis is referred to the Fermi level $E_{f,MD}$ of the MD electrode. The red line is a plot of the Fermi occupation function $f_{0,MD}(E)$ of the MD electrode. The inset shows the V_T waveform used for the simulations and the vertical arrow indicates the time at which the trap occupation f_T has been plotted.

$$\frac{\partial f_T}{\partial t} = c_{MD0}[f_{0,MD} - f_T] + c_{MF0}[f_{0,MF} - f_T]. \quad (9)$$

In steady state conditions, Eq. (9) results in a trap occupation

$$f_T = \frac{c_{MD0}f_{0,MD}(E_T) + c_{MF0}f_{0,MF}(E_T)}{c_{MD0} + c_{MF0}}. \quad (10)$$

Equation (10) shows that at the equilibrium, namely in steady state for $V_T = 0$ V and thus for $E_{f,MD} = E_{f,MF}$, the f_T of acceptor type traps is duly set by the equilibrium Fermi function. When a non zero V_T is applied to the structure, instead, the steady state f_T approaches the equilibrium condition with one of the two electrodes only if the capture rate from that one electrode is much larger than the capture rate from the second electrode.

Figure 3 shows an example of the steady state occupation of acceptor type traps with an energy located 0.4 eV below the HZO conduction band edge and after a SET pulse (see the V_T waveform in the inset). In the example at study, the capture rate c_{MD0} is much larger than c_{MF0} , because of the very different thickness of the dielectric and ferroelectric layers, so that the steady state occupation of the trap is essentially in equilibrium with the Fermi level $E_{f,MD}$ of the MD electrode.

D. MODEL VALIDATION AND ANALYSIS OF EXPERIMENTAL DATA

The models have been validated by comparison with recent experimental data for both the ferroelectric Q - V_F curve (with $Q = P + \epsilon_0 \epsilon_F E_F$) [10], and the read current in corresponding FTJs [4]. Figure 4 shows the Q - V_F curve measured in the metal-ferroelectric-metal system of [10], featuring a 12nm thick $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$ (HZO); the simulations with the LGD multi-domain model of Eq. (1) are also reported. The agreement between simulations and experiments is good and the matching in the switching region improves by accounting for the domain-to-domain variations of α_i , β_i and γ_i .

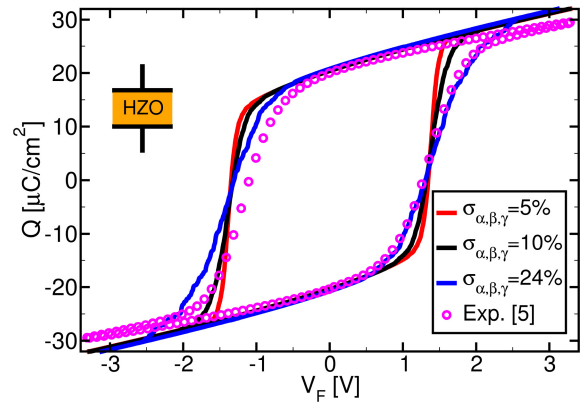


FIGURE 4. Experiments from [10] (symbols) and simulated polarization (lines) versus ferroelectric voltage characteristic of a $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$ layer with $t_F = 12$ nm. The nominal values of the anisotropy constants in the LGD equations are $\alpha = -5.8 \cdot 10^8$ m/F, $\beta = 2.9 \cdot 10^9$ m⁵/F/C², $\gamma = 6.5 \cdot 10^{10}$ m⁹/F/C⁴, and domain to domain variations are introduced according to a normal distribution of α_i , β_i , γ_i , where $\sigma_{\alpha,\beta,\gamma}$ denote the standard deviations normalized to the mean values. Both experiments and simulations correspond to a quasi static condition.

Throughout this work we will use the nominal values for α , β and γ reported in the caption of Fig. 4.

We simulated a MFIM structure featuring a 12 nm HZO ferroelectric, a 2 nm Al_2O_3 dielectric and TiN metal electrodes [4] (see Table 1 for material parameters). Figure 5 (top) shows examples of the setting and reading waveforms applied during the simulations of the FTJs, that were shaped to emulate the triangular waveforms used in the experiments of [4]. As it can be seen from the x -axis, the V_T waveforms are very slow compared to t_p , hence the simulations correspond to a quasi static operation.

In Fig. 5 (bottom), different maximum SET voltage values V_{SET} have been used, clearly resulting in different fractions, f_{UP} , of domains with a positive polarization, stemming from the minor loops in the Q versus V_T curve shown in the inset. By inspecting the f_{UP} in the set and read operation we also see that the MFIM device suffers from a quite strong depolarization effect. In fact, for a given V_{SET} , the f_{UP} during retention (i.e., for $V_T = 0$ V) and read (i.e., for $V_T = 2$ V) is significantly smaller than the corresponding f_{UP} reached in the SET operation. This occurs because the fairly large dielectric thickness $t_D = 2$ nm results in a strong depolarization field (see the sketch in Fig. 2(b)), producing a backswitching to $P_i < 0$ of some of the domains that had switched to $P_i > 0$ during the setting phase.

Figure 6 finally compares simulations and experiments for the I_R of FTJs at a read voltage $V_R = 2$ V. Our simulations in Fig. 6 can track the experiments quite well with the reasonable values of the oxide mass m_{ox} reported in Table 1 [19].

III. SIMULATION BASED DESIGN OF FTJS

The minimum I_R value required by applications is set by the transistors leakage current and by the noise of the sense

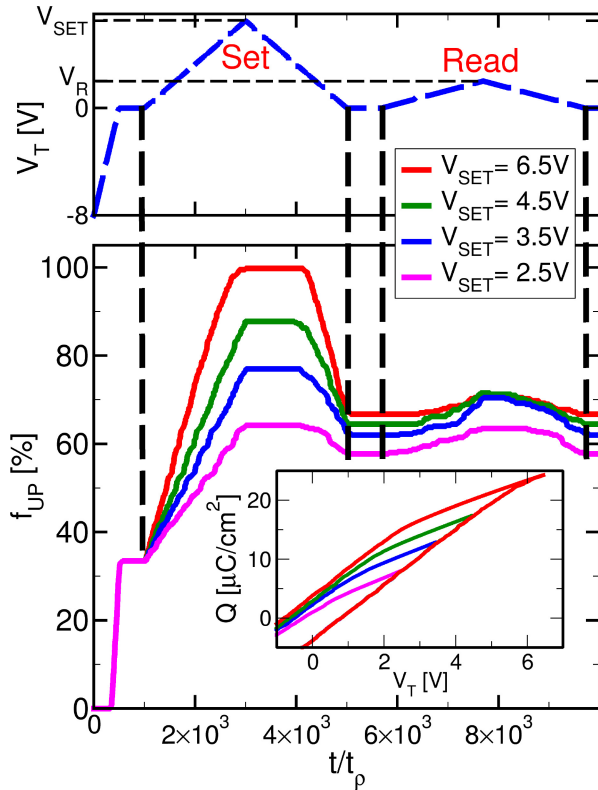


FIGURE 5. (Top) Examples of setting and reading waveforms used in the simulations of the MFIM based FTJs of [4] (see parameters in Table 1); read voltage is $V_R = 2$ V. (Bottom) Corresponding fractions f_{UP} , defined as the percentage of the domains having a positive polarization during the set and read operation and for different V_{SET} . The inset shows minor loops in the Q versus V_T plots corresponding to different V_{SET} values.

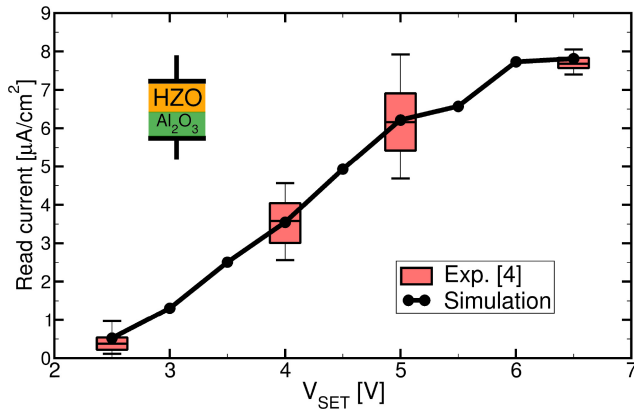


FIGURE 6. Experiments from [4] (boxes, device area $\approx 3.14 \cdot 10^{-4}$ cm²), and simulations (black solid line) for the read current at $V_R = 2$ V of an HZO/Al₂O₃ FTJ (12 nm / 2 nm) and versus the set voltage V_{SET} . The error bars for experiments were inferred from the cycle to cycle variations reported in Fig. 3(d) of [4].

amplifier and, for recent designs of neuromorphic processors, a reasonable target is approximately 100 pA [20], [21]. The results in Fig. 6 show that, for $V_{SET} = 2.5$ V, a device area larger than 10^4 μm^2 is needed to reach the $I_R = 100$ pA limit. Moreover the ON/OFF current ratio $R_I = [I_{R,max}/I_{R,min}]$ is only about ten, that seems too small

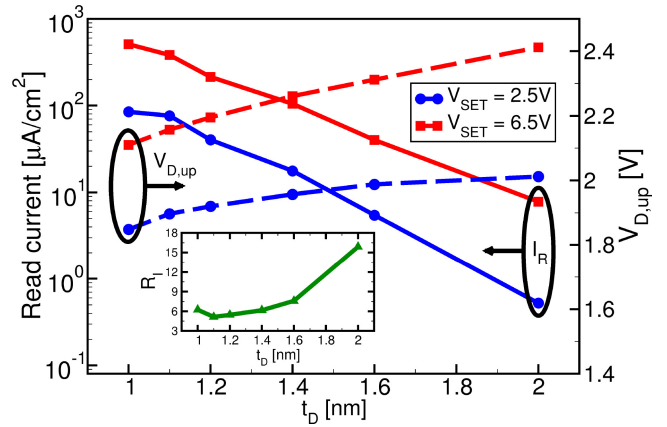


FIGURE 7. Read current at $V_R = 2$ V (left y axis) versus the Al₂O₃ thickness for an HZO/Al₂O₃ FTJ ($t_F = 12$ nm) and for $V_{SET} = 2.5$ V or 6.5 V. The average voltage drop, $V_{D,up}$, for the positive polarization domains is also reported (right y axis) in read condition, and the current ratio $R_I = [I_{R,max}/I_{R,min}]$ is shown in the inset.

for the desired 4-bit resolution of the synaptic weights [22]. Hence the primary goals of our FTJ design exploration are the increase of I_R and R_I .

A. DESIGN FOR NEGLIGIBLE CHARGE TRAPPING

The most obvious route to increase I_R is the scaling of the dielectric thickness t_D , whose effects are illustrated in Fig. 7 for the HZO/Al₂O₃ stack. As it can be seen, by thinning the Al₂O₃ layer the I_R increases, but R_I degrades (see inset). A marked R_I reduction with decreasing t_D has been observed also in experiments [10]. Fig. 7 also shows that, by thinning Al₂O₃ and thus increasing C_D , the average $V_{D,up}$ for the positive polarization domains decreases (right y axis), and eventually $qV_{D,up}$ cannot overcome $[\Phi_{MD} - \chi_F] \simeq 2.45$ eV (see Fig. 2(a)).

In order to reduce C_D for a given t_D , we replaced the tunnelling oxide with SiO₂, having a dielectric constant about 2.5 times smaller than Al₂O₃. Figure 8(a) reports I_R and versus V_{SET} for two variants of a HZO/SiO₂ based FTJ, and compared to the HZO/Al₂O₃ baseline case of Fig. 6 (black line). By using a 1 nm SiO₂ layer and maintaining TiN electrodes the I_R at $V_R = 2.0$ V largely increases (red line), but R_I does not improve. In the second option of the HZO/SiO₂ based FTJ we considered a low workfunction Al electrode ($\Phi_M \simeq 4.08$ eV), so as to reduce the SiO₂ tunnelling barrier $[\Phi_{MD} - \chi_D]$. This leads to a large I_R increase at fixed V_R , that we exploited to decrease both V_R to 1.5 V and the minimum V_{SET} to 2 V. The corresponding results in Fig. 8(a) (green line) show a large improvement for both I_R and R_I compared to the HZO/Al₂O₃ case. Indeed, Fig. 8(b) reveals that the 1 nm SiO₂ design leads to $V_{D,up}$ values comparable to the 2 nm Al₂O₃ for $V_R = 2$ V; moreover for Al electrodes the $qV_{D,up}$ can overcome $[\Phi_{MD} - \chi_F]$ even for $V_R = 1.5$ V.

The engineering of the metal work-function for the capping electrodes is still quite actively investigated for the

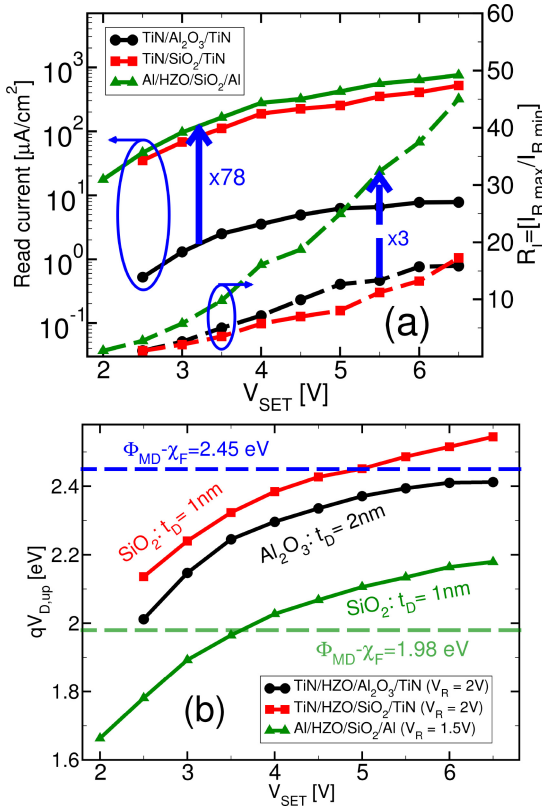


FIGURE 8. (a) Read current (left y axis) and $R_I = [I_{R,max}/I_{R,min}]$ (right y axis) versus the SET voltage for the TiN/HZO/ Al_2O_3 /TiN structure ($t_D = 2$ nm, $V_R = 2$ V) in Fig. 6, and for two variants of an HZO/ SiO_2 based FTJ, namely for TiN/HZO/ SiO_2 /TiN ($t_D = 1$ nm, $V_R = 2$ V), and for Al/HZO/ SiO_2 /Al ($t_D = 1$ nm, $V_R = 1.5$ V). The HZO thickness is $t_F = 12$ nm in all cases. (b) Average voltage drop, $V_{D,up}$, for the positive polarization domains (as in Fig. 7), for the different design options. The ferroelectric tunnelling barrier [$\Phi_{MD} - \chi_F$] is substantially reduced for the Al electrode.

design of FTJs [23], [24]. In this respect, while the crystallization annealing with a TiN electrode is the most popular option to induce ferroelectricity in the HZO, a robust HZO ferroelectricity has been experimentally reported also for different metal electrodes [23], [25].

B. DESIGN IN THE PRESENCE OF CHARGE TRAPPING

Because it has been argued that in ferroelectric–dielectric stacks the charge injection and trapping can compensate to a large extent the ferroelectric polarization [5], we have here analyzed the influence of such a charge trapping on the operation of FTJs. The model described in Section II-C allows us to have the trap occupation f_T for any waveform of the external bias V_T , which can be used to calculate the charges Q_{acc} , Q_{don} trapped in respectively acceptor and/or donor traps as:

$$Q_{acc} = \frac{(-q)}{n_D} \sum_{E_T} N_{acc} f_T(E_T) \Delta E, \quad (11a)$$

$$Q_{don} = \frac{q}{n_D} \sum_{E_T} N_{don} (1 - f_T(E_T)) \Delta E, \quad (11b)$$

where N_{acc} , N_{don} denote the trap densities and ΔE is the energy step between the discrete trap levels. The overall

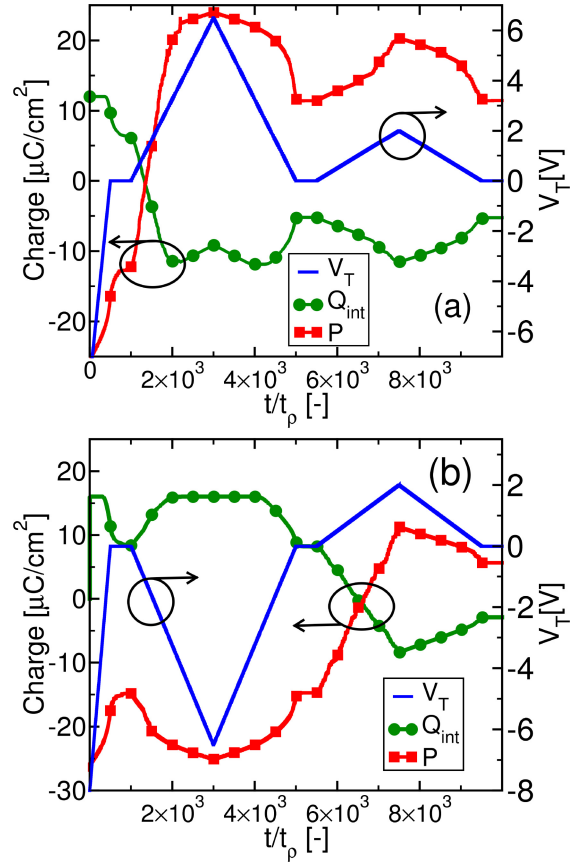


FIGURE 9. Simulated spontaneous polarization (P , red line) and interface charge (Q_{int} , blue line) averaged across the device area. (a) Results for a SET pulse followed by a 2 V read waveform; (b) results for a RESET pulse followed by the same read waveform. The interfacial trap densities used in these simulations are $N_{acc} = N_{don} = 5 \times 10^{13}$ [$\text{cm}^{-2} \text{eV}^{-1}$].

interface charge Q_{int} is simply the sum of Q_{acc} and Q_{don} . Equations (9) to (11) refer to a single domain in the FTJ structure, but it is understood that Eq. (9) was solved in each domain and self-consistently with the LGD equations for the ferroelectric dynamics. Moreover, in all simulations including traps, in each domain the charge Q_{int} was duly added to the polarization P in the calculation of all relevant quantities, such as $V_{D,i}$, $V_{F,i}$ in Eqs. (2).

Figure 9 shows an example of the waveforms for the average spontaneous polarization, P , and interface charge, Q_{int} , during a SET and a RESET pulses followed by a read pulse. As it can be seen, the acceptor and donor trap densities are such that approximately 50% of the ferroelectric polarization is compensated by Q_{int} during the SET/RESET phase, as well as during the read operation. Furthermore, the average P and Q_{int} tend to follow specular trajectories in Fig. 9. If we focus on the rising V_T ramp in Fig. 9(a), for example, this can be understood because, when Q_{int} produces a significant compensation of P , then the Q_{int} detrapping and the rising V_T ramp have an additive effect on the increase of the ferroelectric field that produces the P switching. This

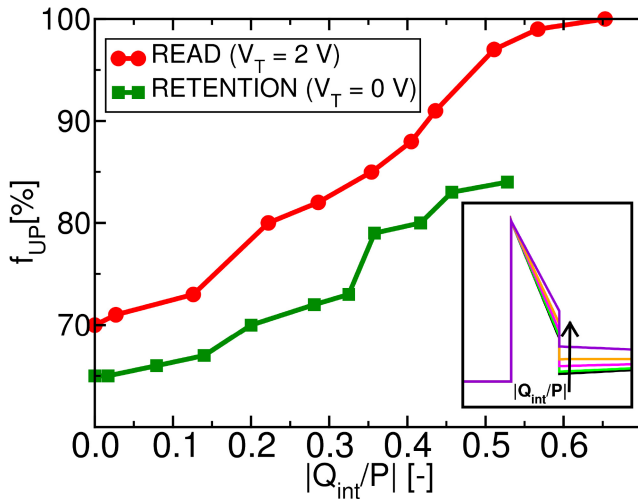


FIGURE 10. Percentage of domains with a positive polarization, f_{UP} , versus the charge compensation produced by interface traps and here quantified as $|Q_{int}/P|$. The f_{UP} is evaluated after a SET pulse during either retention or read phases. The inset illustrates the conduction band profile (averaged across the device area) close to the ferroelectric–dielectric interface and evaluated during the read pulse. The interfacial trap densities (with $N_{acc} = N_{don}$) varies between 0 and 5×10^{13} [$\text{cm}^{-2}\text{eV}^{-1}$].

creates the link between Q_{int} and P that results in roughly specular variations.

We now notice that the trapping induced compensation of the ferroelectric polarization observed in Fig. 9 is instrumental in order to stabilize the polarization by reducing the otherwise very large depolarization field in the ferroelectric. This latter point is best illustrated by Fig. 10, reporting the percentage f_{UP} of domains with a positive polarization after a SET pulse versus the charge compensation quantified as $|Q_{int}/P|$. The results are shown for either the retention (i.e., $V_T = 0$ V) or the read phase (i.e., $V_T = 2$ V). As expected, a larger polarization can be stabilized by increasing Q_{int} , however this does not result in an improved band bending in read mode. In fact, the inset shows that, by increasing $|Q_{int}/P|$, the average voltage drop, V_D , across the dielectric degrades and the HZO conduction band minimum at the ferroelectric–dielectric interface is pushed up. This is a serious drawback of the charge compensation via Q_{int} , which hinders the attainment of a band diagram favourable for the tunnelling injection through the thin dielectric layer.

It is presently difficult to be more quantitative about the trade-off between the favourable and the detrimental effects of the trapping-induced compensation of the ferroelectric polarization, particularly because it is difficult to estimate the trapped charge in actual devices. In this latter respect, the values of trap densities considered in Figs. 9, 10 are admittedly quite large, however they are not at all inconsistent with recent experimental papers that have reported estimates for the areal density of trapped charge in HZO based FTJs or FeFETs in the range of 10^{14} cm^{-2} [6], [26].

IV. CONCLUSION

An in-house developed simulator for FTJs has been presented and calibrated against experiments. The developed simulator has revealed fundamental to study the delicate tradeoffs between the reading current modulation and the depolarization field that hampers the retention of FTJs based synaptic devices. The results show that the use of a SiO_2 tunnelling dielectric and low workfunction metal electrodes can greatly increase the read current dynamic range, thus enabling the multi-bit synaptic weight resolution.

Concerning the detrimental effects of the depolarization field, we demonstrated that the contribution of charge trapping can be beneficial for the stabilization of the polarization during retention. However, the trapped charge may reduce the gain in the read current dynamics, thus limiting the benefits of an optimized design for ferroelectric tunnelling junctions.

REFERENCES

- [1] S. Yu, “Neuro-inspired computing with emerging nonvolatile memory,” *Proc. IEEE*, vol. 106, no. 2, pp. 260–285, Feb. 2018.
- [2] S. Slesazec and T. Mikolajick, “Nanoscale resistive switching memory devices: A review,” *Nanotechnology*, vol. 30, no. 35, Jun. 2019, Art. no. 352003. [Online]. Available: <https://doi.org/10.1088/1361-6528/ab2084>
- [3] S. Ambrogio *et al.*, “Equivalent-accuracy accelerated neural-network training using analogue memory,” *Nature*, vol. 558, no. 7708, pp. 60–67, 2018.
- [4] B. Max, M. Hoffmann, S. Slesazec, and T. Mikolajick, “Direct correlation of ferroelectric properties and memory characteristics in ferroelectric tunnel junctions,” *IEEE J. Electron Devices Soc.*, vol. 7, pp. 1175–1181, 2019.
- [5] H. W. Park *et al.*, “Polarizing and depolarizing charge injection through a thin dielectric layer in a ferroelectric-dielectric bilayer,” *Nanoscale*, vol. 13, no. 4, pp. 2556–2572, 2021.
- [6] K. Toprasertpong, M. Takenaka, and S. Takagi, “Direct observation of interface charge behaviors in FeFET by quasi-static split C-V and hall techniques: Revealing FeFET operation,” in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2019, pp. 23.7.1–23.7.4.
- [7] J. Li, Y. Qu, M. Si, X. Lyu, and P. D. Ye, “Multi-Probe characterization of ferroelectric/dielectric interface by C-V, P-V and conductance methods,” in *Proc. IEEE Symp. VLSI Technol.*, 2020, pp. 1–2.
- [8] S. Deng *et al.*, “Examination of the interplay between polarization switching and charge trapping in Ferroelectric FET,” in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, 2020, pp. 4.4.1–4.4.4.
- [9] R. Fontanini, M. Massarotto, R. Specogna, F. Driussi, M. Loghi, and D. Esseni, “Modelling and design of FTJs as high reading-impedance synaptic devices,” in *Proc. 5th IEEE Electron Devices Technol. Manuf. Conf. (EDTM)*, 2021, pp. 1–3.
- [10] B. Max, M. Hoffmann, S. Slesazec, and T. Mikolajick, “Ferroelectric tunnel junctions based on ferroelectric-dielectric $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2/\text{Al}_2\text{O}_3$ capacitor stacks,” in *Proc. 48th Eur. Solid-State Device Res. Conf. (ESSDERC)*, 2018, pp. 142–145.
- [11] T. Rollo, F. Blanchini, G. Giordano, R. Specogna, and D. Esseni, “Stabilization of negative capacitance in ferroelectric capacitors with and without a metal interlayer,” *Nanoscale*, vol. 12, no. 10, pp. 6121–6129, 2020.
- [12] T. Rollo, F. Blanchini, G. Giordano, R. Specogna, and D. Esseni, “Revised analysis of negative capacitance in ferroelectric-insulator capacitors: Analytical and numerical results, physical insight, comparison to experiments,” in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2019, pp. 7.2.1–7.2.4.
- [13] D. Esseni and R. Fontanini, “Macroscopic and microscopic picture of negative capacitance operation in ferroelectric capacitors,” *Nanoscale*, vol. 13, no. 21, pp. 9641–9650, 2021.

- [14] M. Lundstrom and C. Jeong, *Near-Equilibrium Transport*. Hackensack, NJ, USA: World Sci., 2013. [Online]. Available: <https://www.worldscientific.com/doi/abs/10.1142/7975>
- [15] M. V. Fischetti, S. E. Laux, and E. Crabbé, "Understanding hot-electron transport in silicon devices: Is there a shortcut?" *J. Appl. Phys.*, vol. 78, no. 2, pp. 1058–1087, 1995. [Online]. Available: <https://doi.org/10.1063/1.360340>
- [16] D. Esseni, P. Palestri, and L. Selmi, *Nanoscale MOS Transistors: Semi-Classical Transport and Applications*. Cambridge, U.K.: Cambridge Univ. Press, 2011.
- [17] F. Driussi, P. Palestri, and L. Selmi, "Modeling, simulation and design of the vertical graphene base transistor," *Microelectron. Eng.*, vol. 109, pp. 338–341, Sep. 2013. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/S0167931713003638>
- [18] H. Schroeder, "Poole-Frenkel-effect as dominating current mechanism in thin oxide films—An illusion?!" *J. Appl. Phys.*, vol. 117, no. 21, 2015, Art. no. 215103. [Online]. Available: <https://doi.org/10.1063/1.4921949>
- [19] F. Driussi, S. Spiga, A. Lamperti, G. Congedo, and A. Gambi, "Simulation study of the trapping properties of HfO₂-based charge-trap memory cells," *IEEE Trans. Electron Devices*, vol. 61, no. 6, pp. 2056–2063, Jun. 2014.
- [20] N. Qiao and G. Indiveri, "Scaling mixed-signal neuromorphic processors to 28 nm FD-SOI technologies," in *Proc. IEEE Biomed. Circuits Syst. Conf. (BioCAS)*, 2016, pp. 552–555.
- [21] M. Sharifshazileh, K. Burelo, T. Fedele, J. Sarnthein, and G. Indiveri, "A neuromorphic device for detecting high-frequency oscillations in human iEEG," in *Proc. 26th IEEE Int. Conf. Electron. Circuits Syst. (ICECS)*, 2019, pp. 69–72.
- [22] T. Pfeil *et al.*, "Is a 4-bit synaptic weight resolution enough? Constraints on enabling spike-timing dependent plasticity in neuromorphic hardware," *Front. Neurosci.*, vol. 6, p. 90, Jul. 2012. [Online]. Available: <https://www.frontiersin.org/article/10.3389/fnins.2012.00090>
- [23] R. Cao *et al.*, "Effects of capping electrode on ferroelectric properties of Hf_{0.5}Zr_{0.5}O₂ thin films," *IEEE Electron Device Lett.*, vol. 39, no. 8, pp. 1207–1210, Aug. 2018.
- [24] B. Max, T. Mikolajick, M. Hoffmann, S. Slesazeck, and T. Mikolajick, "Retention characteristics of Hf_{0.5}Zr_{0.5}O₂-based ferroelectric tunnel junctions," in *Proc. IEEE 11th Int. Memory Workshop (IMW)*, 2019, pp. 1–4.
- [25] Y.-C. Lin, F. McGuire, and A. D. Franklin, "Realizing ferroelectric Hf_{0.5}Zr_{0.5}O₂ with elemental capping layers," *J. Vac. Sci. Technol. B*, vol. 36, no. 1, 2018, Art. no. 011204. [Online]. Available: <https://doi.org/10.1116/1.5002558>
- [26] J. Li, M. Si, Y. Qu, X. Lyu, and P. D. Ye, "Quantitative characterization of ferroelectric/dielectric interface traps by pulse measurements," *IEEE Trans. Electron Devices*, vol. 68, no. 3, pp. 1214–1220, Mar. 2021.