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High-Temperature Characterizations of a Half-Bridge Wire-Bondless SiC MOSFET Module

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ABSTRACT SiC MOSFET allows higher temperature capability with higher switching efficiency than that of conventional Si devices, due to its superior electrical and thermal properties. Nevertheless, there are few reports on the systematic characterization of the SiC MOSFET power module operating at high-temperature. In this paper, a SiC MOSFET power module with planar interconnection was designed and fabricated to achieve low parasitic inductance and improved thermal performance. The static and dynamic performance of the SiC power module were characterized at 200°C. The thermal resistance of the double-sided cooling power module is 28.5% lower than that of the one with single-sided cooling.

INDEX TERMS Wire-bondless, SiC MOSFET, high-temperature.

I. INTRODUCTION

Compared with conventional Si devices, silicon carbide (SiC) semiconductor features high thermal conductivity, high switching speed, low switching loss, and excellent heat resistance, allows it to work for high-temperature and high-frequency applications [1]. However, traditional packaging technologies for Si-IGBT could not meet the harsh requirement of SiC power devices. For example, the emitter of the Si-IGBT chip is usually connected by bonding wires, which induces significant parasitic inductance and would thus limit the switching frequency [2]. Furthermore, only one-sided cooling can be provided in the traditional wire-bonding packaging, leading to high thermal resistance.

Recently, many efforts have been made by removing bond-wires, enabling double-sided cooling. Advanced packaging technologies, such as die-attach materials with high thermal and electrical conductivities, integrated radiator for improved heat dissipation, module design with low parasitic inductance and double-sided cooling capability for significant thermal resistance reduction [3], [4], [5]. The switching transients, thermal performance, and parasitic inductance have been characterized at room temperature. For example, up to 75% of the parasitic inductance and 40% of the thermal resistance can be reduced by integrating the radiator with the SiC power module [6]. It was clear that the parasitic inductance of a double-sided power module could be reduced as low as 1.63 nH by only removing bond-wires [7], [8], [9], and the maximum junction temperature could be decreased by a range from 15% to 35 % in the double-sided cooling way [10]. Moreover, in industry, ALSTOM used flip-chip technology to achieve double-side cooling and improve the heat dissipation capacity of its power modules [11]. The second-generation Camry hybrid vehicles used planar power modules under the double-sided cooling to improve the heat removal as well as reducing costs [12]. it is incomplete to only characterize the performance of the double-sided power modules at room temperature [13]. Lack of performance characterizations of the wire-bondless SiC MOSFET module at high temperatures could limit the applications, e.g., electrical vehicle.

This paper presented a demonstration of 900-V/196-A wire-bondless SiC MOSFET module with the double-sided

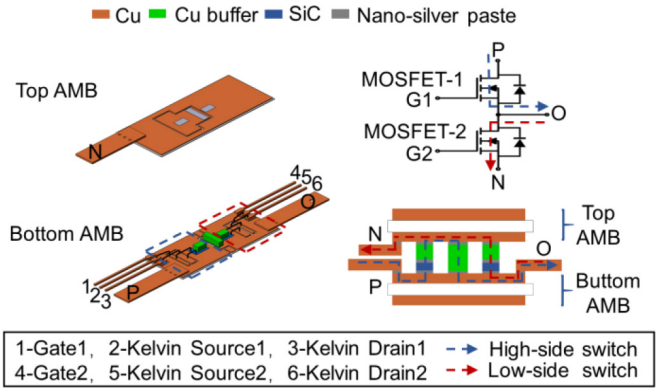

FIGURE 1. Schematics of a wire-bondless 900-V/196-A SiC MOSFET module.

cooling capability and extremely low parasitic inductance. The static and dynamic electrical properties at high-temperature were characterized. Great thermal performance under different cooling conditions was verified for the wire-bondless SiC module due to its double-sided cooling capability.

This paper was organized as follows: Section II described the packaging structure and material selection of the 900-V/196-A wire-bondless SiC MOSFET module. Section III and Section IV evaluated the electrical and the thermal performance of the SiC MOSFET power module at temperature up to 200°C, respectively.

II. MODULE DESIGN AND FABRICATION

A. PACKAGE STRUCTURE

Fig. 1 shows the iso-view of the wire-bondless half-bridge SiC MOSFET modules. Each arm contains one SiC MOSFET (CPM3-0900-0010A, CREE). The MOSFET body diode was used for freewheeling.

The SiC chips are sandwiched between two AMB substrates. Cu spacer was employed on the top side of the chips to reduce the thermomechanical stress. For the high-side switch, current flows from the terminal "P" of the bottom substrate to the terminal "O" of the bottom substrate. For the low-side switch, current flows from the terminal "O" of the bottom substrate to the terminal "N" of the top substrate. P and N are stacked together to shorten the length of the power loop as well as reducing the parasitic inductance.

B. MATERIALS

Packaging materials for each part of the wire-bondless SiC MOSFET are summarized in Table 1. The top-side metallization of AlSiCu is not suitable for soldering or sintering, so the top source electrodes of the SiC chips were metalized with Ti/Ni/Ag using the magnetron sputtering technology. The nano-silver paste was used as the die-attach material because of its high melting temperature, excellent thermal, electrical conductivities [14] and high reliability, especially at high temperatures [15]. Si_3N_4 active-metal-brazing substrates (AMB) with high thermal

TABLE 1. Materials for the wire-bondless SiC MOSFET module.

Material	Property
Substrates	Si_3N_4 substrate 0.32 mm Si_3N_4, 0.8 mm Cu
Cu buffer-attach layer	Nano-silver paste Thickness of 80 μm
Copper Buffer	Cu sheet coated with silver Cu thickness of 2.5 mm
Die (Source)-attach layer	Nano-silver paste Thickness of 80 μm
SiC MOSFET	900-V/196-A 7.26 mm×4.36 mm from Cree
Die (Drain)-attach layer	Nano-silver paste Thickness of 80 μm
Terminals	Copper coated with silver
Terminals layer	Thickness of 0.8 mm
Bonding wires	Al Diameter of 8 mils
Encapsulant	Epoxy resin

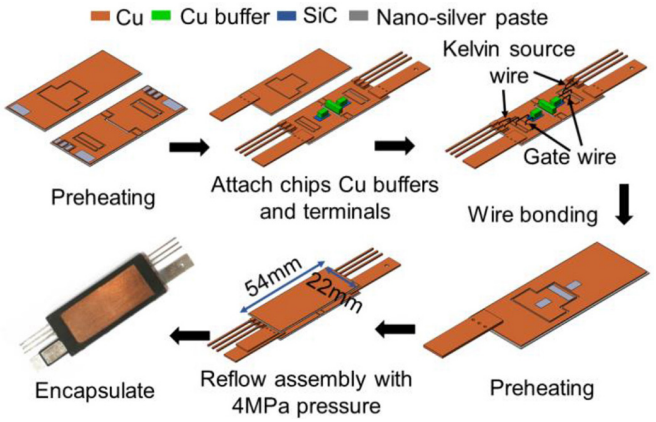

FIGURE 2. Fabrication process of a 900-V/196-A SiC MOSFET module.

conductivity were used due to their low thermal expansion coefficient (CTE) as well as excellent high-temperature stability. Epoxy resin (EME-G780 Type C from Sumitomo Bakelite) with high-temperature stability was used to as the encapsulant. Such encapsulation could be stable up to 200°C and provide sufficient mechanical support for the wire-bondless SiC module.

C. MODULE FABRICATION

Fig. 2 shows the fabrication process of the wire-bondless SiC MOSFET module. Both the AMB substrates and the terminals were cleaned by acetone/alcohol/DI water. Nano-silver paste was screen-printed at the terminal of AMB substrates, and followed by preheating for 10 min at 100°C to remove most of the solvents before sinter-bonding. Another 80-μm thick nano-silver paste was screen-printed onto the bottom AMB substrate. Both the SiC dies and Cu buffer spacers were placed on the as-printed paste separately using a pick and place system (T-300-F-C3, TRESKY). The AMB substrate with the as-mounted chips and the Cu buffer spacers were pressureless sinter-bonded in a vacuum reflowing furnace (RO716, ATV) under a formic acid atmosphere to prevent the oxidation of the AMB substrates.

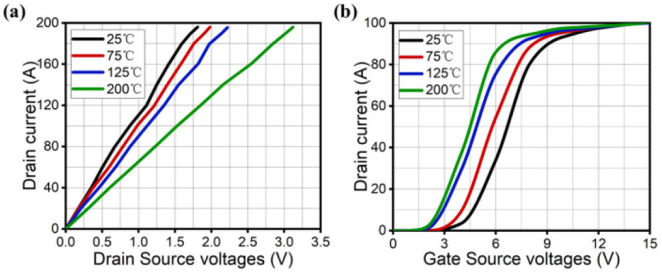

FIGURE 3. (a) *I-V* curves and (b) transfer characteristics at different temperatures.

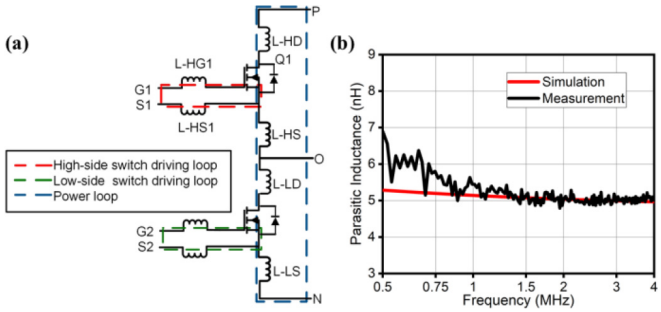

FIGURE 4. (a) Parasitic inductance network of the wire-bondless SiC MOSFET module; (b) Simulated and measured power loop inductance.

The gate and kelvin source the as-attached SiC MOSFETs were interconnected with the corresponding terminals by aluminum bonding-wires only to monitor the V_{gs} and V_{ds}.

80-μm-thick nano-silver paste was screen-printed onto the top AMB substrate and followed by heating for 10 min at 100°C.

The top AMB substrate and the as-sintered bottom one was sinter-bonded together by sintering the as-dried nano-silver paste under the help of 4 MPa pressure using the same heating profile.

Finally, the as-assembled wire-bondless half-bridge SiC module was encapsulated with the high-temperature epoxy resin using transfer molding technology. The dimensions of the demonstrated SiC module are 54 mm × 22 mm × 5 mm.

III. ELECTRICAL PERFORMANCE

A. STATIC ELECTRICAL PROPERTIES

The static electrical characteristic of the wire-bondless SiC MOSFET module were tested using a curve tracer (371A, TEKTRONIX) at different junction temperatures ranging from 25°C to 200°C, with drain current, I_d, up to 196 A. Fig. 3(a) shows the relationship between the measured I_d and the drain-source voltage V_{ds} of the low-side switch. At the gate voltage of 15 V, the $R_{ds(on)}$ increases monotonously with the junction temperatures. At 25°C, the drain-source saturation voltage, $V_{ds(sat)}$, of the low-side switch is 1.81 V when the I_d is 196 A, which is lower than the typical value, 1.9 V, from the device datasheet (CPM3-0900-0010A, CREE). It was likely that the superior conductive sintered nano-silver as die attachment and the elimination of the bonding wires reduced the packaging resistance.

At 200°C, the drain-source saturation voltage rises to 3.12V rapidly, which is 72% higher than that at 25°C. At room temperature, it was believed that MOSFET channel resistance dominated the total on-resistance. With an increase of the junction temperature, other scattering mechanisms such as Coulomb and phonon scattering play a dominant role in the thermal emission of electrons from interface traps, so that their collective effects on the channel resistance were somewhat canceled out, increasing the total on-resistance of the SiC MOSFET [16]. Significant improvement was needed to allow the SiC MOSFET operating at the junction temperature of more than 200°C.

Besides the $V_{ds(sat)}$, the gate threshold voltage, $V_{gs(th)}$, is also sensitive to the junction temperature. The transfer characteristics of the SiC MOSFET module are shown in Fig. 3(b). $V_{gs(th)}$ decreases from 3.2V at 25°C to 1.7V at 200°C, resulting in a leftward shift in the *I-V* curve. Due to its faster switching speed, it was suggested that a negative turn-off bias was required to improve the threshold margin and dV/dt immunity to avoid false triggering during the switching process [17].

B. PARASITIC INDUCTANCE

Fig. 4(a) shows the parasitic inductance network of the wire-bondless half-bridge SiC module. The parasitic inductance of the power loop consists of L-HD, L-HS, L-LD, and L-LS. The high-side switch driving circuit inductance consists of L-HG1 and L-HS1 and the low-side switch driving circuit inductance consists of L-LG2 and L-LS2. The DC parasitic inductance of the wire-bondless MOSFET module was extracted using the Ansoft Q3D Extractor. The power loop inductance between the "P" and "N" terminals affects the ringing and overshoot in the drain-source loop of the module [18], and was estimated using the following:

$$L_{\text{power-loop}} = L + M \tag{1}$$

where L is the parasitic inductance, and M is the mutual inductance between the parasitic inductors [19].

A KEYSIGHT E4990A impedance analyzer was used to measure the parasitic inductance between the P and N terminals experimentally. Fig. 4(b) shows the simulated power loop parasitic inductance is ∼5 nH at 4 MHz, which agrees well with the measurement.

C. DYNAMIC ELECTRICAL PROPERTIES

The switching transients of the MOSFET module were characterized by double pulse testing. Fig. 5(a) shows the experimental platform and circuit diagram of the double-pulse tester. The DC bus voltage, V_{CC}, is 450 V. The pulse current, I_d, ranges from 100 A to 150 A. An extra gate resistance, R_g, of 10 Ω was introduced. The load inductance, L, is 100 μH. A specific ceramic heater was used to rise the junction temperature, i.e., T_j, to a specific stable

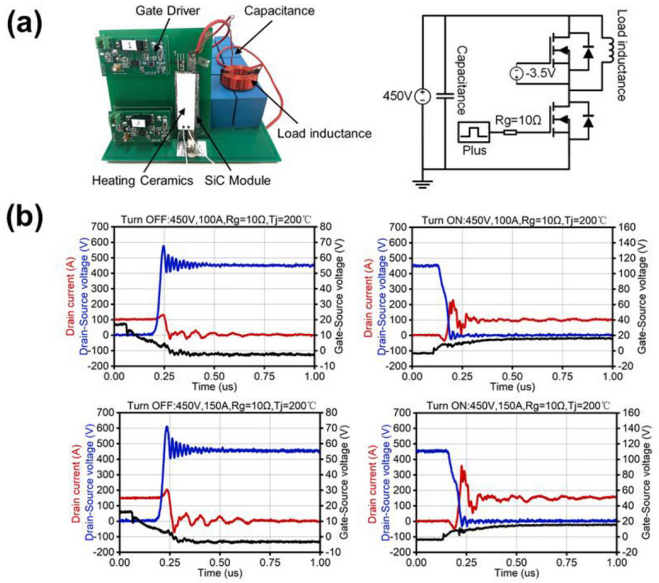

FIGURE 5. **Double-pulse test: (a) test bench and circuit diagram; (b) on and off transients at 200°C.**

TABLE 2. **List of switching time, switching loss, and voltage spike.**

V_{cc}/V	V_{ds} spike /V	△U /V	I_d /A	t_{on} /ns	t_{off} /ns	P_{on} loss /mJ	P_{off} loss /mJ	T_j/°C
450	664	214	150	69.2	171.6	0.18	4	25
450	648	198	150	68	178.8	0.12	3.98	75
450	632	182	150	66.8	190	0.11	4.05	125
450	616	166	150	66.8	198.8	0.19	4.04	200

value ranging from 25°C to 200°C for further measurement. The case temperature was monitored by a thermocouple underneath the bottom AMB substrate. The high-side switch was always forced off by applying V_{ge} of −3.5V. V_{ds} and I_d were recorded by a high-voltage differential probe and a Rogowski Coil, respectively. However, the induced current was easily influenced by the surrounding electric field, so the current waveform has some spurious and unexpected peaks. Only the switching transients of the low-side switch were recorded at different junction temperatures as shown in Fig. 5(b). Table 2 lists the switching time, the switching loss, and the voltage spike of the wire-bondless SiC module.

When the I_d was fixed as 150A and the T_j varied from 25°C to 125°C, the turn-off time increases, and the turn-on time decreases. Due to the presence of parasitic inductance, V_{ds} could generate an overshoot voltage during the turn-off transient of the SiC MOSFET device. The peak voltage dropped by ∼7.2% as from 664V to 616V. The voltage overshoot decreased as the junction temperature increases. The voltage overshoot dropped by ∼22.4% as from 214V to 166V. As the junction temperature increases, the voltage overshoot decreases due to the short turn-off time. At high temperatures, the latching current decreases due to the increased current gain of the NPN and PNP transistors. The decrease in mobility leads to an increase in the resistance of the P-base region, which increases the shutdown time [20]. Although the turn-off time was increased, the turn-off voltage spike could reduce. Consequently, the turn-off losses could be almost constant. As the T_j increases, the gate turn-on voltage decreases and V_{gs} remains at 15V, resulting in a decrease in turn-on time. The decrease in gate turn-on voltage leads to a decrease in turn-on loss.

When the T_j was raised to 200°C, the device can switch normally at $I_d = 100$ A. If continuing to increase the I_d to 150 A, it was observed that the device could not be turned on normally anymore after multiple pulse tests. It was believed that the SiC MOSFET was damaged due to its gate reliability and trapping effect at the SiO_2 interface. Therefore, it was not recommended to operate the SiC MOSFET at the drain current of >150 A at 200°C continuously.

IV. THERMAL PERFORMANCE

Junction-to-case thermal resistance, i.e., R_{th-jc}, is an important parameter for evaluating the thermal performance of power packages. The R_{th-jc} of MOSFET modules can be measured by electrical methods by recording the forward voltage drop of the body diode to estimate the junction temperature in transient condition [21], and V_{sd} as a temperature-sensitive parameter (TSP) was used as follows:

$$R_{th-jc} = \frac{Tj - Tc}{P} \tag{2}$$

$$\triangle T_j = \triangle V_{sd}/K \tag{3}$$

$$\triangle V_{sd} = V_{sd\_i} - V_{sd\_f} \tag{4}$$

where P is the MOSFET body diode power, T_c is the case temperature, which is directly measured by a thermocouple, and T_j is the junction temperature. V_{sd_i} and V_{sd_f} is the voltage variations of the switching process V_{sd} obtained by a real-time recording, and K is the correlation coefficient between TSP and T_j.

Based on the temperature dependence of the forward voltage drop of the diode, the oil bath heating module was used to calculate the K-factor to characterize the relationship between the forward voltage of the diode and its junction temperature. Fig. 6(a) shows the equipment for thermal resistance measurement. The body diode associated with the SiC MOSFET connects with the IGBT in series. The heating period and the cooling period is controlled by turn-on and turn-off the IGBT. To avoid MOSFET chip spontaneous heating, the K factor was measured at a small inductive current of 30 mA. Fig. 6(b) shows the measured K factor of the low-side switch MOSFET body diode, i.e., 2.32 mV/°C.

For single-sided cooling, the SiC module was placed on a water-cooled plate, and the heat of the SiC module was carried away by the flowing circulating cooling water, keeping Tc at 25°C. Then a second water-cooled plate was placed on the module's top substrate and the operation was repeated to measure the thermal resistance under double-sided cooling conditions.

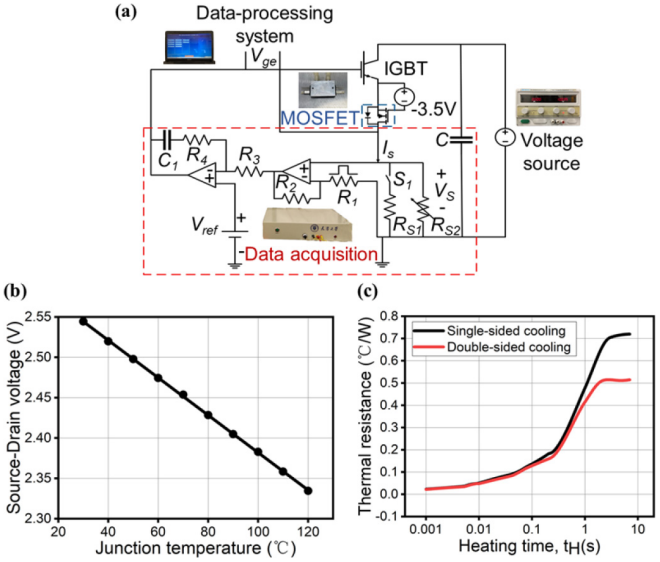

FIGURE 6. (a) Thermal resistance measurement equipment; (b) *K* factor of body diode; (c) thermal resistance comparison under different cooling conditions.

Fig. 6(c) shows the thermal impedance of the SiC module measured at heating times ranging from 0.001 to 7 s and heating power is 28.68 W. When the heating time is less than 250 ms, the heat dissipation is so small that the thermal impedance of the SiC module under the double-sided cooling and the single-sided cooling are 0.17°C/W and 0.19°C/W, respectively. When the heating time is greater than 3 s, the transient thermal impedance changes slightly with the heating time. It was believed that the heat dissipation of the wire-bondless SiC module reach dynamic equilibrium. Therefore, in this paper, we assumed the thermal impedance at a heating time of 7 s as the steady-state thermal resistance, the measured $R_{\text{th}-\text{jc}}$ and the junction temperature of the wire-bondless SiC module under the double-sided cooling are only 0.51°C/W and 39.63 °C, which are ∼28.5% and∼12.8% lower than those under the single-sided cooling, respectively. Therefore, the double-sided cooling can improve the power density of the SiC module greatly.

V. CONCLUSION

In this paper, a 900-V/196-A wire-bondless SiC MOSFET module has been designed, fabricated and characterized up to 200°C. The thermal resistance of the SiC module under the double-sided cooling condition could reach as low as 0.51°C/W, which is 28.5% lower than that under the single-sided cooling condition. The excellent electrical performance and low parasitic parameters at 200°C prove the feasibility of the SiC module for high-temperature application.

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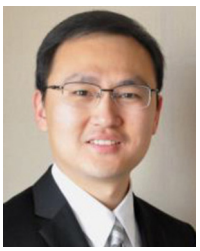

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