Received 15 September 2021; accepted 6 October 2021. Date of publication 11 October 2021; date of current version 18 October 2021.
The review of this article was arranged by Editor J. Wang.

Digital Object Identifier 10.1109/JEDS.2021.3119052

Gray Wolf Optimization-Based Modeling Technique Applied to GaN High Mobility Electron Transistors

ANWAR JARNDAL (Senior Member, IEEE)

Electrical Engineering Department, University of Sharjah, Sharjah, UAE

CORRESPONDING AUTHOR: A. JARNDAL (e-mail: ajarndal@sharjah.ac.ae)

This work was support by the University of Sharjah, UAE.

ABSTRACT In this paper an improved Gray-Wolf-Optimization (GWO) based small-signal modeling is developed. The proposed method is demonstrated by modeling GaN High Electron Mobility Transistors (HEMTs) on SiC and Diamond substrates. The technique bases on engineering the optimization objective function to provide reliable values for the model parameters; while keeping a better fitting for the targeted measurements. The reliability of extraction has been further improved by using physical relevant condition to remove any unrealistic values during the optimization process. The modeling procedure was applied on 2x50-μm, 8x150-μm, 8x250-μm and 16x250-μm GaN HEMTs on SiC substrate in addition to 2x125-μm and 4x125-μm GaN HEMTs on Diamond substrate. Very good results were obtained for both technologies with an excellent fitting for the related measurements. The results also show the reliability of the developed technique and validate its applicability for small- and large-signal modeling applications.

INDEX TERMS GaN HEMT, gray Wolf optimization, scattering parameter measurements, semiconductor device modeling, silicon carbide substrate, Diamond substrate.

I. INTRODUCTION

Small- and large-signal modeling of new microwave transistors such as GaN High Electron Mobility Transistors (HEMTs) is attracting topic of research [1]–[7]. There is still great interest, especially for small-signal modeling of the new version of the GaN device on Diamond substrate [8]–[10]. The important of the small-signal modeling is coming from its nature as a base for large-signal and noise modeling of the device [11]–[16]. The small-signal modeling becomes challenging with increasing the operating frequency toward the targeted millimeter-wave range for the future wireless communication systems. This high frequency stimulates extra parasitic effects that must be counted in the equivalent circuit model. To improve the quality of services, the millimeter-wave systems are adopted to work at higher power based on large-periphery devices of complicated structures. This accordingly further enhance the distributed parasitic effects and the small-signal model becomes more complicated with higher number of elements. These distributed effects [17], [18] in addition to non-quasi-static (NQS) effects [19], [20] make the model parameters extraction more difficult. Direct extraction technique was widely reported and successfully implemented for standard model [21], [22] such as the one presented in Fig. 1-a. However, this method is not working with the distributed model in Fig. 1-b. The number of unknown model parameters is greater than the typically used S-parameters measurements. In this case, optimization based extraction process will be crucially needed. Many optimization extraction methods were demonstrated over the last years [23]–[26].

As well known, the local minima are typical problems with the optimization methods, especially for local approaches including gradient and simplex methods [27]. The optimization process could stack in a local minimum instead of attaining the global solution and thus physical

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

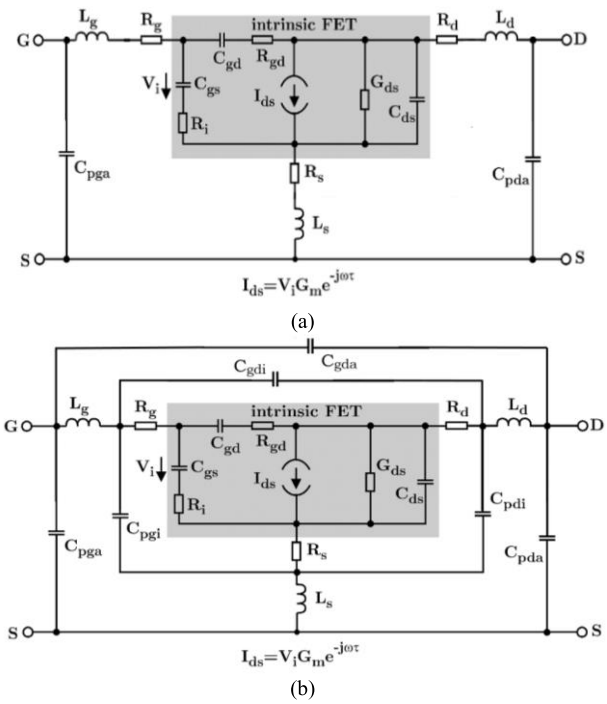

FIGURE 1. **Small-signal equivalent-circuit model for GaN HEMT: (a) standard model (b) distributed parasitic capacitance model.**

non-relevant values could be obtained [27]. The performance depends on the initial guess and thus many techniques have been reported to address this problem. One of these techniques is the hybrid approach based on combining the optimization and direct methods [28], [29]. The direct method could be used to initiate the extraction process by generating reliable estimation for the equivalent-circuit elements, which would then be used as an appropriate starting point for the local optimization process [28]. The reliability of the initial and thus the final values depends on the base measurements. In this case, the measurement uncertainty will influence the quality of the starting values obtained from the first phase of direct extraction. To address this issue an extraction method was reported in [1] to find reliable values for the model elements by means of global optimization. The technique is based on engineering the objective function to have more physical relevant restrictions such as the quasi-static behavior of the intrinsic transistor. This technique has been further improved in this paper by adding extra bias conditions and restrictions to improve the reliability of model parameters extraction. This could be observed from the S-parameters presented in Fig. 2 at triode-forward bias condition. As can be seen, the current proposed procedure provides better fitting with respect to the reported one in [1]. As it will be presented in the next Sections, this method is also demonstrated by small-signal modeling of several GaN HEMTs on SiC and Diamond substrates.

The main additional contributions of this paper with respect to the reported work in [1] are: (i) further enhancement of the objective function by adding extra bias

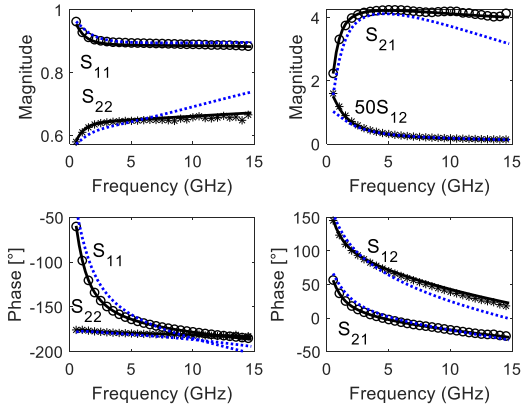

FIGURE 2. **Fitting of measured S-parameters (symbols) using the reported method in [1] (dotted lines) and the current proposed technique (solid lines) applied on 1-mm GaN HEMT-on-SiC at V_{GS} = 1 V and V_{DS} = 5 V.**

conditions in forward-triode region and a reliability condition during the optimization process; (ii) using the recent technique of gray wolf optimization (GWO) [30]; (iii) extended demonstration by modeling different sizes of GaN HEMTs on SiC and Diamond substrates over wide range of bias conditions. This paper is structured as follows. The investigated devices and their characterization are described in Section II. The GWO based procedure, the developed modeling technique and the obtained results are presented and discussed in Section III. Finally, conclusions are provided in Section IV.

II. DEVICE PHYSICS AND EQUIVALENT CIRCUIT MODEL

The considered SiC based on-wafer devices fabrication process is reported in [31]. All of these devices have the same gate length of 0.15 μm with different gate widths of 2x50 μm, 8x125 μm, 8x250 μm and 16x250 μm. The characterization was done using a broadband vector network analyzer (VNA). The VNA calibration was based on the line-reflect-match method using the 104-783 wide-band Impedance Standard Substrates calibration kit from Cascade Microtech Inc. [32]. The other devices are fabricated on 500 μm diamond substrates. More details about the epitaxial structure and fabrication process have been reported in [33]. The devices have a gate length of 0.25 μm and different gate widths of 2x125 μm and 4x125 μm. The model in Fig. 1-b was adopted to simulate the small-signal characteristics including the expected distributed parasitic effects at high frequency. As it was mentioned, the higher frequencies stimulate extra distributed parasitic effects and, in this case, the extrinsic capacitances can be distributed between pad (C_{pga}, C_{pda} and C_{gda}) and inter-electrode (C_{pgi}, C_{pdi} and C_{gdi}) capacitances. These parasitic effects become more obvious in large-periphery multi-finger devices. This also will improve the de-embedding process and enable us to develop a scalable model that can be used to predict the performance of larger devices.

III. GRAY WOLF OPTIMIZATION

Gray Wolf Optimization has been used to find optimal values for the extrinsic elements of the small-signal model.

The model elements are optimized to minimize the error (maximize the fitness) between the simulated and measured S-parameters at "cold" pinch-off condition. The error is defined as:

$$\varepsilon = \varepsilon_r + k_1\sigma_{Cgs} + k_2\sigma_{Cgd} + k_3\sigma_{Cds} + k_4\sigma_{Gm} \quad (1)$$

$$where,\ \ \varepsilon_r = \frac{1}{N}\left\| \sum_{n=1}^{N} \sum_{\substack{i=1,2 \\ j=1,2}} \left[\left(Re\left(S_{ij,n}^{m} - S_{ij,n}^{p} \right) \right)^2 + \left(Im\left(S_{ij,n}^{m} - S_{ij,n}^{p} \right) \right)^2 \right] \frac{1}{W_{ij}} \right\|. \quad (2)$$

N in (2) is the total number of the considered frequency points and S^{m} and S^{p} are the measured and simulated Pinch-off S-parameters, respectively. W_{ij} in (2) is a weighting factor used to de-emphasise data points that show high uncertainty. The impact of measurement uncertainty increases in the pinch-off measured data of high reflection/low transmission coefficients [3], [34]. σ_{Cgs}, σ_{Cgd}, σ_{Cds}, and σ_{Gm} in (1) are the normalized mean standard deviations of C_{gs}, C_{gd}, C_{ds}, and G_m, respectively, at different bias conditions [1]. As it was explained in [1], these are selected to cover typical classes of linear-mode of operation. In this work, additional bias condition at triode-forward was added to cover also switching-mode of operation. The extraction procedure is summarized by the flow chart in Fig. 3. These steps are applied to find the extrinsic capacitive elements of the model in Fig. 1-b. As it is well known that the GWO algorithm is inspired by gray wolves, and it mimics their strict leadership hierarchy and hunting mechanisms. The algorithm is based on definition of four best candidate solutions (of lower error) corresponding to the four typical types of gray wolves: alpha, beta, delta and omega [30]. α is considered to be the first optimal solution, β is the second best solution and δ is the third best solutions. The remaining candidate solutions or search agents are assumed to be the ω wolves and their positions are updated according to the positions of α, β and δ as follows [30]:

$$\vec{X}(t+1) = \frac{\vec{X}_1(t) + \vec{X}_2(t) + \vec{X}_3(t)}{3}. \quad (3)$$

$\vec{X}_1(t)$, $\vec{X}_2(t)$ and $\vec{X}_3(t)$ are calculated based on the current positions of α, β and δ ($\vec{X}_\alpha(t)$, $\vec{X}_\beta(t)$ and $\vec{X}_\delta(t)$) as follows:

$$\vec{X}_1(t) = \vec{X}_\alpha(t) - A\left| C\vec{X}_\alpha(t) - \vec{X}(t) \right| \quad (4)$$

$$\vec{X}_2(t) = \vec{X}_\beta(t) - A\left| C\vec{X}_\beta(t) - \vec{X}(t) \right| \quad (5)$$

$$\vec{X}_3(t) = \vec{X}_\delta(t) - A\left| C\vec{X}_\delta(t) - \vec{X}(t) \right|. \quad (6)$$

The current t^{th} iteration and next $(t+1)^{\mathrm{th}}$ iteration position vector of the search agent are represented by $\vec{X}(t)$ and $\vec{X}(t+1)$, respectively. Equations (3)-(6) represent a mathematical model to mimic encircling the prey and hunting process (finding the best fitness or minimum-error solution). The coefficient vectors $\vec{A}$ and $\vec{C}$ in (4)-(6) are given by:

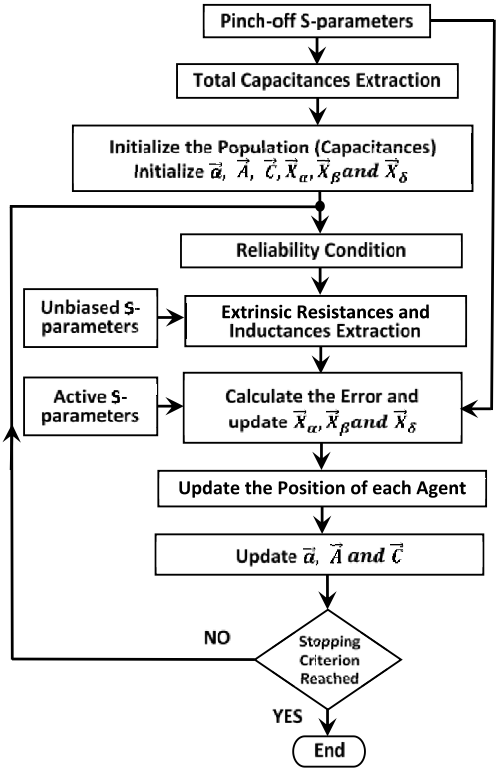

FIGURE 3. Flow chart for the Gray-Wolf optimization procedure.

$$\vec{A} = 2\vec{a}.\vec{r}_1 - \vec{a} \quad (7)$$

$$\vec{C} = 2.\vec{r}_2. \quad (8)$$

$\vec{r}_1$ and $\vec{r}_2$ are random vectors $\in [0, 1]$ to improve the exploration capability of the algorithm and avoid local optima [30]. Vector $\vec{a}$ is linearly decreasing from 2 to 0 over the course of iterations to update the value of $\vec{A}$ and thus the gray wolf position. It is clear from (7) that when $|\vec{A}| < 1$, the gray wolves will be in an exploitation phase to attack the prey (the best solution); while if $|\vec{A}| > 1$, the gray wolves are in the exploration phase and diverge from the prey hoping to find a better prey (better solution). The varying value of A provides a good compromise between exploration and exploitation [30]. As can be seen from (8), the coefficient C has a random value and this will further enhance the exploration and prevent stacking in local solutions. The GWO based extraction process is summarized by the flow chart in Fig. 3. As it is illustrated in the figure, the process is started by using a low-frequency pinch-off S-parameters measurements of the considered device to find the total capacitances C_{gst}, C_{dst}, C_{gdt}, which are used as upper boundaries for the initially generated values of the 6 optimization variables C_{pga}, C_{pda}, C_{gda}, C_{pgi}, C_{pdi} and C_{gdi}. The following conditions in (9)-(11) are then used to remove any non-reliable values for the

TABLE 1. Extracted elements of the model for different size GaN HEMTs on SiC Substrate at pinch-off bias condition.

Model Element	GaN-on-SiC HEMT		
	8x125-μm	8x250-μm	16x250-μm
C_{gs} (fF)	197.7	414.1	840.6
C_{gd} (fF)	109.0	427.9	936.7
C_{ds} (fF)	65.2	254.3	366.5
R_g (Ω)	0.91	1.53	0.81
R_d (Ω)	2.39	0.94	1.14
R_s (Ω)	0.75	0.47	0.23
L_g (pH)	69.3	79.0	117.7
L_d (pH)	56.8	71.0	96.3
L_s (pH)	0.6	4.8	5.3
C_{pga} (fF)	132.6	40.0	150.8
C_{pda} (fF)	79.2	42.2	187.2
C_{gda} fF)	13.8	38.2	51.2
C_{pgi} (fF)	195.8	112.0	169
C_{pdi} (fF)	183.1	174.4	417.6
C_{gdi} (fF)	152.1	25.1	56.3

extrinsic capacitances.

$$C_{pga} + C_{pgi} < C_{gst} \tag{9}$$

$$C_{pda} + C_{pdi} < C_{dst} \tag{10}$$

$$C_{gda} + C_{gdi} < C_{gdt}. \tag{11}$$

The GW based searching process is then conducted to find the optimal values of these capacitances. As can be seen in the flow chart, the reliability condition is applied at each iteration to improve the reliability of extraction. For each assigned values of the extrinsic capacitances, the corresponding values of R_g, R_d, R_s, L_g, L_d and L_s are extracted from Unbiased S-parameters measurements of the same device. The same extrinsic elements are then de-embedded from the pinch-off S-parameters measurements to find the intrinsic capacitances C_{gs}, C_{gd} and C_{ds}. All model elements are then used to simulate the pinch-off S-parameters and find the error ε_r according to (2). The same extrinsic elements are de-embedded from active S-parameters measurements at different bias conditions to find the standard deviations σ_{Cgs}, σ_{Cgd}, σ_{Cds} and σ_{Gm} of the corresponding intrinsic elements. Summation of the fitting error and the standard deviations represent the total error objective function according to (1). These steps are applied to all candidate solutions of the extrinsic elements at each iteration.

The procedure was implemented in MATLAB and applied to the investigated devices of different sizes. These include 100-μm, 1-mm, 2-mm and 4-mm gate-width GaN-on-SiC transistors and 250-μm and 500-μm GaN-on-Diamond devices. The implemented pinch-off S-parameters measurements are at $V_{GS} = -6$ V and $V_{DS} = 0$ V for the SiC based devices; while these measurements are taken at $V_{GS} = -3$ V and $V_{DS} = 0$V for the other devices on Diamond substrate. The active S-parameters measurements are at: ($V_{GS} = -4$ V, $V_{DS} = 25$ V), ($V_{GS} = -3$ V, $V_{DS} = 21$ V), ($V_{GS} = -2$ V, $V_{DS} = 15$ V) and ($V_{GS} = 1$ V, $V_{DS} = 5$ V) for all devices. All measurement was conducted at 25 °C ambient temperature. The results of extrinsic elements extraction are listed in Tables 1 and 2. Furthermore,

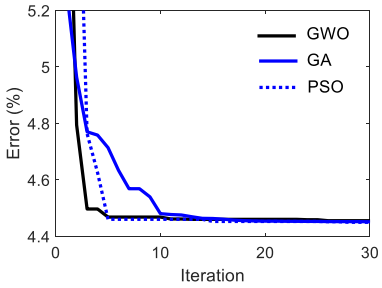

FIGURE 4. Error versus the number of iteration for optimizing the model elements of 8x250-μm device using GWO, PSO and GA.

TABLE 2. Extracted values for the model element of GaN on Diamond HEMTs at pinch-off bias condition.

Model Element	GaN-on-Dia HEMT	
	2×125-μm	4×125-μm
C_{pga} (fF)	4.0	24.6
C_{pda} (fF)	1.62	8.6
C_{gda} (fF)	1.36	10.9
C_{pgi} (fF)	34.2	120.8
C_{pdi} (fF)	35.8	82.6
C_{gdi} (fF)	2.9	11.2
R_g (Ω)	3.11	2.1
R_d (Ω)	7.4	3.7
R_s (Ω)	2.0	1.38
L_g (pH)	78.4	67.3
L_d (pH)	50.7	43.4
L_s (pH)	1.9	2.0
C_{gs} (fF)	211.3	355.3
C_{gd} (fF)	108.1	201
C_{ds} (fF)	65.5	80.5

the proposed GWO-based extraction procedure is compared with Particle Swarm Optimization (PSO) [35] and Genetic Algorithm (GA) [36]. The initial population and number of iterations are restricted by 500 individuals (search agents) and 30 number-of- iterations, respectively. Fig. 4 shows that GWO-based technique has a faster speed of convergence with respect to the PSO and GA. The lower control parameters of the GWO makes it faster than the GA. In addition, it has better exploration capability with respect to the PSO and thus better performance for solving larger scale problems of higher number of optimization variables [37]. The three extraction procedures were implemented using a computer with 1.9 GHz Core-i7 processor and 16 GB RAM. The computation time for GA is 425 seconds, for GWO is 415 seconds and for PSO is 494 seconds. It is clear that the GWO has less computation time with respect to the other techniques.

As it can be noted from the listed values, the intrinsic capacitances show the typical proportionality of these elements with the total gate width. The pad and interelectrode capacitances show also the expected scale-up with device periphery. This also applies to the inductances, which increase with the higher metallization of the larger devices of larger number of fingers. The contact and semiconductor resistances are inversely proportional with gate width and this is clear from reduced values of R_d and R_s for larger

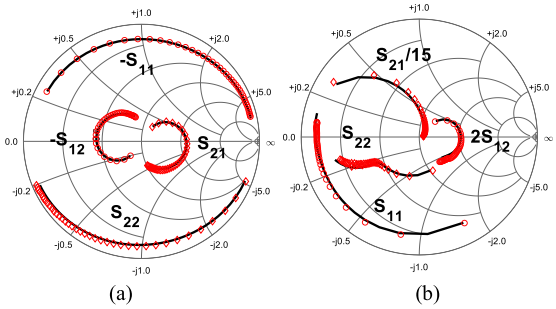

FIGURE 5. Comparison between measurements (symbols) and simulations (lines) for 8x125-μm GN-on-SiC HEMT at: (a) "cold" pinch-off bias condition ($V_{GS} = -6$ V, $V_{DS} = 0$ V) and (b) active bias condition ($V_{GS} = -1$ V, $V_{DS} = 11$ V). The frequency range is from 0.1 to 20 GHz.

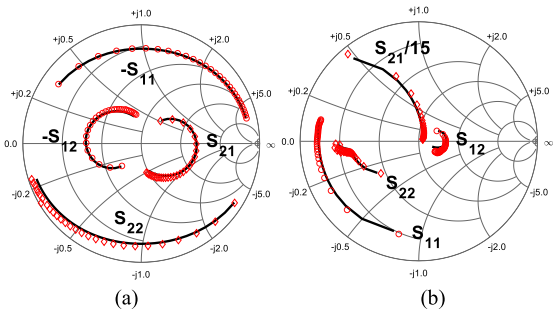

FIGURE 6. Comparison between measurements (symbols) and simulations (lines) for 8x250-μm GN-on-SiC HEMT at: (a) "cold" pinch-off bias condition ($V_{GS} = -6$ V, $V_{DS} = 0$ V) and (b) active bias condition ($V_{GS} = -1$ V, $V_{DS} = 11$ V). The frequency range is from 0.1 to 15 GHz.

devices. As it was reported in [38], the gate resistances R_g is proportional with gate-width and inversely proportional with number of gate fingers. This is clear from the higher value of R_g of 8x250-μm transistor with respect to the 8x125-μm device. This could be observed also from the lower value of R_g for 16x250-μm with respect to the 8x250-μm one. This also applied to the GaN on Diamond devices.

The accuracy of extraction is validated by means of S-parameters fitting, which shows a very good agreement with the measurements at it is illustrated in Figs. 5–9 for the five devices. In general, the outer passive elements of the device/model in the extrinsic part are frequency dependent and should be able to characterize and de-embed the parasitic effects. The intrinsic part of the device, on the other side, characterizes the active area around the channel, which are typically frequency independent. Based on that, the amount of frequency dependency of the intrinsic elements could be used as a measure for the quality of modeling the extrinsic of the device. As can be seen in Figs. 10 and 11, all devices show almost flat curves for the intrinsic elements versus frequency and verify the validity of the proposed model topology and the extraction procedure.

The model reliability was validated also by extracting model elements at different ambient temperature. Table 3 lists the extraction results for 2x50-μm device at 298 °C and

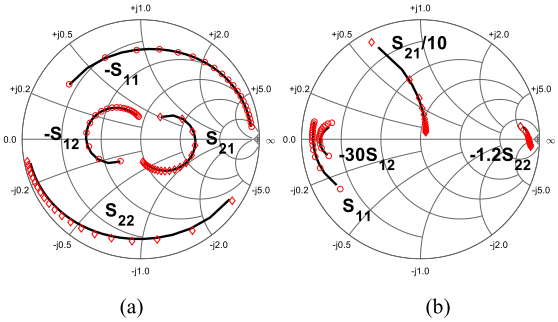

FIGURE 7. Comparison between measurements (symbols) and simulations (lines) for 16x250-μm GN-on-SiC HEMT at: (a) "cold" pinch-off bias condition ($V_{GS} = -6$ V, $V_{DS} = 0$ V) and (b) active bias condition ($V_{GS} = -1$ V, $V_{DS} = 9$ V). The frequency range is from 0.1 to 7 GHz.

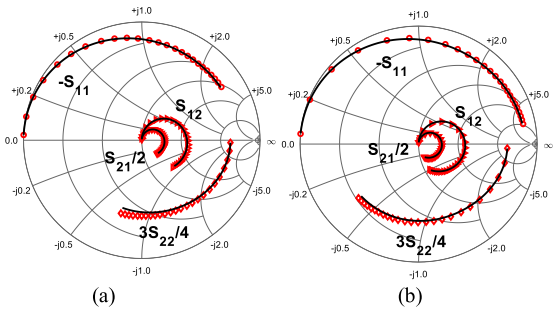

FIGURE 8. Comparison between measurements (symbols) and simulations (lines) at "cold" pinch-off bias condition ($V_{GS} = -3$ V, $V_{DS} = 0$ V) for: (a) 2x125-μm and (b) 4x125-μm GN-on-Dia HEMT. The frequency range is from 0.1 to 20 GHz.

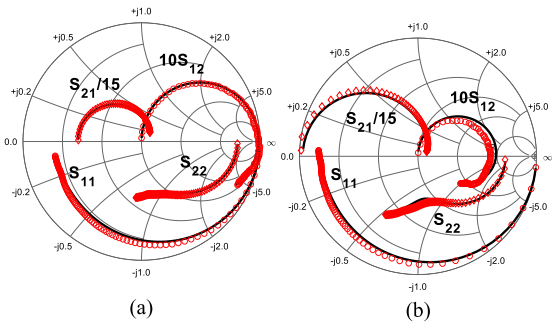

FIGURE 9. Comparison between measurements (symbols) and simulations (lines) for: (a) 2x125-μm GN-on-Dia HEMT at ($V_{GS} = -1.0$ V, $V_{DS} = 20$ V) and (b) 4x125-μm GN-on-Dia HEMT at ($V_{GS} = -1.5$ V, $V_{DS} = 30$ V). The frequency range is from 0.1 to 20 GHz.

328 °C temperatures. The extracted values of the extrinsic resistances show the expected increase with increasing the temperature [39], [40]. This could be attributed to the higher values of the sheet resistivity of the semiconductor material at higher temperatures [39]. Scaling of the intrinsic FET with the gate width is validated by extracting the intrinsic parameters of different sizes devices at the same bias condition. Table 4 lists the extraction results of the investigated devices on SiC substrate at $V_{GS} = -2$ V, $V_{DS} = 21$ V and room temperature of 298 °C. The results are realistic

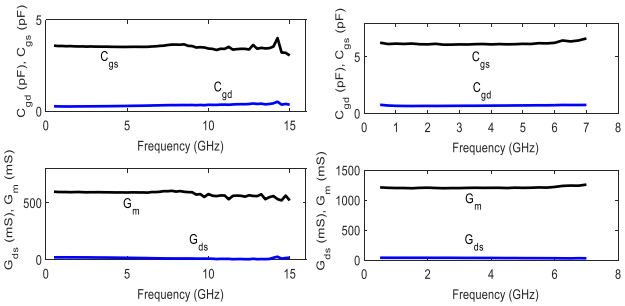

FIGURE 10. Intrinsic elements versus frequency for: (a) 8x250-μm GaN-on-SiC HEMT at $V_{GS} = -1$ V and $V_{DS} = 11$ V and (b) 16x250-μm GaN-on-SiC HEMT at $V_{GS} = -1$ V and $V_{DS} = 9$ V.

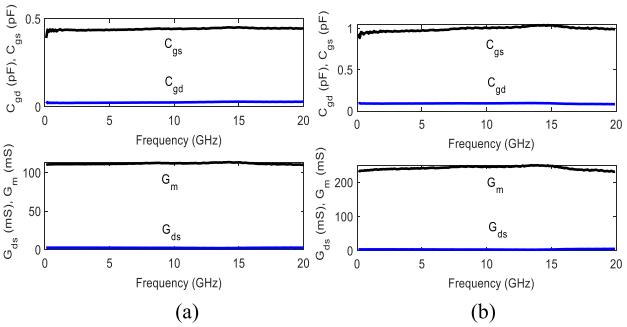

FIGURE 11. Intrinsic elements versus frequency for: (a) 2x125-μm GaN-on-Dia HEMT at $V_{GS} = -1$ V and $V_{DS} = 20$ V and (b) 4x125-μm GaN-on-Dia HEMT at $V_{GS} = -2$ V and $V_{DS} = 15$ V.

TABLE 3. Extracted circuit elements for the model for the 100-μm GaN on SiC HEMT at different ambient temperatures and "cold" pinch-off bias condition ($V_{GS} = -6$ V and $V_{DS} = 0$ V).

Model Element	2x50-μm	
	T=298 K	T=328 K
C_{gs} (fF)	18.0	2.9
C_{gd} (fF)	20.5	13.8
C_{ds} (fF)	17.1	17.9
R_g (Ω)	4.5	6.5
R_d (Ω)	9.4	11.0
R_s (Ω)	6.8	8.4
L_g (pH)	48.6	49.5
L_d (pH)	44.8	31.1
L_s (pH)	0.0	0.0
C_{pga} (fF)	6.7	1.7
C_{pda} (fF)	3.0	1.9
C_{gda} fF)	1.1	1.2
C_{pgi} (fF)	8.4	30.5
C_{pdi} (fF)	16.7	16.3
C_{gdi} (fF)	1.1	8.3

and reflect the unsymmetrical gate capacitance distribution at this bias condition. Typically, C_{gd} has smaller values with respect to C_{gs} under saturation. The results also show the expected scaling of G_m and G_{ds} with the gate width. Also, reliable values are obtained for R_i, R_{gd} and τ.

As it was mentioned, the active intrinsic part of the device is represented by the bias-dependent gate capacitances and conductances in addition to R_i, R_{gs} and τ to characterize

TABLE 4. Extracted intrinsic elements of 1-mm, 2-mm and 4-mm GaN on SiC HEMTs at active bias condition of $V_{GS} = -2$ V and $V_{DS} = 21$ V.

Model Element	Device		
	8x125-μm	8x250-μm	16x250-μm
C_{gs} (pF)	1.78	3.7	6.6
C_{gd} (pF)	0.06	0.18	0.41
C_{ds} (pF)	0.08	0.38	0.55
R_i (Ω)	0.6	1.14	1.2
R_{gd} (Ω)	117.0	49.4	18.5
G_m (mS)	289.6	534.3	1026.6
G_{ds} (mS)	6.8	12.6	22.2
τ (ps)	2.0	2.3	2.2

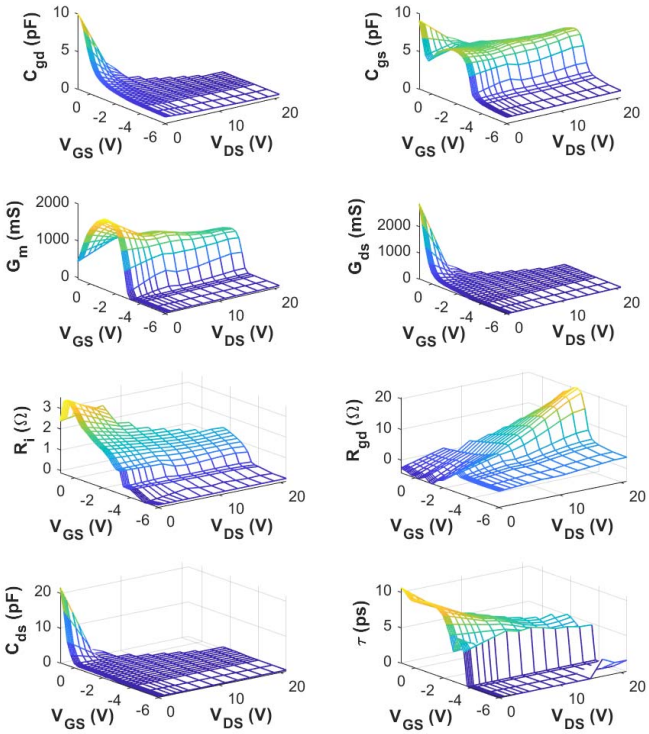

FIGURE 12. Extracted intrinsic parameters versus gate and drain bias voltages for 16×250-μm GaN-on-SiC HEMT.

the non-quasi-static behavior. Fig. 12 show the extracted values of the intrinsic elements at grid of bias voltages: V_{GS} from −6 V to 1 V and V_{DS} from 0 V to 21 V. The values show the typical expected behavior of the intrinsic transistor with the drain and gate voltages. As can be seen, C_{gs} is rapidly decrease in pinch-off because the depletion region under the gate, which determine the effective separation of this capacitor, extends all the way to the heterojunction at high negative gate voltage [41]. The higher extension of the depletion region into the gate-drain side (at higher drain voltage) results in smaller values of C_{gd} with increasing V_{DS}. Under triode-forward bias condition, the depletion region is diminished to symmetrically distributed around the gate metallization and thus as it was expected C_{gs} and C_{gd} show almost similar values. It is clear from the curves the effect of self-heating on G_m, which results in reduced values in the high-power-dissipation (higher drain current and voltage)

areas. The power dissipation induced self-heating degrades the electron saturation velocity and therefore reduces the drain current and the channel transconductnce. R_i simulates the charging process of C_{gs} through the undepleted part of the channel under the gate [42]. The value of R_i is determined by the voltage drop across this part of the channel and the drain current [42]. Thus, as it is expected R_i should have higher values in the triode region of lower drain current. C_{ds} characterizes the drain-source capacitances separated by the high-field part of the depletion layer under triode bias conditions [41]. Thus as it can be observed, this capacitance has higher values at low V_{DS} and V_{GS} bias conditions in the forward-triode region.

IV. CONCLUSION

In this paper the applicability of using a recently develop global optimization of gray wolf algorithm on small-signal modeling of transistors has been demonstrated. The technique has been adopted to provide reliable values for the model elements. It was found that the reliability of extraction can be improved by proper engineering of the objective function and adding more physically relevant constraints. This could be achieved by targeting accuracy and reliability objectives. The first objective was represented by the fitting-error; while the second objective was characterized by the intrinsic elements standard deviation as a measure for the extent of the quasi-static behavior of the intrinsic transistor. The proposed method has been used to simulate GaN HEMTs of different substrates, different sizes, different temperatures and different bias conditions. Very good results have been obtained and validate the applicability of the developed technique for both small-and large-signal modeling of active devices. This also validates the technology independence of the method and its applicability for different types of FETs.

REFERENCES

[1] A. Jarndal, G. Crupi, A. Raff, V. Vadal, and G. Vannini, "An improved transistor modeling methodology exploiting the quasi-static approximation," *IEEE J. Electron Devices Soc.*, vol. 9, pp. 378–386, 2021.

[2] X. Du *et al.*, "ANN-based large-signal model of AlGaN/GaN HEMTs with accurate buffer-related trapping effects characterization," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 7, pp. 3090–3099, Jul. 2020, doi: 10.1109/TMTT.2020.2990171.

[3] J. A. Z. Flores and G. Kompa, "Closed-form extraction strategy of physically meaningful parameters of small-signal HEMT models with distributed parasitic capacitive effects," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 2, pp. 1227–1237, Feb. 2021.

[4] S. Colangeli *et al.*, "Nondestructive, self-contained extraction method of parasitic resistances in HEMT devices," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 7, pp. 2571–2578, Jul. 2020.

[5] A. Jarndal, "On neural networks based electrothermal modeling of GaN devices," *IEEE Access*, vol. 7, pp. 94205–94214, 2019.

[6] G. Crupi, A. Caddemi, D. M. M.-P. Schreurs, and G. Dambrine, "The large world of FET small-signal equivalent circuits," *Int. J. RF Microw. Comput. Aided Eng.*, vol. 26, no. 9, pp. 749–762, 2016.

[7] A. Jarndal and G. Kompa, "A new small-signal modeling approach applied to GaN devices," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 11, pp. 3440–3448, Nov. 2005.

[8] A. Jarndal, X. Du, and Y. Xu, "Modelling of GaN high electron mobility transistor on diamond substrate," *IET Microw. Antennas Propag. J.*, vol. 15, no. 6, pp. 661–673, 2021. [Online]. Available: https://doi.org/10.1049/mia2.12093

[9] Y. Chen *et al.*, "Temperature-dependent small signal performance of GaN-on-diamond HEMTs," *Int. J Numer Model.*, vol. 33, no. 3, 2020, Art. no. e2620.

[10] A. Jarndal, L. Arivazhagan, and D. Nirmal, "On the performance of GaN on silicon, silicon-carbide, and diamond substrates," *Int. J. RF Microw. Comput. Aided Eng.*, vol. 30, no. 6, Jun. 2020, Art. no. e22196.

[11] A. Jarndal, A. Hussein, G. Crupi, and A. Caddemi, "Reliable noise modeling of GaN HEMTs for designing low-noise amplifiers," *Int. J. Numer. Model. Electron. Netw. Devices Fields*, vol. 33, no. 3, Mar. 2019, Art. no. e2585.

[12] F. Danneville, "Microwave noise and FET devices," *IEEE Microw. Mag.*, vol. 11, no. 6, pp. 53–60, Oct. 2010.

[13] A. Nalli *et al.*, "GaN HEMT noise model based on electromagnetic simulations," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 8, pp. 2498–2508, Aug. 2015.

[14] A. Jarndal and G. Kompa, "An accurate small-signal model for AlGaN-GaN HEMT suitable for scalable large-signal model construction," *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 6, pp. 333–335, Jun. 2006.

[15] A. Jarndal and G. Kompa, "Large-signal model for AlGaN/GaN HEMT accurately predicts trapping and self-heating induced dispersion and intermodulation distortion," *IEEE Trans. Electron Devices*, vol. 54, no. 11, pp. 2830–2836, Nov. 2007.

[16] A. Jarndal, A. Z. Markos, and G. Kompa, "Improved modeling of GaN HEMT on Si substrate for design of RF power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 3, pp. 644–651, Mar. 2011.

[17] S. Lee, P. Roblin, and O. Lopez, "Modeling of distributed parasitics in power FETs," *IEEE Trans. Electron Devices*, vol. 49, no. 10, pp. 1799–1806, Oct. 2002.

[18] T. T.-L. Nguyen and S.-D. Kim, "A gate-width scalable method of parasitic parameter determination for distributed HEMT small-signal equivalent circuit," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 10, pp. 3632–3638, Oct. 2013.

[19] A. Raffo *et al.*, "Nonlinear dispersive modeling of electron devices oriented to GaN power amplifier design," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 4, pp. 710–718, Apr. 2010.

[20] G. Crupi, D. M. M.-P. Schreurs, A. Caddemi, A. Raffo, and G. Vannini, "Investigation on the non-quasi-static effect implementation for millimeter-wave FET models," *Int. J. RF Microw. Comput.-Aided Eng.*, vol. 20, no. 1, pp. 87–93, 2010.

[21] A. Jarndal and G. Kompa, "A simple, direct and reliable extraction method applied to GaN devices," *Int. J. Electron.*, vol. 104, no. 3, pp. 1–12, 2017.

[22] Y. Chen *et al.*, "A reliable and efficient small-signal parameter extraction method for GaN HEMTs," *Int. J. Numer. Model. Electron. Netw. Devices Fields*, vol. 33, no. 3, 2020, Art. no. e2540.

[23] G. P. Gibiino, A. Santarelli, R. Cignani, P. A. Traverso, and F. Filicori, "Measurement-based automatic extraction of FET parasitic network by linear regression," *IEEE Microw. Wireless Compon. Lett.*, vol. 29, no. 9, pp. 598–600, Sep. 2019.

[24] A. Jarndal, "Hybrid extraction method based on pinch-off S-parameters for Mm-Wave modeling of GaN HEMTs," in *Proc. IEEE 59th Int. Midwest Symp. Circuits Syst.*, Oct. 2016, pp. 1–4.

[25] A. Majumder, S. Chatterjee, S. Chatterjee, S. S. Chaudhari, and D. R. Poddar, "Optimization of small-signal model of GaN HEMT by using evolutionary algorithms," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 4, pp. 362–364, Apr. 2017.

[26] A. Jarndal, "On modeling of substrate loading in GaN HEMT using grey wolf algorithm," *J. Comput. Electron.*, vol. 19, pp. 576–590, Feb. 2020.

[27] M. Rudolph, *Nonlinear Transistor Model Parameter Extraction Techniques*. Cambridge, U.K.: Cambridge Univ. Press, 2011.

[28] A. Jarndal, R. Essaadali, and A. B. Kouki, "A reliable parasitic extraction method applied to AlGaN/GaN HEMTs," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 35, no. 2, pp. 211–219, Feb. 2016.

[29] A. Jarndal and A. S. Hussein, "Hybrid small-signal model parameter extraction of GaN HEMTs on Si and SiC substrates based on global optimization," *Int. J. RF Microw. Comput.-Aided Eng.*, vol. 29, no. 10, 2019, Art. no. e21555.

[30] S. Mirjalili, S. M. Mirjalili, and A. Lewis, "Grey wolf optimizer," *Adv. Eng. Softw.*, vol. 69, pp. 46–61, Mar. 2014.

[31] R. Lossy, N. Chaturvedi, P. Heymann, J. Würfl, S. Müller, and K. Köhler, "Large area AlGaN/GaN HEMTs grown on insulating silicon carbide substrates," *Physica Status Solidi A*, vol. 194, no. 2, pp. 460–463, 2002.
[32] *104-783 W-Band Impedance Standard Substrate*, Cascade Microtech, Inc., Beaverton, OR, USA, 2004.
[33] Q. Wu *et al.*, "Performance comparison of GaN HEMTs on diamond and SiC substrates based on surface potential model," *ECS J. Solid State Sci. Technol.*, vol. 6, no. 12, pp. Q171–Q178, 2017.
[34] A. Jarndal, "Measurements uncertainty and modeling reliability of GaN HEMTs," in *Proc. Int. Conf. Model. Simulat. Appl. Optim. Conf.*, Tunisia, Hammamet, Apr. 2013, pp. 1–4.
[35] J. Kennedy and R. Eberhart, "Particle swarm optimization," in *Proc. IEEE Int. Conf. Neural Netw.*, vol. 4, 1995, pp. 1942–1948.
[36] M. Mitchell, *An Introduction to Genetic Algorithms*. Cambridge, MA, USA: MIT Press, 1998.
[37] J. Fan, M. Hu, X. Chu, and D. Yang, "A comparison analysis of swarm intelligence algorithms for robot swarm learning," in *Proc. Winter Simulat. Conf.*, Las Vegas, NV, USA, Dec. 2017, pp. 3042–3053.
[38] P. Aaen, J. A. Plá, and J. Wood, *Modeling and Characterization of RF and Microwave Power FETs*. Cambridge, U.K.: Cambridge Univ. Press, 2007.
[39] G. Crupi *et al.*, "Temperature influence on GaN HEMT equivalent circuit," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 10, pp. 813–815, Oct. 2016.
[40] M. A. Alim, A. A. Rezazadeh, and C. Gaquiere, "Small signal model parameters analysis of GaN and GaAs based HEMTs over temperature for microwave applications," *Solid-State Electron.*, vol. 119, pp. 11–18, May 2016.
[41] H. Rohdin *et al.*, "0.1-μm gate-length AlInAs/GaInAs/GaAs MODFET MMIC process for applications in high-speed wireless communications," *Hewlett-Packard J.*, vol. 49, pp. 1–37, Feb. 1998.
[42] P. Ladbrooke, *MMIC Design GaAs FETs and HEMTs*. Norwood, MA, USA: Artech House, 1988.

ANWAR JARNDAL (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from the University of Kassel, Kassel, Germany, in 2006. He was a Postdoctoral Fellow of the École de Technologie Superieure, Quebec University, Canada. He is currently an Associate Professor with the Department of Electrical Engineering, University of Sharjah. He has published over 100 internationally peer-reviewed publications. He has many research interests include active devices modeling, measurements and characterization techniques, power amplifiers design, low-noise amplifier design, local and global optimizations, artificial neural networks, machine learning, fuzzy logic, radio channel modeling, and wireless power transfer. He received the University of Sharjah Annual Incentives Award for distinguished faculty in scientific research. His was also classified as one of the World's Top 2% Scientists 2020 (Stanford University). He serving as a reviewer for more 20 international journals.