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Study on CDM ESD Robustness Among On-Chip Decoupling Capacitors in CMOS Integrated Circuits

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ABSTRACT The integrated circuit (IC) products fabricated in the scaled-down CMOS processes with higher clock rate and lower power supply voltage (V_{DD}) are more sensitive to the transient/switching noises on the power lines with the parasitic inductance induced by the bonding wire. The typical method to suppress the power line noise is to add on-chip decoupling capacitors. Meanwhile, electrostatic discharge (ESD) is also a challenging issue on IC reliability in advanced CMOS technology. For the ICs fabricated in an advanced process, with the thinner gate oxide, the circuits are particularly vulnerable to the charged-device model (CDM) ESD events. However, there was very limited research to investigate the ESD robustness on the decoupling capacitors, especially during the CDM ESD events. In this work, the CDM ESD robustness among different types of decoupling capacitors in ICs was investigated in a 0.18-μm CMOS technology.

INDEX TERMS Power line noise, transient/switching noise, parasitic inductance, decoupling capacitor, charged-device model (CDM), electrostatic discharge (ESD).

I. INTRODUCTION

Owing to the continued scaling down of CMOS technology, the IC products had been operated under the condition of higher clock rate and lower power supply voltage. Maintaining the quality of power supply voltage has become a critical issue, because modern IC products were increasingly sensitive to noise sources, such as the simultaneous switching noise on power lines [1]. The power line noise is related to the switching activity and the current consumption of the circuits [2] with the parasitic component of parasitic inductance induced by the bonding wire. The noise on the power line will cause the degradation of the circuit performance, and also cause the reliability issue. To maintain the quality of the power supply voltage, the most common method is to place the on-chip decoupling capacitors between the power lines of V_{DD} and Vss to reduce the noise arising from IR drop and Ldi/dt effect.

With the progress of CMOS technology, the thinner gate oxide encounters serious ESD reliability issue, especially the charged-device model (CDM) ESD events. The lower oxide breakdown voltage caused by thinner gate oxide was very vulnerable to the charged-device model (CDM) ESD events, which can easily cause damage to the internal circuits and hence need additional ESD protection design [3]–[8]. The discharging current of CDM ESD can be taken as a high-frequency signal. For a high-frequency signal, a low resistive path is provided by the decoupling capacitor due to the physical characteristic ($Z = 1/sC$). Thus, the CDM ESD current will be easily discharged through the decoupling capacitor to cause damage on it, when the CDM ESD is directly discharged from the V_{DD} pin. So far, there were some few reports on investigating the decoupling capacitors with HBM (human-body model) ESD events [9]–[10]. Recently, a study to optimize the MIM (metal-insulator-metal) decoupling capacitor with consideration on CDM robustness was reported [11]. But, no report has studied the MOS decoupling capacitors with CDM ESD events.

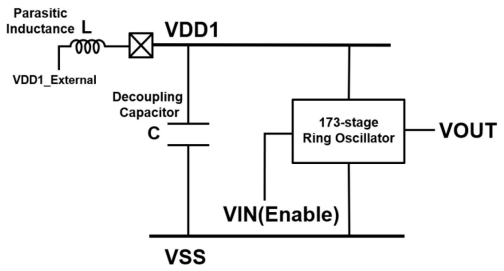

FIGURE 1. **Block diagram of the test circuit and the parasitic inductance induced by the bonding wire. The test circuit includes a ring oscillator of 173-stage inverter chain and a decoupling capacitor.**

In this work, the test circuits realized with a ring oscillator and three types of decoupling capacitors are used to verify the effectiveness of decoupling capacitors on suppressing the power line noise, and especially to investigate the CDM ESD robustness among three types of decoupling capacitors.

II. INTERNAL ESD THREATS OF ON-CHIP DECOUPLING CAPACITORS

Fig. 1 illustrates the block diagram of the test circuit used in this work. The internal circuit is realized by a ring oscillator of 173-stage inverter chain. With the decoupling capacitor (C) added between the power lines (VDD1 and VSS), the decoupling capacitor can suppress the noise on VDD1 which is induced by the switching of the inverter chain inside the ring oscillator. When an enable signal (VIN) is given to the input pin of the ring oscillator, the ring oscillator starts oscillating, and the inverters inside the inverter chain are switching rapidly to cause rapid current variation. This rapid current variation will flow through the bonding wire of VDD1, the parasitic inductance of the bonding wire will cause the Ldi/dt effect of voltage variation, and hence result in power supply noise on VDD1.

In order to suppress the power line noise, the decoupling capacitor (C) is placed between VDD1 and VSS. From the simulation results shown in Fig. 2 and Table 1, the parasitic inductance is selected as 5nH due to the average bonding wire length in our testkey package, which is estimated with the rule of thumb 1nH/1mm [12]. In addition, the capacitance of decoupling capacitor is selected as 5pF for study purpose. Fig. 2(a) shows the ideal condition of the circuit with an output frequency of 97 MHz generated from the ring oscillator, which is without the presence of parasitic inductance and decoupling capacitor. Fig. 2(b) shows the results with the presence of parasitic inductance (5nH) but without the decoupling capacitor. Fig. 2(c) shows the results with the presence of both parasitic inductance (5nH) and decoupling capacitor (5pF). It is clearly observed that the peak-to-peak voltage of power line noise is reduced in Fig. 2(c), as compared with Fig. 2(b). As listed in Table 1, the simulation results show that the decoupling capacitor indeed achieves the purpose of suppressing the power line noise.

The CDM ESD issue, which can discharge a huge current in a very short time, has become more challenging to

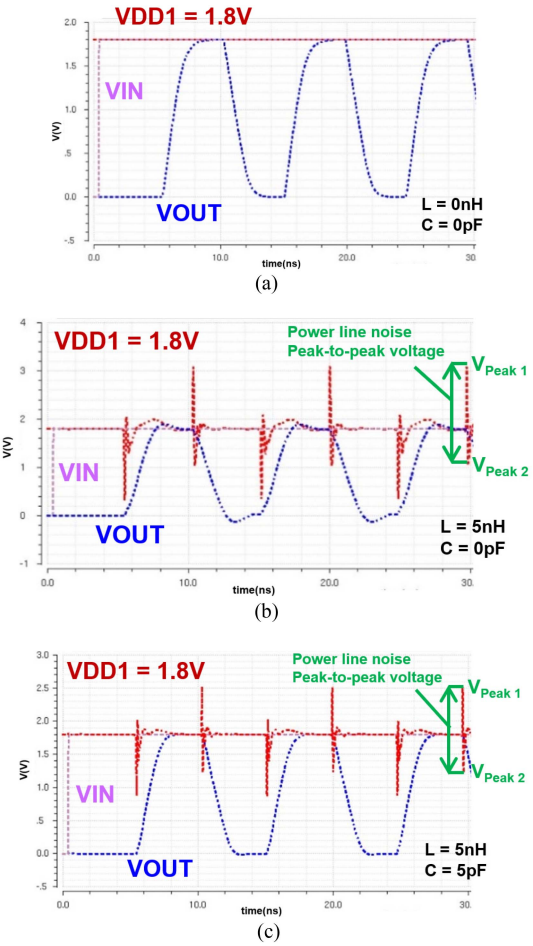

FIGURE 2. **Simulation results of the test circuit (a) without parasitic inductance, (b) with parasitic inductance of 5nH, and (c) with parasitic inductance of 5nH and decoupling capacitor of 5pF. Power line noise induced by the parasitic inductance can be suppressed by decoupling capacitor (the output freq. of ring oscillator is 97MHz).**

TABLE 1. **Simulation results of power line noise with or without decoupling capacitor.**

	$V_{Peak\ 1}$(V)	$V_{Peak\ 2}$ (V)	Power line noise Peak-to-peak voltage (V)
Without decoupling capacitor	3.012	1.036	1.976
With decoupling capacitor	2.514	1.243	1.271

modern IC products with the thinner gate oxide fabricated in the advanced CMOS processes [3]–[8]. Fig. 3 shows the discharging current waveform with the CDM ESD level of +500V from the device under test (DUT) with an equivalent capacitance of 41 pF, as estimated from JEDEC standard [13]. As seen from the measured current transient waveform, the discharging current can reach 7.68A in just 275ps, and the main current pulse is within ~1 ns.

When the CDM ESD is discharging from the VDD1 pin, as illustrated in Fig. 4, a low resistive discharging path is provided by the decoupling capacitor that placed between VDD1 and VSS. The discharging current waveform of CDM can be seen as a high-frequency signal. The low resistive

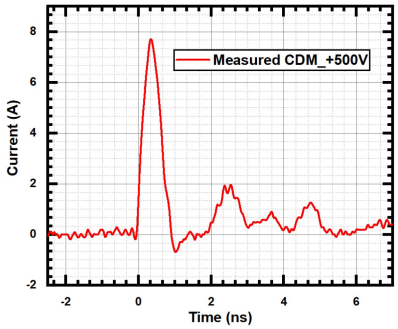

FIGURE 3. Measured CDM ESD current waveform (+500V) from the device under test (DUT) with an equivalent capacitance of 41 pF. The current reaches 7.68A within 275ps, and the main current pulse is within ~1 ns.

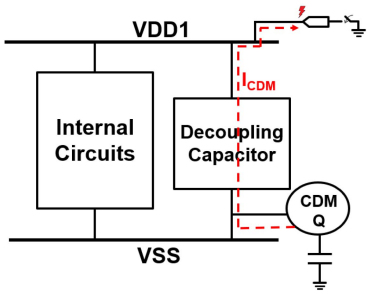

FIGURE 4. The illustration to show CDM ESD current path that will be concentrated to flow through the decoupling capacitor during CDM ESD events, especially when the CDM ESD is discharging from the power pin (VDD1) of internal circuits.

path with its impedance of $Z = 1/sC$ is provided by the decoupling capacitor, thus the CDM discharging current will be concentrated to flow through the decoupling capacitor. If the decoupling capacitor was implemented by the MOS devices with thinner gate oxide, it would be easily damaged during CDM ESD events, especially when the CDM ESD is discharging from the power pin (VDD1) of internal circuits.

III. TEST CIRCUITS FOR INVESTIGATING CDM ROBUSTNESS AMONG DIFFERENT DECOUPLING CAPACITORS

A. RING OSCILLATOR DESIGN

The internal circuit for test chip is realized by a ring oscillator with 173-stage inverter chain, where a decoupling capacitor of ~ 5 pF is added between the power (VDD1) line and ground (VSS) of the ring oscillator. Different types of decoupling capacitors are selected and added to the test chip with the ring oscillator to verify their CDM ESD levels. As shown in Fig. 5, the ring oscillator is designed with 173 inverter stages, not only for the odd number stages to oscillate but also a prime number to minimize the probability of higher harmonic signals [14]. In the inverter chain of 173 inverter stages, one of the inverter stages is replaced by a two-input NAND gate to achieve the purpose of a switch that is used to start or stop the oscillator. The M+1th inverter between the 173-stage ring oscillator and the 4-stage buffer

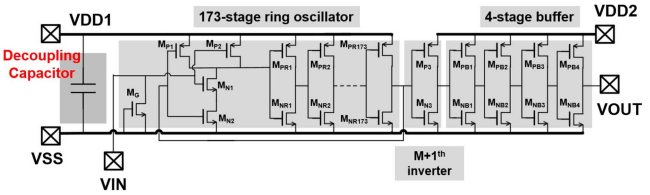

FIGURE 5. The ring oscillator of 173-stage inverter chain with decoupling capacitor was used as the internal circuits of test chip for CDM ESD study, which was designed and fabricated in a 0.18-μm 1.8V CMOS process.

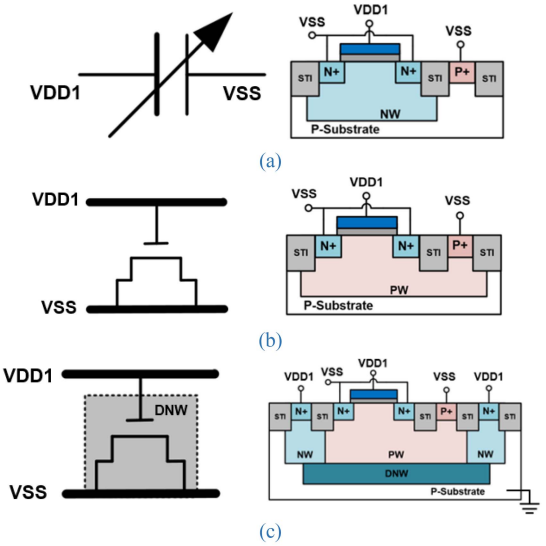

FIGURE 6. The symbols and cross-sectional views of (a) varactor, (b) NMOS capacitor, and (c) NMOS capacitor with DNW.

serves the purpose to partially isolate the effect of the capacitive load [15]. The ring oscillator with decoupling capacitor is separated from the 4-stage buffer, which are placed in two isolated power domains. The 4-stage buffer is used to drive the signal to the output pin for observation on the oscillation frequency that is generated by the 173-stage ring oscillator. To drive the heavy loading at the output pad and the external connection, the traditional tapered buffer circuit with the increased large transistor dimensions was applied [16]. The power line of the 4-stage buffer is supplied by a standalone power pad (VDD2), therefore the power line noise induced by the ring oscillator at the VDD1 can be clearly observed.

B. DECOUPLING CAPACITORS

Three decoupling capacitors were selected and implemented in the test chip with the ring oscillator of 173-stage inverter chain, which were the varactor, NMOS capacitor, and NMOS capacitor with deep N-well (DNW), respectively. The symbol and cross-sectional view of the varactor as decoupling capacitor is shown in Fig. 6(a), whereas Fig. 6(b) shows the symbol and cross-sectional view of the NMOS capacitor. The varactor and NMOS capacitor are selected as the decoupling capacitors, because they have a larger value of effective capacitance per area [2], [17]. Fig. 6(c) shows

TABLE 2. Combinations of test circuits.

Symbol	Description	Decoupling capacitor type
(1) Baseline	ring osc. only	-
(2) Var.	ring osc. + Varactor	Varactor
(3) NMOS_cap.	ring osc. + NMOS	NMOS
(4) NMOS_cap_DNW	ring osc. + NMOS w/ DNW (DNW is biased at VDD1)	NMOS w/ DNW

TABLE 3. Simulation results of decoupling capacitors in layout.

Capacitor type	Spec (pF)	Post-sim (pF)	Area (μm^2)
Var.	5	5.0768	1503.4992
NMOS_cap	5	5.0247	1389.0072
NMOS_cap_DNW	5	6.6539	2704.7219

TABLE 4. Device dimensions of the test circuits.

Subcircuit	Device parameter		
On-chip decoupling capacitor (5pF)	MOS W/L (μm/μm)	Var.	270/2.16
		NMOS_cap	131.1/4.32
		NMOS_cap_DNW	262/2.16
173-stage ring oscillator	MOS W/L (μm/μm)	$M_{P1} = M_{P2} = 2.8/0.18$ $M_{N1} = M_{N2} = 2/0.18$ M_{PR1}~$M_{PR173} = 2.8/0.18$ M_{NR1}~$M_{NR173} = 1/0.18$ $M_G = 120/0.18$	
M+1th inverter	MOS W/L (μm/μm)	$M_{P3} = 2.8/0.18$ $M_{N3} = 1/0.18$	
4-stage buffer	MOS W/L (μm/μm)	Buffer_1	$M_{PB1} = 9.24/0.18$ $M_{NB1} = 3.3/0.18$
		Buffer_2	$M_{PB2} = 30.8/0.18$ $M_{NB2} = 11/0.18$
		Buffer_3	$M_{PB3} = 101.64/0.18$ $M_{NB3} = 36.3/0.18$
		Buffer_4	$M_{PB4} = 335/0.18$ $M_{NB4} = 118.59/0.18$

the symbol and cross-sectional view of the NMOS with deep N-well (DNW) as decoupling capacitor, where a deep n-well (DNW) layer is used to surround the whole NMOS capacitor.

To verify the effectiveness of different decoupling capacitors on suppressing the power line noise of internal circuits (the ring oscillator of 173-stage inverter chain), four combinations of test circuits are set and listed in Table 2. A baseline test circuit is built with the ring oscillator and the 4-stage buffer only, without any decoupling capacitor between the power lines. The other three test circuits are built by the baseline test circuit with the additional on-chip decoupling capacitors of varactor, NMOS capacitor, and NMOS capacitor with deep N-well (DNW), respectively.

The capacitance of the decoupling capacitors is selected as 5 pF. With the device and process parameters provided by foundry, the simulation results of different types of capacitors in the chip layout are listed in Table 3. The device dimensions of all capacitors and transistors used in test circuits are listed in Table 4, which were designed in a 0.18-μm CMOS process with 1.8-V devices.

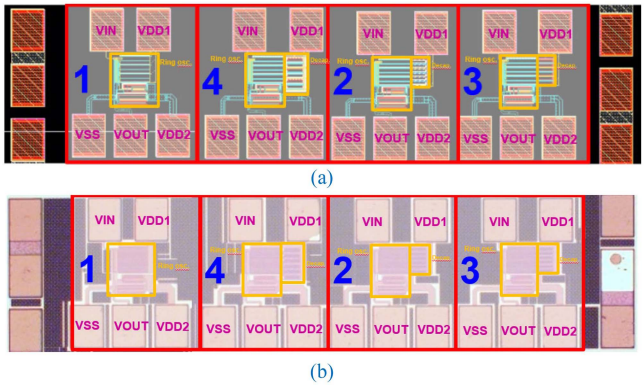

FIGURE 7. The illustrations of (a) layout top view and (b) optical microscope (OM) micrograph of the test circuits in a silicon chip. The numbers on the illustration are corresponding to the symbol numbers of test circuits in Table 2. The additional pad pairs at two sides are specially designed to extend the length of bonding wire for testing with the increased parasitic inductance.

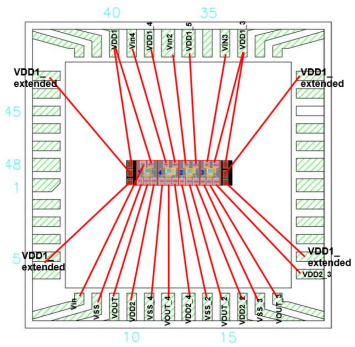

FIGURE 8. Wire bonding plan for the fabricated silicon chip with the test circuits. Bonding two wires in series to the pin of IC to extend the length of bonding wire for testing with increased inductance through the VDD1_extended pin.

IV. EXPERIMENTAL RESULTS AND FAILURE ANALYSIS

The baseline circuit and other three test circuits with different decoupling capacitors have been fabricated in a 0.18-μm 1.8-V CMOS process. The illustration of layout top view and the optical microscope (OM) micrograph of the test chip are shown in Fig. 7. All the test circuits were fabricated in the same die, which was assembled in a 48-pin COB package for function verification and CDM ESD test, as shown in Fig. 8. In addition, the extra two pads in a pair with metal connected between them are placed on the left and right sides of the die. The pad pairs can be bonded with two wires in series between the pin of IC and the lead frame of the package to extend the length of bonding wire for testing with the increased parasitic inductance. After the CDM ESD tests are finished, the standby leakage current and electrical function verification are used to judge whether the device under test (DUT) is passed or failed.

A. FUNCTION VERIFICATION

Before CDM ESD testing, the output functions of all test circuits were verified. In order to verify the effectiveness of

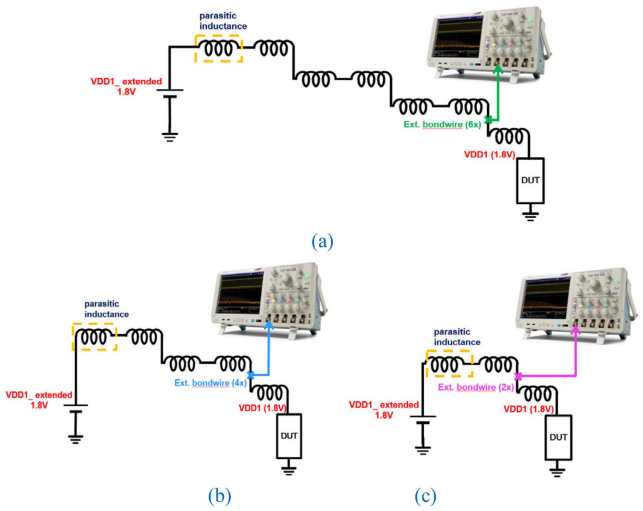

FIGURE 9. Measurement setups for observing the power line noise induced by (a) 6x extending bonding wires, (b) 4x extending bonding wires, and (c) 2x extending bonding wires, through VDD1 pin on IC and VDD1_extended pin on the package.

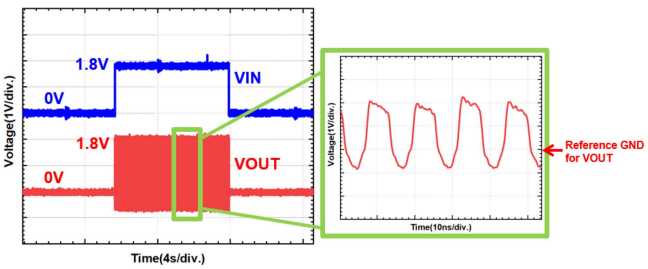

FIGURE 10. Function verification on the fabricated test circuits. The ring oscillator starts to generate the clock-like output waveform (VOUT), when the input signal (VIN) is switched from 0V to 1.8V.

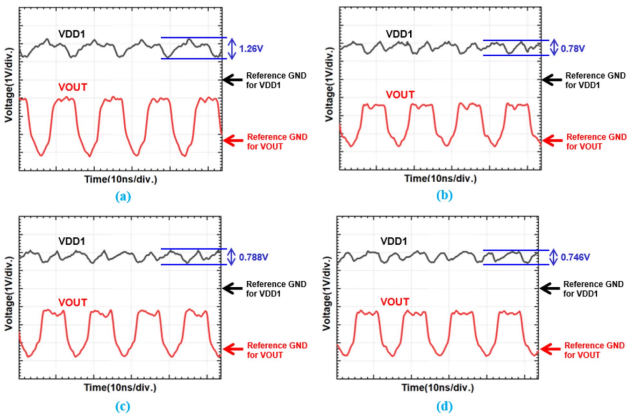

FIGURE 11. The measured voltage waveforms on VDD1 and VOUT of the test circuits (a) without decoupling capacitor, (b) with decoupling capacitor of the varactor, (c) with decoupling capacitor of NMOS, and (d) with decoupling capacitor of NMOS with DNW.

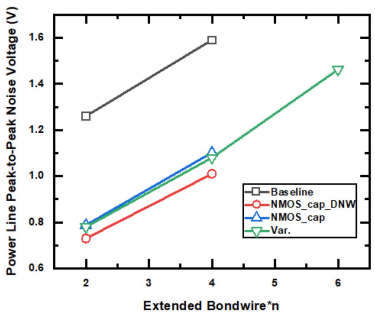

FIGURE 12. Comparisons among the measurement results of four test circuits without or with different decoupling capacitors under different lengths of bonding wires.

the decoupling capacitors, the wire-bonding plan and measure setups for observing the transient/switching noise on the power line are shown in Fig. 9. The oscilloscope (MSO 5104) is connected at the VDD1_extended pin to observe the transient/switching noise that was generated by the ring oscillator of 173-stage inverter chain. To observe the power line noise induced by different lengths of bonding wires, Fig. 9(a) shows the measurement setup for observing the power line noise induced by 6x bonding wires. The measurement setups for observing the power line noise induced by 4x and 2x bonding wires through VDD1 pin on IC and VDD1_extended pin on the package are illustrated in Fig. 9(b) and Fig. 9(c), respectively.

As the measured waveforms shown in Fig. 10, when the VIN pin is given with a logic high signal (1.8V), the ring oscillator starts to oscillate out a clock-like voltage waveform with a frequency of 81 MHz. The transient/switching noise on VDD1 (which supported the 1.8-V power source to the ring oscillator of 173-stage inverter chain) and the VOUT signal are probed and observed with the oscilloscope in Fig. 11 under the package condition of 2x bonding wires. In Fig. 11, the waveforms of power line noises on VDD1 without or with different decoupling capacitors are observed. As seen among Fig. 11(a) (the ring oscillator without decoupling capacitor) and Fig. 11(b)–Fig. 11(d) (the ring oscillators with different decoupling capacitors), the power line peak-to-peak noise voltages on VDD1 in Fig. 11(b)–Fig. 11(d) are indeed reduced, thus the effectiveness of the on-chip decoupling capacitor can be successfully verified. With the presence of decoupling capacitors, the power line peak-to-peak noise voltage is reduced from 1.26V to 0.78V (by varactor), 0.788V (by NMOS capacitor), and 0.746V (by NMOS capacitor with DNW). Among them, the test circuit of a ring oscillator with the decoupling capacitor of NMOS capacitor with DNW has the smallest value of the power line peak-to-peak noise voltage. The measurement results of four test circuits with different lengths of bonding wire are compared in Fig. 12, where the power line peak-to-peak noise voltage is increased as the bonding wire length increasing. The longer the bonding wire is, the larger the value of parasitic inductance, and hence a larger peak-to-peak noise voltage on the power line due to Ldi/dt effect is observed.

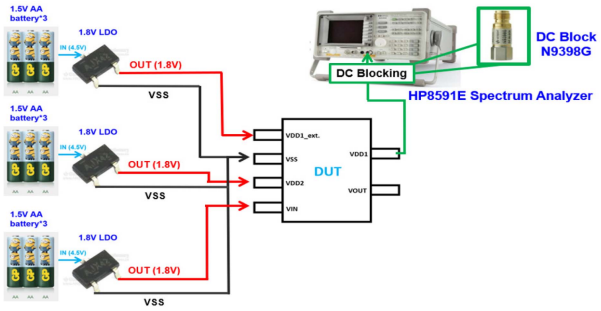

FIGURE 13. The setup to measure the power line noise spectrum by the spectrum analyzer. The DUT is powered by the clean 1.8-V voltage sources those generated from the standalone batteries with 1.8-V LDO regulators. The VDD1 pin is connected through a DC blocking component into the spectrum analyzer to observe the noise spectrum waveform on the VDD1 power line.

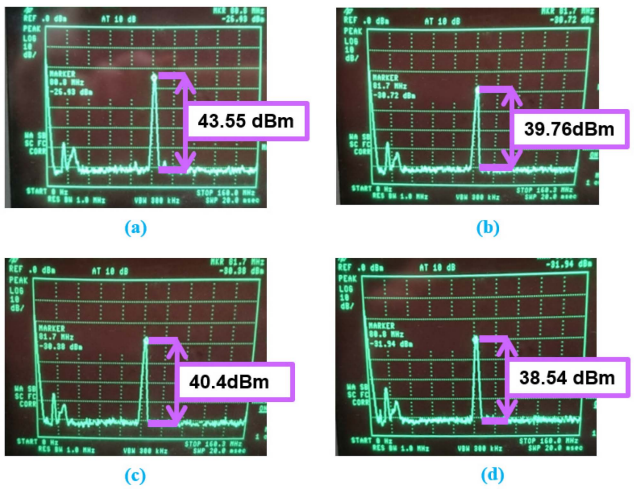

FIGURE 14. The measured spectrum waveforms on the VDD1 power lines of the test circuits, (a) without decoupling capacitor, with decoupling capacitors of (b) varactor, (c) NMOS capacitor, and (d) NMOS capacitor with DNW. The x-axis represents frequency, and the y-axis represents power spectrum. The peak tones of power line noise on VDD1 are all located at 81 MHz.

B. NOISE MEASUREMENT WITH SPECTRUM ANALYZER

The spectrum analyzer (HP8591E) is applied to measure the power line noise spectrum waveform. To fully remove the noise from the machine of switch power supply that was supplied by the external electrical power source of AC 110V, the DUT is powered by the standalone batteries with 1.8-V LDO regulators. Three standalone batteries are connected in series to produce a 4.5-V DC voltage source, which is sent to the input of the LDO to produce a clean output voltage of 1.8V, as the setup shown in Fig. 13. The VDD1 pin of DUT is connected to the signal input of spectrum analyzer with a DC-blocking device (N9398G) to measure the transient/switching noise on VDD1. Between the pins of VDD1_ext. and VDD1, there is the extending bonding wires, as that illustrated in Fig. 9.

The measurement results from the spectrum analyzer are shown in Fig. 14 with the package condition of 2x

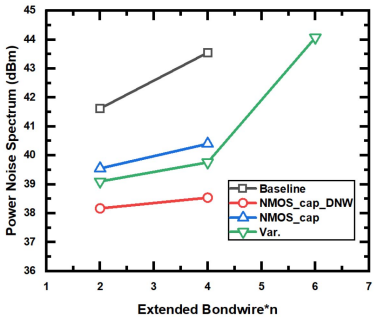

FIGURE 15. Comparisons among the measured power line noise spectrums on the four test circuits without or with different decoupling capacitors under different lengths of bonding wires.

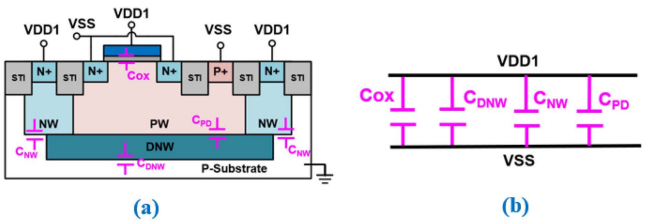

FIGURE 16. (a) The cross-sectional view of the NMOS capacitor with DNW, and (b) the equivalent circuit to show the total capacitance between power lines.

bonding wires. Among Figs. 14(a)–14(d), the x-axis represents frequency and the y-axis represents power spectrum. The peak tones of power line noise observed on VDD1 pins are all located at 81MHz, which is the output frequency of the ring oscillator built with 173-stage inverter chain. The measured power line noise spectrum on the ring oscillator without any decoupling capacitor is 43.55 dBm, as shown ion Fig. 14(a). The noise spectrums on the test circuits of ring oscillators added with decoupling capacitors by varactor, NMOS capacitor, and NMOS capacitor with DNW are 39.76 dBm, 40.4 dBm, and 38.54 dBm, respectively, as shown in Fig. 14(b)–Fig. 14(d). Among the results, the ring oscillator with decoupling capacitor of NMOS capacitor with DNW has the lowest transient/switching noise spectrum on VDD1.

Comparisons among the measured power line noise spectrums on the four test circuits without or with different decoupling capacitors under different lengths of bonding wires are shown in Fig. 15. It is observed that the power line noise spectrum is increased with the increasing length of bonding wires. The longer the bonding wire is, the larger the value of parasitic inductance, and hence a larger noise spectrum on the power line due to Ldi/dt effect is observed.

From the aforementioned experimental results, the ring oscillator with the decoupling capacitor of NMOS capacitor with DNW has a better performance on suppressing power line noise. Fig. 16(a) shows the cross-sectional view of the NMOS capacitor with DNW, where the NMOS capacitor are fully surrounded by the DNW and N-well (NW) layers with the additional parasitic reverse junction capacitance in

TABLE 5. The capacitance of components in decoupling capacitor of NMOS capacitor with DNW.

Component	Capacitance (pF)
C_{OX}	5.0488
C_{NW}	0.0677
C_{DNW}	0.3078
C_{PD}	1.2296

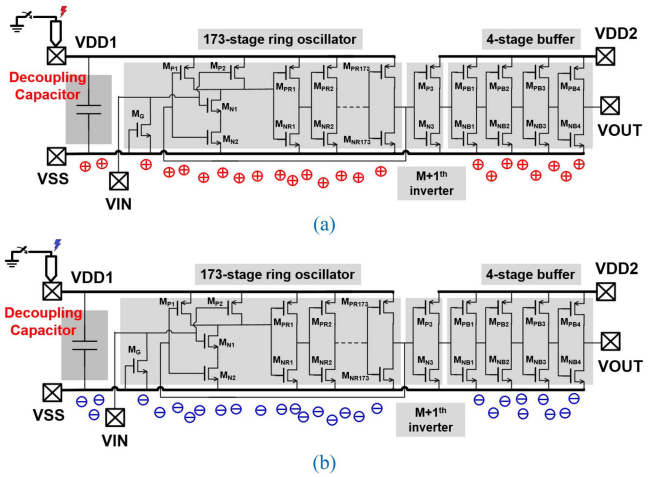

FIGURE 17. Schematic diagrams to illustrate CDM ESD discharging on the VDD1 pin of the test chip under (a) positive, and (b) negative, CDM ESD polarities.

parallel to the original C_{ox}. By sorting out all the capacitive components between the VDD1 and VSS power rails, the equivalent schematic of decoupling capacitor is shown in Fig. 16(b). The total capacitance between VDD1 and VSS is increased from C_{ox} to $C_{ox} + C_{DNW} + C_{NW} + C_{PD}$, where the C_{ox} represents the main capacitance (formed by the gate oxide) in the original NMOS capacitor, C_{DNW} represents the reverse junction capacitor of DNW and P-substrate, C_{NW} represents the reverse junction capacitor of NW and P-substrate, and C_{PD} represents the reverse junction capacitor of P-well (PW) and DNW.

The value of each capacitive component is listed in Table 5, which is calculated with the junction area and the relative process parameters. The C_{PD} component has a larger value than C_{DNW}, because the doping concentration of PW is higher than that of P-substrate. With the parasitic capacitive components added into the total capacitance, the NMOS capacitor with DNW results in a better performance on suppressing power line noise.

C. CDM ESD ROBUSTNESS

The CDM ESD test is performed by pointing the pogo pin to VDD1 pin with both positive and negative polarity stresses. The schematics of CDM ESD discharging with positive and negative polarities are shown in Figs. 17(a) and 17(b), respectively. The CDM ESD tester used in this work is Thermo Scientific Orion3. The failure criterion is defined as

TABLE 6. Zapping condition of CDM ESD testing.

Zap condition	
Zap pin	VDD1
Zap interval	1s
Zap polarity	+/-
Start	125V
End	1kV
Step	125V

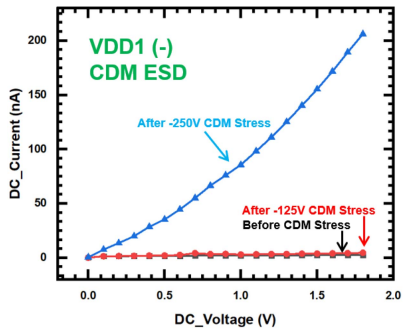

FIGURE 18. DC I-V characteristics on VDD1 of the test circuit with decoupling capacitor of varactor before and after CDM ESD stress.

one of the electrical or function verification results out of specifications.

The CDM test is performed on the fabricated silicon chip with different test circuits (listed in Table 2) inside a 48-pin COB package. The zapping condition of the CDM ESD test is shown in Table 6. For electrical verification, the failure criterion is defined as the I-V curve shifting over 30% from its initial curve, or the leakage current under 1.8-V bias increasing 10 times of magnitude from the initial leakage current before CDM stress. Fig. 18 shows the traced DC I-V characteristic on the test circuit of a ring oscillator with the decoupling capacitor of varactor before and after CDM ESD stress. The I-V curve after CDM stress of −250V shifts significantly, and the leakage current under 1.8-V bias increases over 10 times of magnitude.

For function verification, the failure criterion is defined as the output function after CDM stress is incorrect or deviates from its original output waveform. For example, the measured output waveform of the ring oscillator with the decoupling capacitor of varactor after CDM stress of −250V is shown in Fig. 19. The output waveform has a significant deviation after CDM stress.

All measured results of four test circuits under CDM ESD stress are listed in Table 7, where if the DUT passed 125V qualification but failed at 250V, the CDM level is listed as 125V. The test circuits with decoupling capacitors show worse CDM ESD robustness than that of the baseline design (without decoupling capacitor), except for the ring oscillator with the decoupling capacitor realized by NMOS capacitor with DNW. The decoupling capacitor realized by NMOS capacitor with DNW can sustain higher CDM ESD

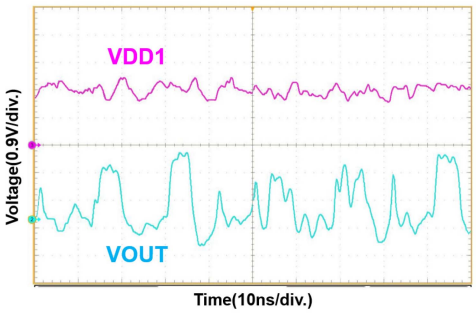

FIGURE 19. The measured voltage waveform of VOUT in the test circuit with decoupling capacitor of varactor after CDM ESD stress of −250V, the output function is incorrect.

TABLE 7. CDM testing results (pass level) of test chip.

Designs		Positive CDM (V)	Negative CDM (V)
(1) Baseline	ring osc. only	Over 1k	Over -1k
(2) Var.	ring osc. + Varactor	125	-125
(3) NMOS_cap	ring osc. + NMOS	250	-250
(4) NMOS_cap_DNW	ring osc. + NMOS w/ DNW (DNW is biased at VDD1)	Over 1k	Over -1k

robustness of over +/1 kV, whereas the decoupling capacitor realized by varactor (NMOS capacitor) can sustain CDM ESD stress of only +/−125V (+/−250V), respectively. In the test circuits, the gate length of the NMOS capacitor is longer than that of the varactor. With a longer channel length, the decoupling capacitor has a larger equivalent series resistance along its ESD discharging path, and thus the discharging peak current would be somewhat reduced to get a higher CDM ESD test result.

From the illustration in Fig. 20(a) under positive CDM stress on VDD1 pin, with the presence of DNW and NW layers surrounding the whole NMOS capacitor, the CDM ESD current can be discharged through the parasitic junction that formed between P-substrate and the DNW to reduce the probability of ESD damage on the thin gate oxide layer of NMOS capacitor. Therefore, it results in higher CDM ESD robustness than that of the other two designs with decoupling capacitors realized by of varactor and NMOS capacitor. The CDM ESD discharging path under negative CDM stress on VDD1 pin was also illustrated in Fig. 20(b). The results of using DNW to improve CDM ESD robustness were ever reported in several prior works [18], [19].

D. FAILURE ANALYSIS

The electrical failure analysis (EFA) is performed with InfraRed Optical Beam Induced Resistance Change (IR-OBIRCH) to locate the failure point. By scanning and heating through the surface of voltage-applied IC with an IR-laser, the position of impedance variation different from other regions has a higher probability to be considered as the abnormal failure point.

As shown in Fig. 21(a) and Fig. 22(a), the failure points are detected and located on the decoupling capacitors realized by NMOS capacitor and varactor, after −500V/+500V

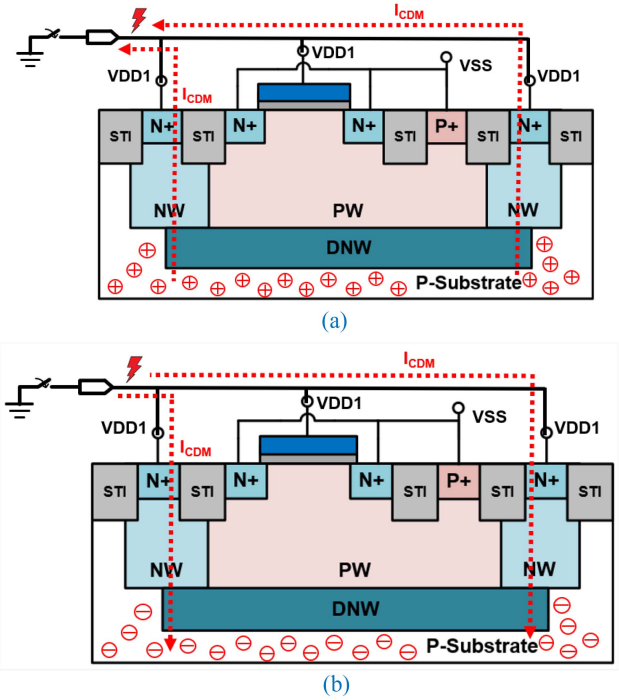

FIGURE 20. Cross-sectional view of the decoupling capacitor realized by NMOS capacitor with DNW during (a) positive, and (b) negative, CDM ESD stressing on VDD1 pin. The CDM ESD current is discharged through the parasitic junction that formed between P-substrate and the DNW to result in a higher CDM ESD robustness.

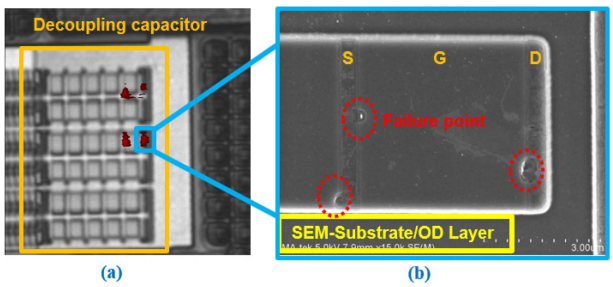

FIGURE 21. Failure analysis results of the ring oscillator with decoupling capacitor of NMOS capacitor. The (a) EFA and (b) SEM results after −500V CDM stress on the VDD1 pin are shown.

CDM stress on VDD1, respectively. The failure spots were observed by IR-OBIRCH, when the test circuits were with 1.8-V bias at VDD1 in the off state of the ring oscillator (VIN=0V). According to the IR-OBIRCH failure locations, the physical failure analysis (PFA), as those shown in Fig. 21(b) and Fig. 22(b), on the decoupling capacitors of NMOS capacitor and varactor is performed with de-layer and Scanning Electron Microscope (SEM), respectively. With the inspection of contact anomalies and poly profile by High Acceleration Voltage (HKV) SEM, it is clearly observed that the failure points are on the gate oxide or on the source/drain edges near to the gate oxide. The source/drain regions of the NMOS capacitor and varactor are directly connected to VSS to form the decoupling capacitor. Such failure locations can

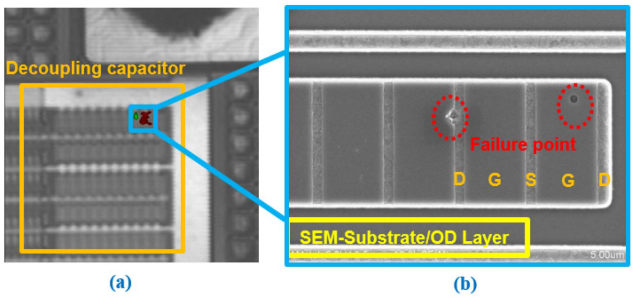

FIGURE 22. Failure analysis results of the ring oscillator with decoupling capacitor of the varactor. The (a) EFA and (b) SEM results after +500V CDM stress on the VDD1 pin are shown.

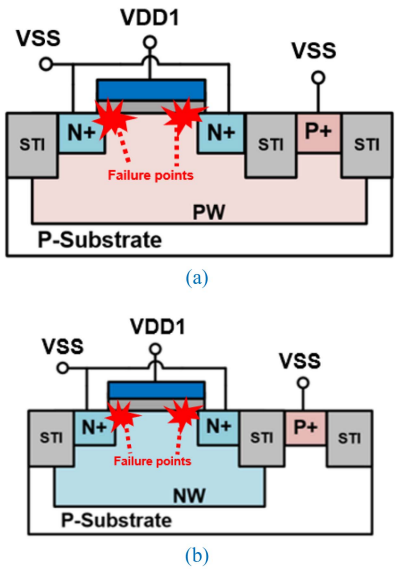

FIGURE 23. Cross-sectional view to illustrate the failure location on the gate oxide of (a) NMOS capacitor and (b) varactor, after the CDM ESD stress.

be confirmed due to the gate oxide breakdown causing by CDM ESD stress, as illustrated in Fig. 23.

V. CONCLUSION

CDM ESD threats on the on-chip decoupling capacitors realized by three different decoupling capacitors have been investigated and verified in silicon chip fabricated by a 0.18-μm CMOS technology. The measured results on the power line transient/switching noises and CDM ESD robustness have revealed that the NMOS capacitor surrounding with DNW is the best solution to realize the decoupling capacitor. In addition, the IR-OBIRCH and the de-layer SEM results showed that the decoupling capacitors realized by varactor or NMOS capacitor are very sensitive to gate oxide damage during CDM ESD stresses. The comprehensive study results of this work can be really benefit and helpful to IC designers on how to optimize the on-chip decoupling capacitors with higher CDM ESD robustness.

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