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Simulation Study of 4H-SiC High-k Pillar MOSFET With Integrated Schottky Barrier Diode

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ABSTRACT A SiC high-k (HK) split-gate (SG) MOSFET is proposed with a Schottky barrier diode (SBD) integrated between the split gates, and is investigated by numerical TCAD simulation. Results show that it has the same breakdown voltage as the SiC high-k (HK) MOSFET with an optimized and practical k value of 30 for its insulation pillar, which results in the highest breakdown voltage (1857 V). The forward voltage (V_F) and reverse recovery charge (Q_{RR}) of the device are 0.9 V and 3.49 $\mu C/cm^2$ respectively, much lower than those of the SiC HK MOSFET due to the SBD. Moreover, lower reverse transfer capacitance (C_{RSS}), smaller gate charge (Q_G), and smaller gate-to-drain charge (Q_{GD}) are achieved for the proposed device because of the split-gates, leading to much lower switching power loss when compared with the SiC HK MOSFET. All these results indicate that the SiC HK SG-MOSFET has promising potential in future power electronics applications.

INDEX TERMS SiC MOSFET, breakdown voltage, high-k dielectric, Schottky barrier diode, split-gate.

I. INTRODUCTION

4H-SiC is a promising semiconductor material for the next-generation power devices in recent years due to its superior characteristics such as wide energy bandgap, high critical electric field, and high thermal conductivity [1]–[3]. SiC power metal-oxide-semiconductor field-effect transistor (MOSFET) is considered to be a potential choice to replace silicon insulated-gate bipolar transistor (IGBT) in many power electronics applications in the future because the performances of silicon power devices are reaching their limits [4]–[9].

Si high-k (HK) pillar MOSFET has been extensively investigated recently because it can effectively overcome the charge imbalance problem and fabrication complexity of super-junction MOSFET by replacing its p-pillar by high-k dielectric material (the gate dielectric is still SiO_2). One of the critical issues for Si HK MOSFET is that the permittivity of the high-k material needs to be extremely high (> 200) [10]–[17]. However, HK MOSFET based on SiC has been rarely studied. The selection of high-k material needs to be considered carefully because SiC HK MOSFET works at much higher voltage than its Si counterpart [16].

In most power electronics systems, a SiC MOSFET is usually connected in parallel with a discrete SiC Schottky barrier diode (SBD) as a freewheeling diode because the inherent PN diode of SiC MOSFET has a high knee voltage (about 2.7 V), resulting in high power loss [18]–[20]. In addition, expansion of stacking faults from basal-plane dislocations (BPDs) also degraded both the forward conduction voltage (V_F) of the body PN diode and the characteristics of SiC MOSFET [21]. In recent years, Sung *et al.* [22]–[24] monolithically integrated a SiC MOSFET and a Schottky barrier diode using a single ohmic/Schottky process scheme, which is beneficial because both devices share the same edge termination and eliminate the parasitic inductance of the diode package, thus reducing chip size and decreasing power loss, respectively. SiC split-gate MOSFET with a merged SBD [25] and SBD-wall-integrated trench MOSFET (SWITCH-MOS) [26], [27] were also proposed to solve this problem. However, integrating SBD into SiC MOSFET without deteriorating its on-resistance (R_{ON}) performance is still challenging.

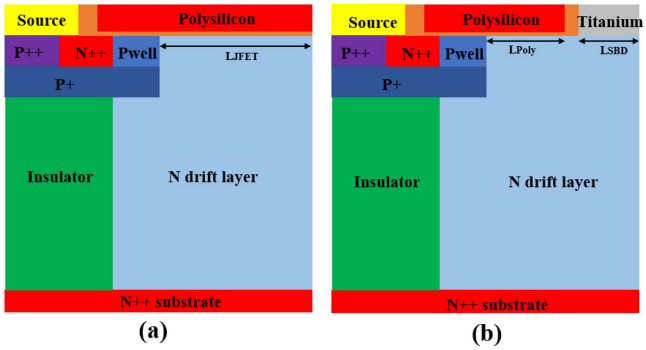

FIGURE 1. Cross-sectional view of (a) SiC HK MOSFET, (b) SiC HK SG-MOSFET.

TABLE 1. Device parameters for simulation.

Parameter	Value
N drift layer doping concentration	1 x 10^{16} cm^{-3}
Pwell region doping concentration	1 x 10^{17} cm^{-3}
N++ region doping concentration	1 x 10^{19} cm^{-3}
N++ substrate doping concentration	1 x 10^{19} cm^{-3}
P++ region doping concentration	1 x 10^{19} cm^{-3}
P+ region doping concentration	3 x 10^{18} cm^{-3}
Channel length	0.5 μm
N++ region width	0.5 μm
N++ region depth	0.3 μm
P++ region width	0.5 μm
P++ region depth	0.3 μm
P+ region width	1.5 μm
P+ region depth	0.7 μm
Insulator pillar width	1.0 μm
Insulator pillar thickness	9.0 μm
JFET width (L_{JFET})	1.0 μm
Overlap width between polysilicon and N drift layer (L_{Poly})	0.65 μm
Schottky contact width (L_{SBD})	0.4 μm
Gate oxide thickness	50 nm
Insulator k value	To be optimized

In this work, a SiC HK MOSFET with integrated SBD is proposed for smaller forward voltage and lower switching loss. Optimization of the k value of the SiC HK MOSFET and performance comparison between SiC HK MOSFET's with/without integrated SBD are discussed in detail with the help of TCAD simulation.

II. DEVICE STRUCTURE AND PARAMETERS

Fig. 1(a) depicts the schematic structure of the SiC HK MOSFET, while Fig. 1(b) shows the proposed SiC HK split-gate (SG) MOSFET. Compared with the SiC HK MOSFET, the SiC HK SG-MOSFET features split gates and a Schottky barrier diode integrated between them. The work function of Schottky barrier metal (titanium) is 4.9 eV [28], and the Schottky metal is shorted to the source contact. Structural parameters of the two devices are listed in Table 1, where all the parameters of the two devices are the same except L_{JFET} and L_{SBD} in the SiC HK SG-MOSFET.

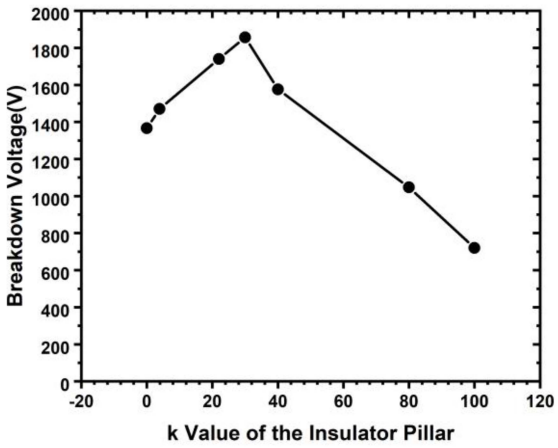

FIGURE 2. Breakdown voltage of the SiC HK MOSFET with different pillar insulators at 300 K.

Two-dimensional device simulations were carried out with SILVACO ATLAS [29]. Physical models including Fermi-Dirac statistics, bandgap narrowing, Shockley-Read-Hall recombination, Auger recombination, incomplete dopant ionization, field-dependent mobility, anisotropic materials properties and impact ionization were implemented. In this work, the interface traps between the gate oxide/insulation pillar and SiC and substrate resistance are ignored. Since the k value of the insulation pillar is an important parameter affecting the breakdown voltage of the SiC HK MOSFET, it will be optimized first in this work.

III. NUMERICAL SIMULATION AND RESULT ANALYSIS

A. OPTIMIZATION OF K VALUE OF THE INSULATION PILLAR

Fig. 2 shows the breakdown characteristics of the SiC HK MOSEFTs with different insulators such as SiO_2 (k = 3.9), HfO_2 (k = 22), TiO_2 (k = 80) and others with k = 0, 30, 40, 100 at 300 K. k = 0 means that the insulation pillar region is replaced by the N drift layer with the same doping concentration, resulting in the conventional SiC vertical double-diffused metal-oxide-semiconductor (VDMOS) transistor [30]. The breakdown voltage is extracted at $I_D = 1$ nA/cm^2. With increasing k value, the breakdown voltage of the SiC HK MOSFET increases firstly, but then decreases. The SiC HK MOSFET with k = 30 has the highest breakdown voltage (1857 V). Consequently, the optimized k value for the SiC HK MOSFET is 30, which is much lower than the optimized value k of 200 (impractical to achieve) for the Si HK MOSFET [16].

The electric field distributions for $V_{DS} = 1000$ V in the SiC HK MOSFET with different insulators are shown in Fig. 3. With increasing k value, the electric field at the interface between the P+ region and the insulation pillar increases according to $\varepsilon_{HK}E_{HK} = \varepsilon_S E_S$ [16], where ε_{HK} and ε_S are the relative permittivities of the high-k insulation pillar and the semiconductor, respectively; E_{HK} and E_S are the electric fields in the high-k insulator and the semiconductor,

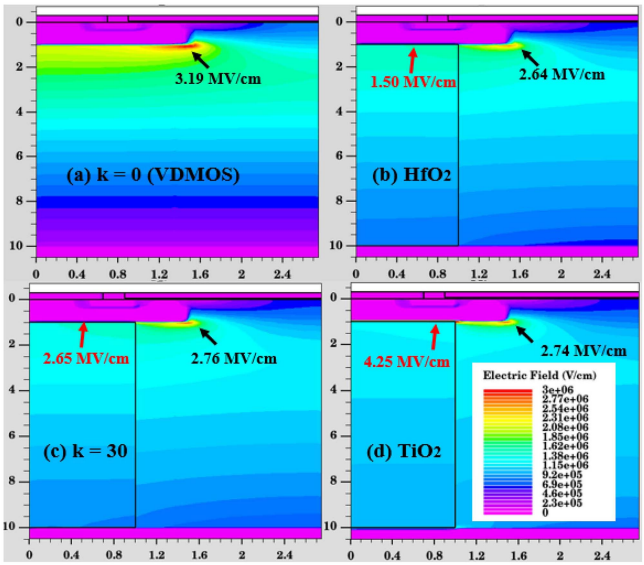

FIGURE 3. Electric field distribution in the SiC HK MOSFET with different pillar insulators at 1000 V and 300 K.

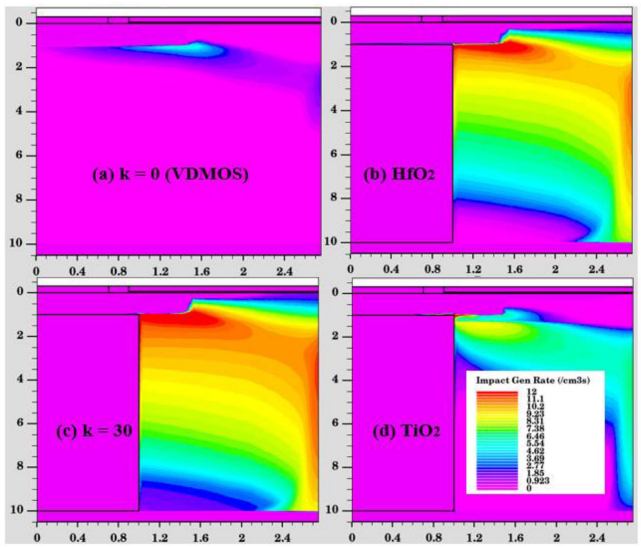

FIGURE 4. Impact generation rate distribution in the SiC HK MOSFETs with different pillar insulators at breakdown voltage and 300 K.

respectively. Under the same doping concentration and same thickness of the N drift layer, the breakdown voltage of SiC MOSFET is 10 times that of silicon MOSFET [3]. In addition, the relative permittivity of silicon (11.9) is close to that of SiC (9.76). Consequently, the electric field in the high-k insulation pillar of the SiC HK MOSFET is about 10 times that in the Si HK MOSFET at breakdown voltage, leading to a weaker reduced surface field (RESURF) effect [16] in the SiC HK MOSFET than in the Si HK MOSFET. Consequently, the optimal k value in the SiC HK MOSFET is lower than that in the silicon counterpart.

Fig. 4 shows the impact generation rate distributions in the SiC HK MOSFETs with different insulators at breakdown voltage. With increasing k value, the electric field at

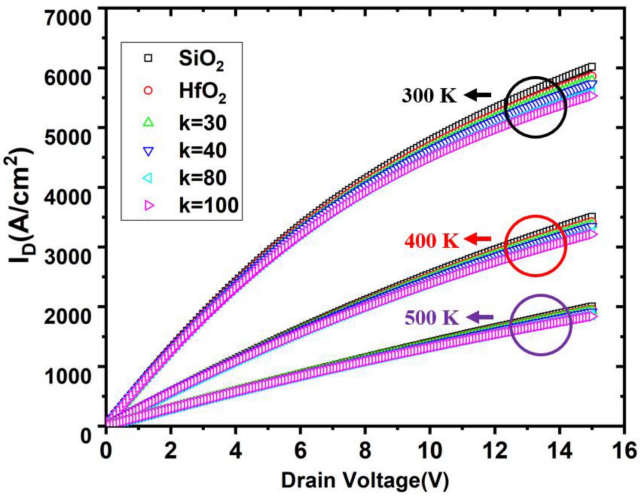

FIGURE 5. Output characteristics of the SiC HK MOSFETs with different pillar insulators at different temperatures.

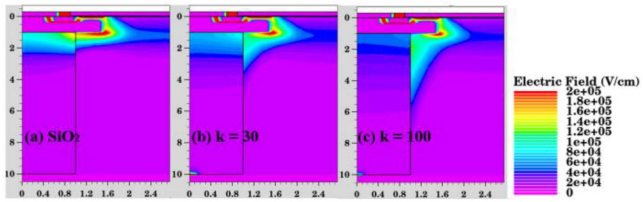

FIGURE 6. Electric field distribution in the SiC HK MOSFETs with different pillar insulators at V_{GS} = 20 V, V_{DS} = 15 V and 300 K.

the interface between the P+ region and the insulation pillar becomes extremely high according to $\varepsilon_{HK}E_{HK} = \varepsilon_S E_S$, thus resulting in premature breakdown. Consequently, the breakdown point moves from near the corners between the P+ region and the JFET region to the interface between the P+ region and the insulation pillar.

The on-state output characteristics of the SiC HK MOSFETs with different insulators are shown in Fig. 5 (without considering the interface-trapped charge). With temperature increasing, the output current decreases due to a reduction in carrier mobility at higher temperature caused by the lattice scattering [31]. With increasing k value, the output current also decreases. To understand this, Fig. 6 shows the electric field distributions in the SiC HK MOSFETs at $V_{GS} = 20$ V, $V_{DS} = 15$ V and 300 K. The electric field in the drift region near the insulator increases with the k value of the insulator due to the RESURF effect [16]. Thus, the electron mobility in the drift region near the insulator decreases due to high electric field as shown in Fig. 7. Consequently, the output current degrades with higher k value for the insulator.

B. CHARACTERISTICS COMPARISON BETWEEN SIC HK MOSFET AND SIC HK SG-MOSFET

For fair comparison, both SiC HK MOSFET and SiC HK SG- MOSFET have the same insulation pillar with

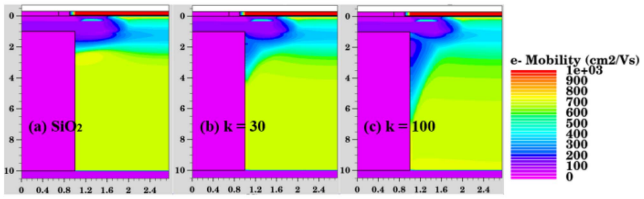

FIGURE 7. Electron mobility distribution in the SiC HK MOSFETs with different pillar insulators at $V_{GS} = 20$ V, $V_{DS} = 15$ V and 300 K.

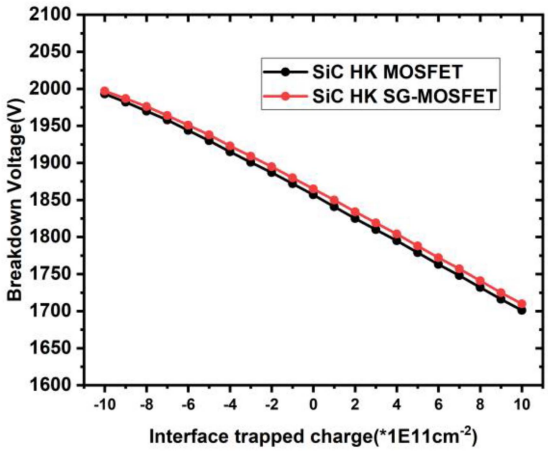

FIGURE 8. Breakdown voltage vs. interface-trapped charge for the SiC HK MOSFET and SiC HK SG-MOSFET at 300 K.

the optimal k value of 30 in the subsequent discussion. The dependences of off-state breakdown characteristics on interface-trapped charge for the two devices ($V_{GS} = 0$ V) at 300 K are shown in Fig. 8.

Under the effect of interface-trapped charge (N_{it}), the effective doping density (N_{eff}) of the drift layer can be defined as $N_{\text{eff}} = N_D + \alpha \frac{N_{it}}{w}$, where N_D is the N drift layer doping density, α the adjust ratio of N_{it} and w the N drift layer width. Consequently, with the interface-trapped charge density changing from -1 x 10^{12} cm^{-2} to 1 x 10^{12} cm^{-2}, the breakdown voltages of the two devices both decreased due to higher effective doping density [32]. Without the interface-trapped charge, the breakdown voltage is 1857 V for the SiC HK MOSFET and 1865 V for the SiC HK SG-MOSFET, indicating that adding a Schottky barrier diode in the SiC HK MOSEFT has little influence on its breakdown characteristics.

The on-state output characteristics ($V_{GS} = 20$ V) of the two devices at different temperatures are shown in Fig. 9 (without considering the interface-trapped charge). The R_{ON} of the SiC HK MOSFET and the SiC HK SG-MOSFET at $I_D = 1$ kA/cm^2 are 1.55 mΩ·cm^2 and 1.77 mΩ·cm^2 respectively at 300 K, 3.60 mΩ·cm^2 and 4.09 mΩ·cm^2 respectively at 400 K, and 7.07 mΩ·cm^2 and 8.04 mΩ·cm^2 respectively at 500 K. At 300 K, the current density distributions of the devices at $V_{GS} = 20$ V, $V_{DS} = 15$ V are shown in Fig. 10,

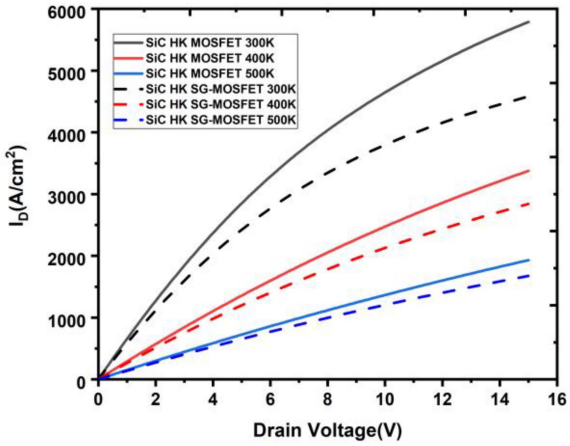

FIGURE 9. Output characteristics of the SiC HK MOSFET and SiC HK SG-MOSFET at different temperatures.

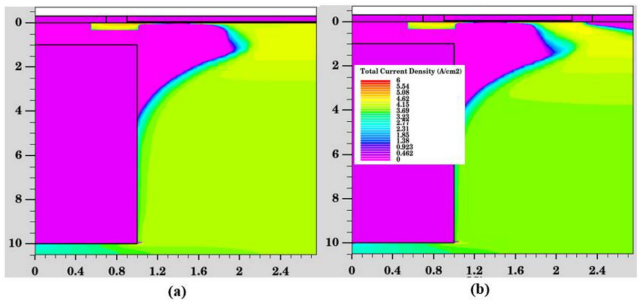

FIGURE 10. Current density distribution at $V_{GS} = 20$ V, $V_{DS} = 15$ V and 300 K for (a) SiC HK MOSFET, and (b) SiC HK SG-MOSFET.

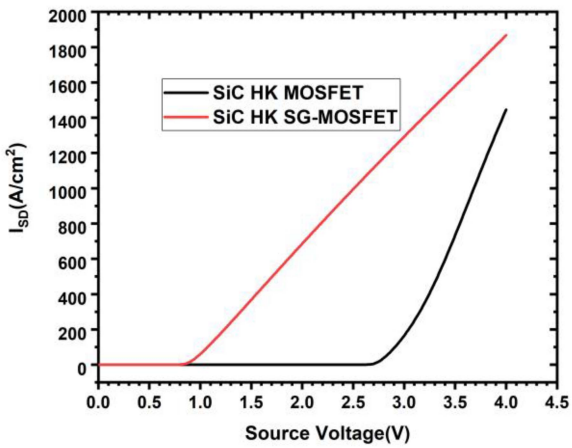

FIGURE 11. Reverse conduction characteristics of the SiC HK MOSFET and SiC HK SG-MOSFET.

demonstrating that the current density at the Schottky contact area is reduced, thus increasing the R_{ON} of the SiC HK SG-MOSFET.

If not specified, all the simulations are without interface-trapped charge and at 300 K in the subsequent discussions. Fig. 11 depicts the reverse conduction characteristics of the MOSFETs. The forward voltage (V_F) of the SiC HK

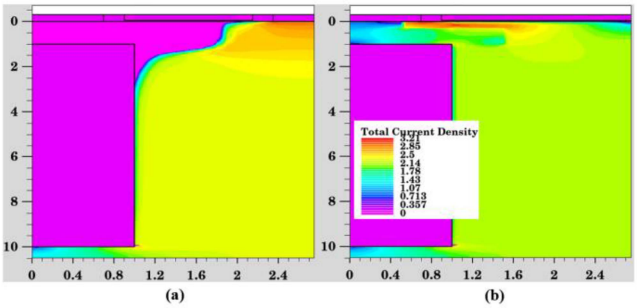

FIGURE 12. Current density distribution at $I_S = 100$ A/cm^2 for (a) SiC HK MOSFET, and (b) SiC HK SG-MOSFET.

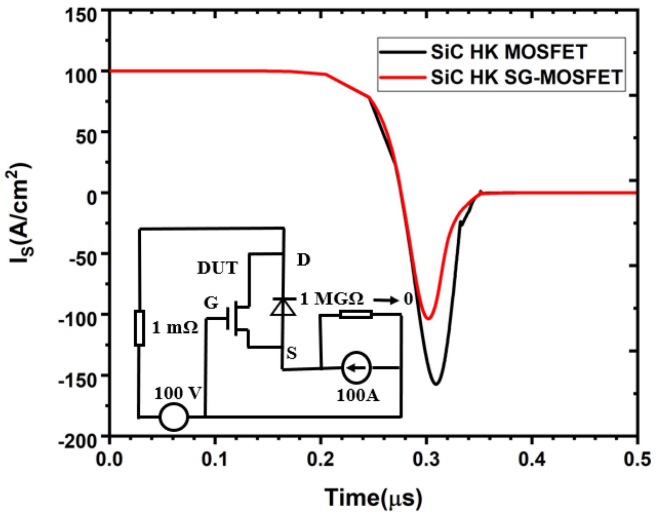

FIGURE 13. Reverse recovery characteristics of the SiC HK MOSFET and SiC HK SG-MOSFET. Inset: test circuit.

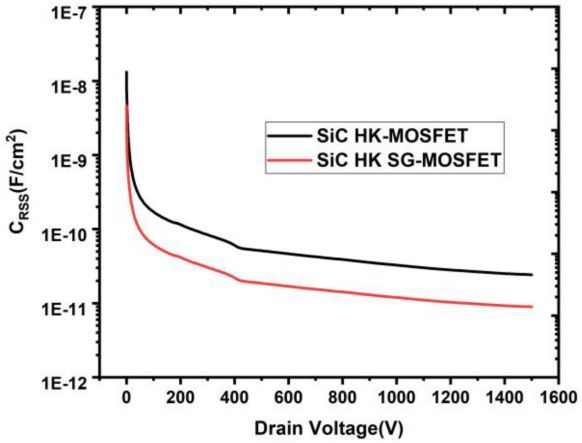

FIGURE 14. Reverse transfer capacitances (C_{RSS}) of the SiC HK MOSFET and SiC HK SG-MOSFET at $V_{GS} = 0$ V.

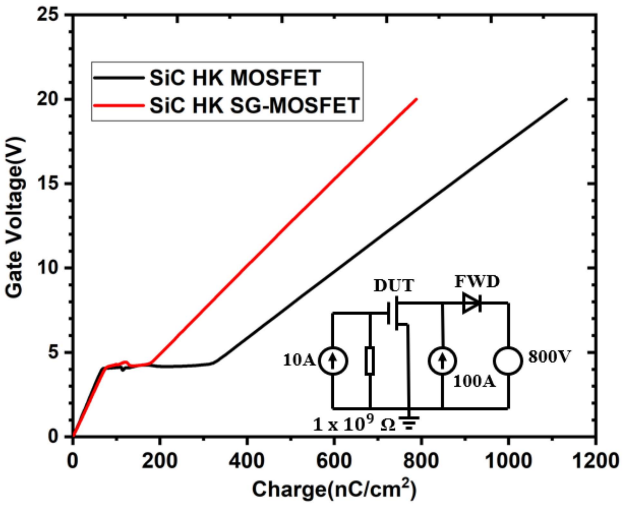

FIGURE 15. Gate-charge characteristics of the SiC HK MOSFET and SiC HK SG-MOSFET. Inset: test circuit.

MOSFET is 2.7 V, while that of the SiC HK SG-MOSFET (0.9 V) is much lower due to the Schottky barrier diode between the split gates.

The current density distributions in the SiC HK MOSFET and SiC HK SG-MOSFET at a source current (I_S) of 100 A/cm^2 are shown in Fig. 12. The inherent PN junction in the SiC HK SG-MOSFET is inactivated because V_F is decreased to 0.9 V.

The MIXEDMODE [29] tool in ATLAS was utilized to investigate the reverse recovery characteristics of the devices. The chip area of the device under test (DUT) was set to be 1 cm^2. The simulation results are plotted in Fig. 13 with the test circuit shown in its inset. The reverse recovery time (t_{RR}) and peak reverse recovery current (I_{RMM}) for the SiC HK MOSFET and the SiC HK SG-MOSFET are 61.2 ns and 59.9 ns, 157.3 A/cm^2 and 103.6 A/cm^2, respectively. The reverse recovery charge (Q_{RR}) for the SiC HK MOSFET and SiC HK SG-MOSFET is 5.76 μC/cm^2 and 3.49 μC/cm^2, respectively. Consequently, compared with the SiC HK MOSFET, the I_{RMM} and Q_{RR} of the SiC HK SG-MOSFET are reduced by 34.1 % and 39.4 %, respectively, due to the Schottky contact in the SiC HK SG-MOSFET.

Fig. 14 shows the reverse transfer capacitances ($C_{RSS} = C_{GD}$) of the SiC HK MOSFET and SiC HK SG-MOSFET at $V_{GS} = 0$ V. The amplitude and frequency of ac signal are set to 10 mV and 1 MHz to extract the capacitance in this work [33]. Owing to the smaller overlap between the polysilicon gate and the JFET region in the SiC HK SG-MOSFET than in the SiC HK MOSFET, the extracted C_{RSS} at $V_{DS} = 800$ V is 14.2 pF/cm^2 for the SiC HK SG-MOSFET, 63.6 % lower than that of the SiC HK MOSFET (39.0 pF/cm^2). Lower C_{RSS} helps decrease the switching power loss of the MOSFET [34], [35].

The gate-charge curves of the two MOSFETs are shown in Fig. 15. The supply voltage V_{DD} is 800 V, usually used for devices with BV under 2000 V. The area of the DUT is set to be 1 cm^2. A constant current of 10 A is used to charge the gate electrode. The gate charge (Q_G) and gate-to-drain charge (Q_{GD}) of the SiC HK MOSFET are 1132 nC/cm^2 and 207 nC/cm^2, respectively, while those of

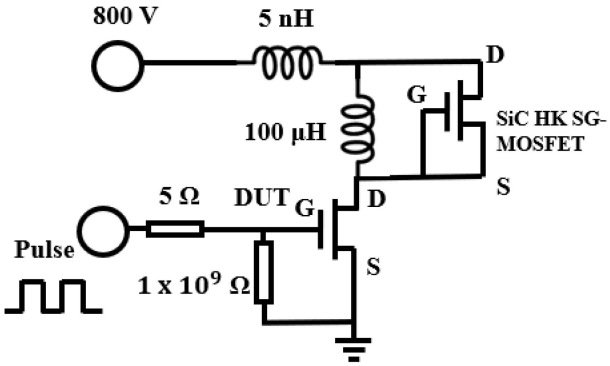

FIGURE 16. Test circuit for switching performance of the SiC HK MOSFET and SiC HK SG-MOSFET.

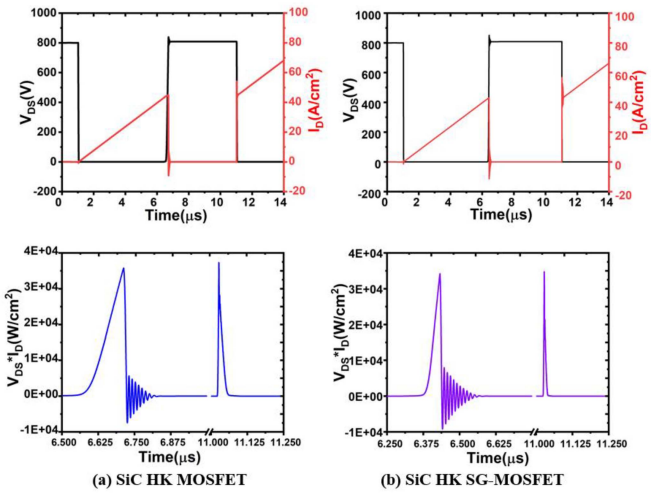

FIGURE 17. Switching waveforms for the SiC HK MOSFET and SiC HK SG-MOSFET.

the SiC HK SG-MOSFET are 788 nC/cm^2 and 108 nC/cm^2, respectively, reduced by 30.4 % and 47.8 %, respectively due to lower C_{GD}. Consequently, the SiC HK SG-MOSFET features a Baliga figure of merit (FoM) $Q_G \cdot R_{ON}$ and $Q_{GD} \cdot R_{ON}$ reduced by 20.5 % and 40.4 %, respectively.

The switching performances of the MOSFETs are studied by using a double-pulse test as shown in Fig. 16. The area of the DUT is set at 1 cm^2. The integrated Schottky barrier diode in the SiC HK SG-MOSFET is used as the freewheeling diode (FWD) and the area of the SiC HK SG-MOSFET is set at 0.01 cm^2. The supply voltage V_{DD} is 800 V. The load inductance and the parasitic stray inductance are 100 μH and 5 nH, respectively. The gate resistance is 5 Ω. The gate voltage pulse switching between 0 V and 20 V is used to define the device between off-state and on-state. The switching frequency is 100 kHz, and a duty circle of 0.5 is assumed. The rise time and fall time of the gate signal are set as 10 ns.

Fig. 17 shows the switching waveforms of the MOSFETs.

The turn-on energy loss (E_{ON}) and turn-off energy loss (E_{OFF}) of the SiC HK MOSFET are 0.46 mJ/cm^2 and 2.58 mJ/cm^2, respectively, while those of the SiC HK SG-MOSFET are 0.18 mJ/cm^2 and 1.18 mJ/cm^2, reduced by 60.9 % and 54.3 %, respectively due to lower C_{RSS} [34], [35].

TABLE 2. Comparison between the studied MOSFETs (at 300 k).

	SiC HK MOSFET	SiC HK SG-MOSFET
V_F	2.7 V	0.9 V
BV	1857 V	1865 V
R_{ON}	1.55 mΩ·cm^2	1.77 mΩ·cm^2
I_{RMM}	157 A/cm^2	103 A/cm^2
t_{RR}	61.2 ns	59.9 ns
Q_{RR}	5.76 μC/cm^2	3.49 μC/cm^2
C_{RSS}	39.0 pF/cm^2	14.2 pF/cm^2
Q_G	1132 nC/cm^2	788 nC/cm^2
Q_{GD}	207 nC/cm^2	108 nC/cm^2
$Q_G \cdot R_{ON}$	1755 mΩ·nC	1395 mΩ·nC
$Q_{GD} \cdot R_{ON}$	321 mΩ·nC	191 mΩ·nC
E_{ON}	0.46 mJ/cm^2	0.18 mJ/cm^2
E_{OFF}	2.58 mJ/cm^2	1.18 mJ/cm^2

*t_{RR} and Q_{RR} are measured at I_S = 100 A/cm^2
C_{RSS} is measured at V_{DS} = 800 V

IV. CONCLUSION

In this work, the k value of the insulation pillar in the SiC HK MOSFET is firstly optimized for maximum device breakdown voltage by TCAD simulation. The optimal k value (30) for the MOSFET is more practical than the very high value (200) for its Si counterpart. La_2O_3 and $LaAlO_3$ [36], LaTiO [37] and HfTiO [38] can be the potential high-k material candidates. By magnetron sputtering or atomic layer deposition, the high-k material can be deposited to fill up the trench [38], [39]. Then, the device is integrated with a Schottky barrier diode to form a new device - SiC HK SG-MOSFET. Compared with the SiC HK MOSFET, the proposed device demonstrates the same breakdown voltage, much smaller V_F, better reverse recovery performance and lower switching loss, with little R_{ON} degradation. Therefore, the proposed SiC HK SG-MOSFET could be a promising and competitive candidate for power electronics applications in the future.

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