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No-Snapback LDMOS Using Adaptive RESURF and Hybrid Source for Ideal SOA

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ABSTRACT A simple modification to the lateral DMOS is demonstrated, enabling a significant extension to the electrical safe operating region. This approach uses a novel Hybrid Source to suppress the parasitic bipolar, prevent snapback and enable operation at high drain voltage & current regions that have traditionally been inaccessible due to triggering of the parasitic bipolar. Trigger currents exceeding 10x that of conventional PN source devices under grounded gate, very fast TLP conditions have been achieved. This improvement does not compromise the basic DC parameters, such as specific on-resistance or breakdown voltage. This paper covers the device architecture, formation of the Hybrid Source, electrical performance, TCAD simulation and discussion of the mechanisms behind this new device and the improvements it enables.

INDEX TERMS Lateral double-diffused MOSFET (LDMOS), electrostatic discharge (ESD), safe operating area (SOA), bipolar junction transistor (BJT), robustness, ruggedness.

I. INTRODUCTION

LDMOS transistors have become dominant in power management IC applications due to good electrical performance and ease of integration. All LDMOS transistors contain an undesired, parasitic bipolar junction transistor (BJT) [1] that has a negative effect on the host LDMOS. At high drain voltages, the BJT is prone to parasitic turn-on, which places an electrical limitation on the range of operable bias conditions.

Efforts have been made over the decades to suppress the impact of the parasitic bipolar, which usually involved the use of a highly doped body to reduce the BJT base resistance and delay the triggering of the BJT [1], [2], [3].

An alternative, novel approach is to utilize a Hybrid Source LDMOS architecture to provide unparalleled bipolar suppression. First introduced at ISPSD 2020 [4], this concept has been proven as not only a viable substitute for the highly doped body, but an even better complementary ESD solution when used together.

This work greatly expands beyond the initial results of the Hybrid Source LDMOS [4]. An improved overall architecture is presented to further enhance the performance, culminating in more than tenfold improvement of the BJT trigger current at grounded gate conditions. This improved Hybrid Source LDMOS device architecture has been implemented on an existing 0.18μm BCD on SOI Automotive Process [5]. In addition to demonstrating performance improvement, supplementary insight into the creation of the Hybrid Source and its underlying mechanisms is provided.

II. HYBRID SOURCE LDMOS

A. BACKGROUND AND DEVICE

Traditionally, Schottky Barrier MOS Transistors have been associated with low voltages and deep sub-micron integration. Research in the 1990s and early 2000s focused

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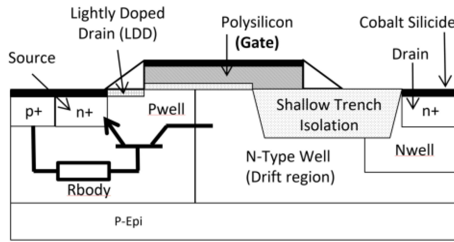

FIGURE 1. Traditional LDMOS and parasitic BJT.

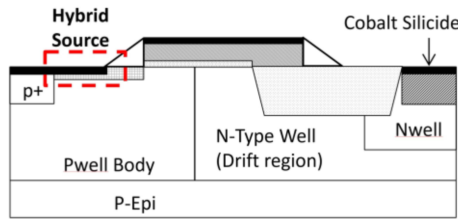

FIGURE 2. Hybrid Source LDMOS.

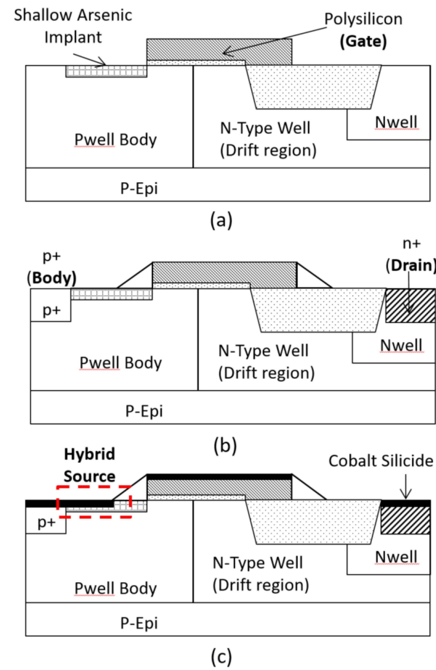

FIGURE 3. Process flow for the Hybrid Source. (a) Self-aligned shallow arsenic implantation (b) Gate sidewall formation and n-type/p-type diffusions (c) Cobalt silicidation to form the Hybrid Source junctions.

on utilizing the Schottky junction to address the challenges of ever smaller transistors [6]. Much of this research went into addressing the fundamental problem with Schottky junctions - high metal-semiconductor barrier height, which limited drive currents. Solutions to this included exotic silicide materials [7] and dopant segregation to modulate the barrier height [8]. Such approaches were increasingly successful [6], but the Schottky Barrier MOS approach never really gained traction in the deep sub-micron arena.

Schottky junction application in power transistors has been sporadic, and thus far have not been used for the purpose of improving the electrical Safe Operating Area (e-SOA). In LDMOS transistors, the e-SOA is limited by triggering of the parasitic BJT, Fig. 1, at high drain voltages. This leads to snapback and ultimately destruction of the device. If this BJT can be suppressed, a higher drain voltage can be sustained and the electrical Safe Operating Area (e-SOA) extended.

Traditionally, suppression of the BJT has been attempted through the use of a highly doped body region [1]–[3]. This reduces the well resistance. Thus, a smaller base-emitter voltage is attained in response to hole flow from the drain-body breakdown and triggering of the BJT is postponed. An alternative method is to use a Hybrid Source [4], Fig. 2. The Hybrid Source is formed between the cobalt silicide metallization and the underlying silicon.

In substituting the conventional PN source with a Hybrid Source, the electron injection efficiency of the source is degraded, which reduces the gain of the parasitic BJT and in turn improves the e-SOA. However, it is not sufficient to merely create a metal/semiconductor source, as the same poor electron injection that is beneficial for parasitic BJT suppression is detrimental to LDMOS drive current and on-resistance. To retain low on-resistance, a self-aligned, shallow arsenic implant is used in conjunction with the silicidation to create a Hybrid Source junction with quite distinct vertical and lateral attributes. Vertically, there exists a dopant segregated rectifying Schottky junction. Laterally, the implanted arsenic creates an ohmic junction between the silicide and the channel region, enabling high drive currents. Such a Hybrid junction is optimal for LDMOS operation, retaining low on-resistance while suppressing the parasitic BJT.

One further key aspect of this revised Hybrid Source LDMOS architecture is the addition of an adaptive drain NWELL, which encloses the drain n+ active region. This adaptive drain NWELL does not require any additional masks as it is shared with the low voltage PMOS transistor in this technology. As such, it is formed simultaneously with the body of the low voltage PMOS transistor. The purpose of this additional well is to mitigate the high electric field that forms at the edge of the drain active region when the space charge in the drift region is compensated by electrons injected from the channel and therefore the space charge region boundary moves to the drain active edge. The benefit of this on the e-SOA have been described elsewhere [9] and this change has been instrumental in the improved performance compared to the first Schottky LDMOS results [4]. The physical mechanisms behind this will be discussed later in Section V. The combination of the adaptive drain region, the Hybrid Source, optimal body and drift region design enable electrical operation at high trigger currents and voltages across all gate bias conditions.

B. HYBRID SOURCE LDMOS PROCESS FLOW

The integration-friendly implementation of the Hybrid Source to these devices is shown in Fig. 3. All front

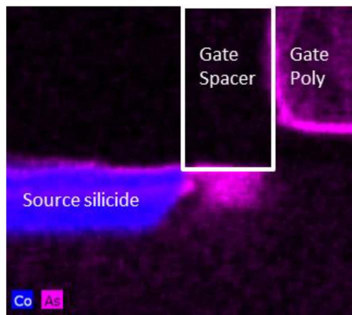

FIGURE 4. Resultant Hybrid Source junction.

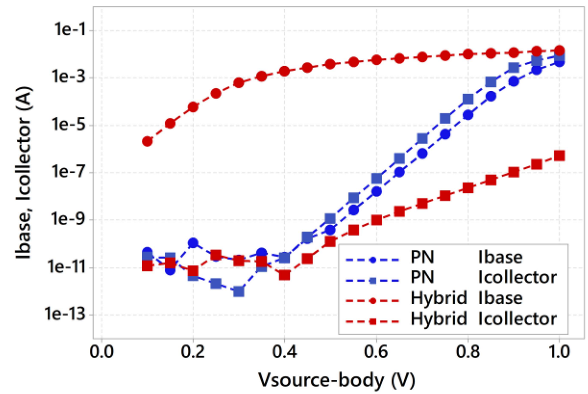

FIGURE 5. 70V LDMOS parasitic BJT body/drain current.

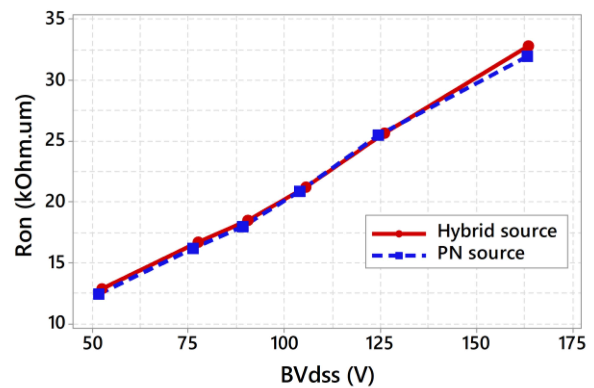

FIGURE 6. BDS/On-Resistance for 40V to 125V Hybrid and PN source LDMOS.

end of line (FEOL) processing is the same as the donor devices, including DTI, STI, well implants, gate oxidation and polysilicon deposition. The process flow only diverges after etching the polysilicon gate. At this point, an ultra-shallow, high dose arsenic implantation is performed which is self aligned to the polysilicon, Fig. 3a. The projected implant energy is selected to be less than the depth of the source silicide. The purpose of this implant is to modulate the barrier height of the Schottky junction to optimize the tradeoff between channel current and BJT suppression. The gate sidewall formation is then performed, using conventional oxide/silicon nitride/oxide deposition and etch and n-type/p-type implantation is performed to contact the drain and body regions of the device, Fig. 3b. Finally, cobalt silicidation is formed at the source, gate and drain regions, Fig. 3c.

This process flow results in a Hybrid Source as indicated by the Energy Dispersive X-Ray Spectroscopy (EDS) result of Fig. 4, a vertical Schottky junction to the body and a lateral ohmic connection to the channel region.

III. DC PERFORMANCE

A. PARASITIC BJT

Since the intention is to improve the electrical SOA, characterization of the lateral BJT was also performed using a dedicated separate source-bulk structure. The emitter-base (source-body of the BJT, Fig. 1) junction was forward biased and the terminal currents measured, Fig. 5. The body current flows across the forward biased source-body junction, and here a clear differentiation between the PN source reference and Hybrid Source device can be seen, as would be expected given the lower turn-on voltage of the Schottky diode. The collector (drain) current is several decades lower for the Hybrid Source LDMOS. When the base-emitter junction is forward biased to 1V, the Hybrid Source LDMOS collector (drain) current is 4 decades lower than the conventional PN source LDMOS. This is indicative that the source is not injecting electrons to be transported to the collector – poor injection efficiency [10], as would be expected from a majority carrier Schottky junction [11].

Such Schottky junction suppression of the parasitic BJT has been reported for low voltage transistors [12]. The significance of this finding for power transistors is the impact on the electrical operating region where the BJT contributes to curtailment of the LDMOS e-SOA.

B. LDMOS

The standard power transistor metrics of on-resistance and breakdown voltage across a range of drift lengths covering the operational voltage nodes, 40V to 125V, is shown in Fig. 6. From the overlapping PN source and Hybrid Source results, we can see that the Hybrid Source can be introduced without compromising the basic DC metrics.

IV. TRANSMISSION LINE PULSE PERFORMANCE

Transmission Line Pulse (TLP) measurements were used to determine the electrical Safe Operating Area (e-SOA) of the device. These were conducted using a HPPI TLP-3010C. Fixed voltages of 0V, 5V and 7V were applied to the gate and rectangular current pulses applied at the drain with pulse widths of 2.5ns and 100ns. The pulse rise times were 100ps and 5ns respectively. Following the pulsed drain current measurement, a DC leakage measurement, Ileak, is performed to observe degradation and ultimately destruction of the device. The TLP measurement for each gate voltage ceases when leakage current exceeds 1μA. Both pulsed drain voltage/current and DC leakage are shown for all the TLP results in this section.

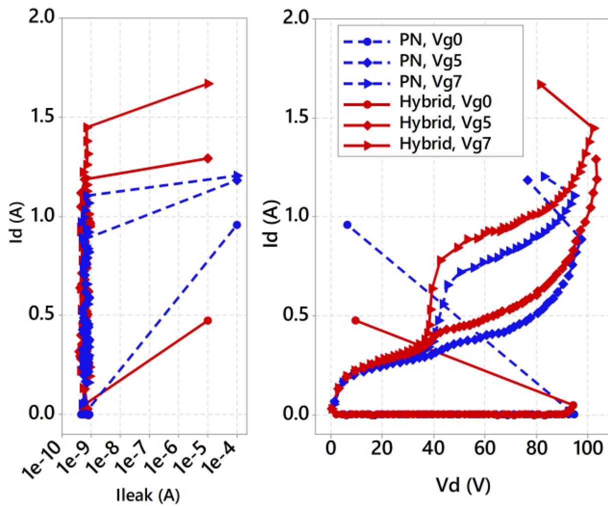

FIGURE 7. Comparison of 70V Hybrid Source LDMOS and conventional 70V PN source LDMOS, 100ns TLP, W = 80µm, NF = 16.

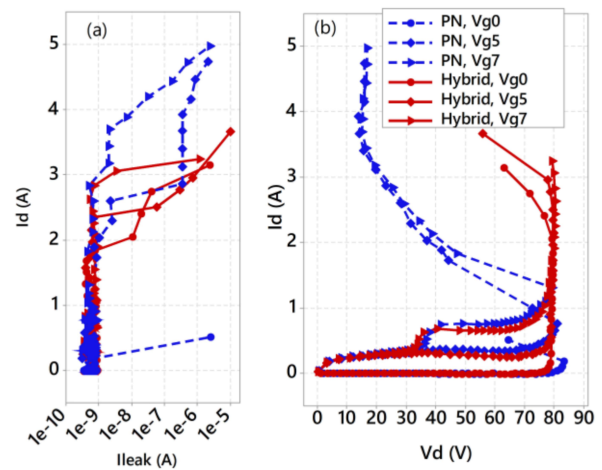

FIGURE 8. Comparison of 70V Hybrid Source LDMOS and 70V PN source LDMOS drain current and leakage, 2.5ns pulse width, W = 80µm, NF = 16.

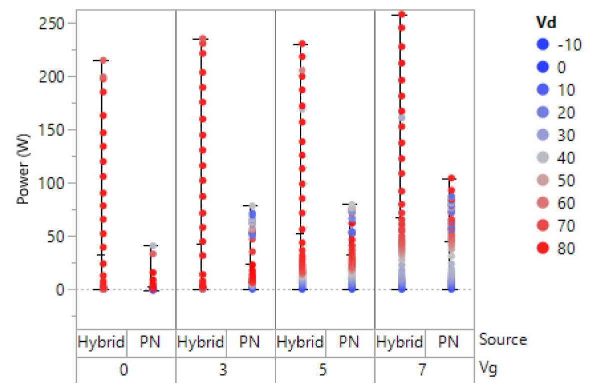

FIGURE 9. Power to failure for the PN source LDMOS and the Hybrid Source LDMOS at 2.5ns pulse width.

A. 100NS MEASUREMENT AND RESULTS

The 100ns Transmission Line Pulse results (TLP) for the 70V Hybrid Source LDMOS are shown as Fig. 7. A modest improvement is noted compared to the conventional PN source LDMOS under high gate voltage with the trigger voltage and trigger current being 7.6% and 30% higher respectively.

B. 2.5NS MEASUREMENT AND RESULTS

At 2.5ns pulse width, the conventional PN source LDMOS snaps back at the trigger voltage to the holding voltage, before the current increases to It2 and the device fails, Fig. 8, a text book response [13]. In contrast, the Hybrid Source LDMOS takes a completely different IV trajectory. With the Schottky junction suppression of the parasitic BJT, no snapback is seen and the avalanche current of the drain-bulk junction continues to increase until thermal destruction of the device. At grounded gate condition, the conventional PN source has a low failure current, 0.18A(0.14mA/um). The conventional PN source LDMOS snaps back to a holding voltage of around 13V for Vg = 5V and Vg = 7V. En-route to this holding voltage, device degradation has already set in as indicated by increased device leakage when the TLP drain currents exceed 2A.

For the Hybrid Source LDMOS, under grounded gate conditions, drain currents of around 2A (1.5mA/um) are possible before the onset of leakage. This is more than 10x that seen for the PN source LDMOS. At higher gate voltages, the trigger voltage sees no reduction, a square SOA is maintained and no snapback is observed. This could be advantageous for protection by a parallel ESD clamp. For short ESD pulse rise times, a short residual voltage and current spike can occur in the HVMOS device due to the limited triggering speed of the ESD clamp, e.g., system-level ESD (IEC 61000-4-2) pulses. Here, a device with Hybrid Source could take over the spike originating from the first short high current peak in non-snapback mode and survive, while with a PN source the parasitic BJT would trigger, resulting in deep snapback and destruction by the subsequent much longer main current peak. The high 2.5ns TLP current capability of the Hybrid Source LDMOS would also facilitate ESD protection against the fast and short CDM (Charged Device Model) pulses which for typically required protection levels have much higher peak currents than those typically required for tests with the slower and longer HBM (Human Body Model) pulses. This is in contrast to the PN source LDMOS where the current capability is not significantly higher for 2.5ns than for 100ns pulse width and thus a larger device width would be required to pass the CDM target peak current than for HBM.

While the failure currents, It2, are similar for both the PN source and Hybrid Source LDMOS, the drain voltage under which this happens is significantly different. For this reason it is useful to compare the power-to-failure metric [14], Vd * Id, as shown in Fig. 9. Prior to the leakage exceeding 1uA, the defined failure leakage, the Hybrid Source LDMOS power is 2x to 4x that of the PN source LDMOS, depending on the applied gate bias condition. From this

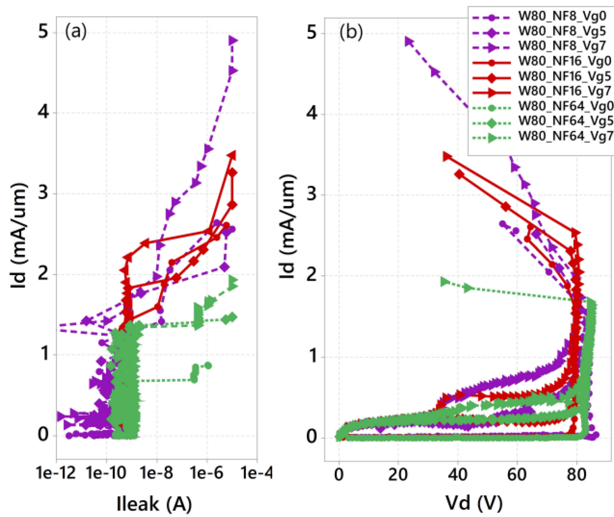

FIGURE 10. 2.5ns TLP results for three different geometries with 8, 16 and 64 fingers. Wfinger = 80μm.

metric, the Hybrid Source LDMOS appears much more robust.

Generally, the failure current does not scale with device width for conventional LDMOS [17]. This is because the current at failure is not uniformly distributed across the entire width of the device, but rather is limited to a narrow current filament. The reader is referred to Shrivastava [18] for a detailed description of how such current filaments develop and the mechanisms underpinning it.

One of the key mechanisms is the localized triggering of the parasitic bipolar. Since the Hybrid Source suppresses the parasitic BJT, it is worth revisiting the conventional wisdom regarding failure current scalability. Fig. 10 shows the 2.5ns TLP and leakage results for three different sized devices, with 8, 16 and 64 fingers. Each finger is 80um wide, so the total widths are 640μm, 1280μm and 5120μm. The drain current is normalized to milliamps per micron of the device width. Referring to the DC leakage, Fig. 10a, one can observe the onset of degradation for TLP pulses mostly in the range 1.5mA···2.5mA. Given the biggest structure total width is 8x that of the smallest, this indicates there is scaling of the failure current with the device width under these 2.5ns very fast pulse conditions. The rate of Ileak degradation is a function of the device geometry.

When the device reaches thermal breakdown with the local temperature exceeding the intrinsic temperature, somewhere in the device the ensuing negative differential resistance leads to formation of a current filament where all the drain current will go through. For a device with large width this drain current is large, resulting in significant damage and a consequential step increase in leakage while for a small device this current is smaller and thus the amount of damage and leakage current gradually increases with increasing TLP current.

V. TCAD SIMULATION

TCAD simulation was conducted under TLP conditions to further understand the mechanisms behind the improved

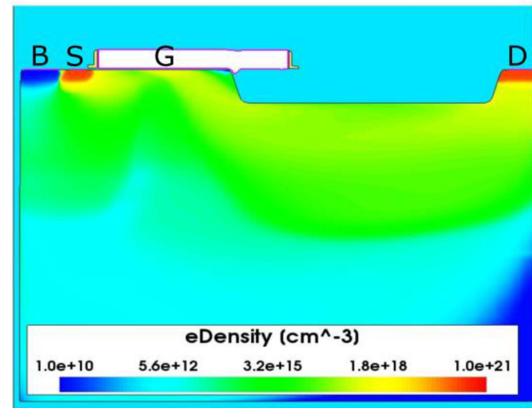

FIGURE 11. Electron concentration for the PN source LDMOS Vgs = 5V, Id = 1.1mA/um, 100ns pulse.

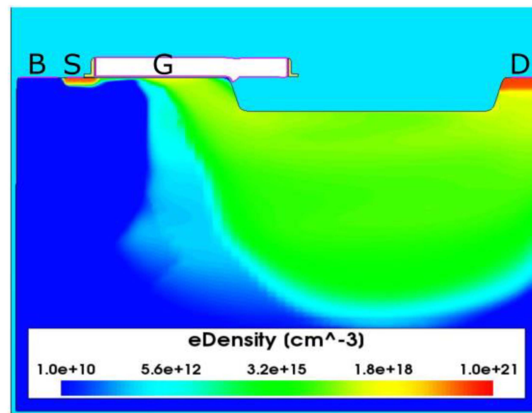

FIGURE 12. Electron concentration for the Hybrid Source LDMOS Vgs = 5V, Id = 1.1mA/um, 100ns pulse.

Hybrid Source performance. Of particular interest is the differences in hole and electron flow, as these are instrumental in the triggering of the parasitic BJT and the resultant BJT gain respectively. For the PN source, electron injection is observed across the whole of the source region, Fig. 11. Both the distribution of electrons into the bulk and the magnitude are higher than in the case of the Hybrid Source, Fig. 12. For the Hybrid Source, electron injection is also observed as a result of the ultra-shallow arsenic implant under the gate spacer. This implant is critical in enabling a low on-resistance, but as can be seen from these results it is not without the consequence of enhancing the electron injection to the bulk of the device. However, even with this enhancement of the minority carrier injection across the Hybrid Source, the BJT can still be effectively suppressed.

Passing through the resistive body of the transistor, a potential difference is created between the body of the device and the source terminal triggering the parasitic BJT [15]. By reducing the resistance, the BJT triggering can be delayed. However, in adopting a Hybrid Source, a shallower source junction is created. This enables a more direct path for holes to pass to the p+ body pick up, Fig. 14.

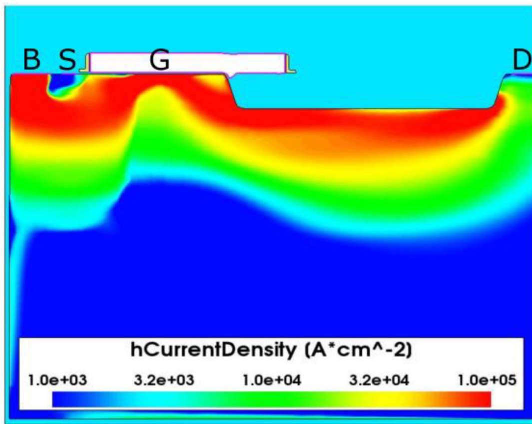

FIGURE 13. Hole current density for the PN source LDMOS Vgs = 5V, Id = 1.1mA/um, 100ns pulse.

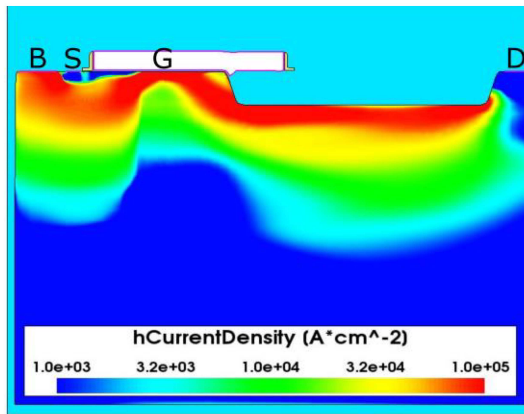

FIGURE 14. Hole current density for the Hybrid Source LDMOS Vgs = 5V, Id = 1.1mA/um, 100ns pulse.

Thus, a lower resistance is seen by the holes, and an enhancement to the electrical SOA can be expected. Previously, this resistance reduction had been in the range 21%...58% [4]. The combination of these two mechanisms, reduced body resistance and reduced electron injection from the source, are key elements in suppressing the parasitic bipolar which fundamentally changes the nature of the failure mechanism compared to a conventional LDMOS. For the conventional device, parasitic bipolar induced electrical snapback (electrical instability [14]), current filamentation and ultimately thermal failure. For the Hybrid Source LDMOS, electrical snapback is skipped and the thermal failure becomes a feature of the drain side engineering. Fig. 8 clearly illustrates this fundamental change. Although bipolar triggering has been suppressed in the Hybrid Source LDMOS, the Kirk effect [19] is still evident and the resultant high currents, electric field and impact ionization result in joule heating at the drain side, Fig. 15. At high enough currents, the critical temperature is reached and the device is destroyed. Thus, even in the absence of parasitic bipolar electrical triggering, the Hybrid Source LDMOS current capability will be limited by such thermal effects.

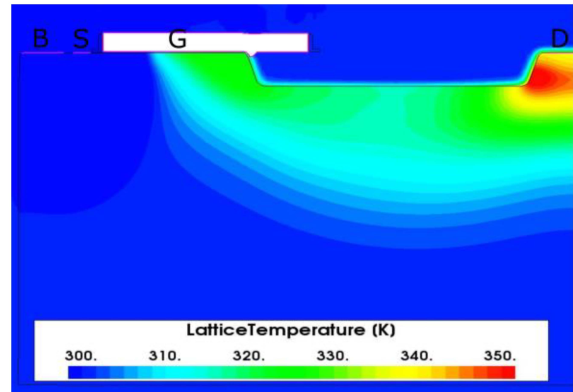

FIGURE 15. Simulated lattice temperature without an adaptive drain region, Vg = 5V, Tpulse = 2.5ns.

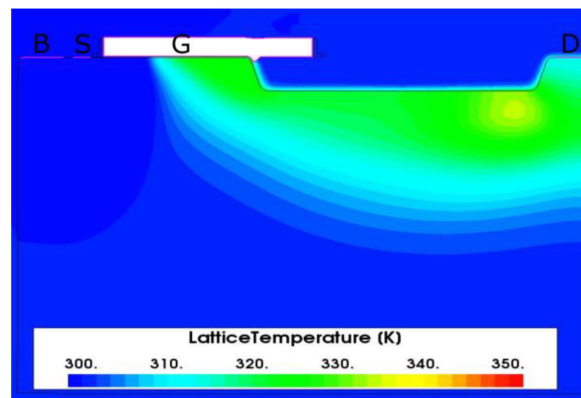

FIGURE 16. Simulated lattice temperature with an adaptive drain region, Vg = 5V, Tpulse = 2.5ns.

One key drain design feature to enable higher failure currents is the adaptive drain region [9]. The higher doping near the drain counters the additional negative charge of mobile carriers in the drift region at high drain current densities, thereby reducing the electric field and impact ionization at the drain active edge. The effect of this under TLP conditions is to reduce the lattice temperature in that region, enabling the Hybrid Source LDMOS to achieve higher failure currents than previously reported without such an adaptive drain region [4]. TCAD simulation without and with this adaptive drain region demonstrates this, Fig. 15 and Fig. 16 respectively. For the same current density, lower temperature is seen when the adaptive drain implant is used, Fig. 16, or alternatively, a higher current is needed for the adaptive drain to attain the same lattice temperature as the device without the adaptive drain. Thus, the adaptive drain enables the high It2 failure currents noted in the 2.5ns TLP results.

The combination of these design features, the Hybrid Source and the adaptive drain region, enable the Hybrid Source LDMOS to operate in bias regions that have traditionally been impossible.

VI. CONCLUSION

The Hybrid Source concept has been implemented on an 0.18μm Modular High-Voltage SOI Technology using an

integration-friendly process flow that readily lends itself to commercial application. The resultant devices sufficiently suppress the parasitic bipolar, resulting in both higher trigger voltages and trigger currents than the PN source reference devices. The Hybrid Source LDMOS can operate in bias regions that have traditionally been inaccessible in conventional LDMOS transistors due to triggering of the parasitic BJT.

REFERENCES

[1] P. Hower *et al.*, "A rugged LDMOS for LBC5 technology," in *Proc. 17th ISPSD*, Santa Barbara, CA, USA, 2005, pp. 327–330.

[2] K. Kawamoto, S. Takahashi, S. Fujino, and I. Shirakawa, "A no-snapback LDMOSFET with automotive ESD endurance," *IEEE Trans. Electron Devices*, vol. 49, no. 11, pp. 2047–2053, Nov. 2002.

[3] T. Matsudai *et al.*, "0.13µm CMOS/DMOS platform technology with novel 8V/9V LDMOS for low voltage high-frequency DC-DC converters," in *Proc. 22nd ISPSD*, Hiroshima, Japan, 2010, pp. 315–318.

[4] B. Toner *et al.*, "Schottky source LDMOS—Electrical SOA improvement through BJT suppression," in *Proc. 32nd ISPSD*, Vienna, Austria, 2020, pp. 34–37

[5] Y. Hao *et al.*, "A 0.18µm SOI BCD technology for automotive application," in *Proc. 27th ISPSD*, Hong Kong, China, 2015, pp. 177–180.

[6] J. M. Larson and J. P. Snyder "Overview and status of metal S/D Schottky barrier MOSFET technology," *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 1048–1058, May 2006.

[7] S. Zhu *et al.*, "N-type Schottky barrier source/drain MOSFET using Ytterbium silicide," *IEEE Electron Device Lett.*, vol. 25, no. 8, pp. 565–567, Aug. 2004.

[8] A. Kinoshita, Y. Tsuchiya, A. Yagishita, K. Uchida, and J. Koga, "Solution for high-performance Schottky-source/drain MOSFETs: Schottky barrier height engineering with dopant segregation technique," in *Symp. VLSI Technol. Dig. Tech. Papers*, 2004, pp. 168–169.

[9] K. Kinoshita, Y. Kawaguchi, and A. Nakagawa, "A new resurf concept for 20V LDMOS withour breakdown voltage degradation at high current," in *Proc. ISPSD*, 1998, pp. 65–68.

[10] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. Boston, MA, USA: Springer, 2008.

[11] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. New York, NY, USA: Wiley, 2007.

[12] M. Nishisaka, S. Matsumoto, and T. Asano, "Schottky source/drain SOI MOSFET with shallow doped-extension," in *Proc. Int. Conf. Solid State Devices Mater.*, 2002, pp. 586–587.

[13] O. Semenov, H. Sarbishaei, and M. Sachdev, *ESD Protection Device and Circuit Design for Advanced CMOS Technologies*. Dordrech, The Netherlands: Springer, 2008.

[14] Y. Cao, U. Glaser, S. Frei, and M. Stecher, "A failure levels study of non-snapback ESD devices for automotive applications," in *Proc. IEEE IRPS*, Anaheim, CA, USA, 2010, pp. 458–465.

[15] P. L. Hower, "Safe operating area—A new frontier in LDMOS design," in *Proc. 14th ISPSD Conf.*, Santa Fe, NM, USA, 2002, pp. 1–8.

[16] S. Reggiani *et al.*, "Experimental extraction of the electron impact-ionization coefficient at large operating temperatures," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2004, pp. 407–410.

[17] Y. Chung, H. Xu, R. Ida, W. G. Min, and B. Baird, "ESD scalability of LDMOS devices for self-protected output drivers," in *Proc. 17th ISPSD Conf.*, Santa Barbara, CA, USA, 2005, pp. 351–354.

[18] M. Shrivastava, H. Gossner, M. S. Baghini, and V. R. Rao, "Part II: On the three-dimensional filamentation and failure modeling of STI type DeNMOS device under various ESD conditions," *IEEE Trans. Electron Devices*, vol. 57, no. 9, pp. 2243–2250, Sep. 2010.

[19] A. W. Ludikhuize, "Kirk effect limitations in high voltage IC's," in *Proc. 6th ISPSD Conf.*, 1994, pp. 249–252.