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# Analyses and Experiments of Ultralow Specific On-Resistance LDMOS With Integrated Diodes

**JIE WEI (Member, IEEE), KAIWEI DAI, XIAORONG LUO (Senior Member, IEEE), ZHEN MA, JIE LI, CONGCONG LI, AND BO ZHANG (Senior Member, IEEE)**

State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu 610054, China

CORRESPONDING AUTHOR: X. LUO (e-mail: xrluo@uestc.edu.cn)

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**ABSTRACT** An ultralow specific on-resistance ($R_{on,sp}$) accumulation-mode LDMOS (ALDMOS) is proposed and investigated by simulations and experiments. The proposed ALDMOS features two separated integrated diodes (SID) above the N-drift surface, which forms high density electron accumulation layer in the on-state. Meanwhile, the SID not only assists depleting the N-drift to increase the N-drift doping centration ($N_d$) in the off-state, but also modulates the lateral electric field to improve the breakdown voltage ($BV$). Thus, the proposed SID ALDMOS could achieve ultralow $R_{on,sp}$ and maintain high $BV$ simultaneously. The layout and key fabrication processes of the SID ALDMOS are demonstrated. The measured results show that the SID ALDMOS realizes a $BV$ of 483V and $R_{on,sp}$ of 29.3m$\Omega$.cm$^2$, with a high FOM value of 7.96MW/cm$^2$. Its $R_{on,sp}$ is decreased by 33.7% compared with triple RESURF LDMOS at the same $BV$.

**INDEX TERMS** Specific on-resistance, accumulation mode, LDMOS, breakdown voltage, integrated diode.

## I. INTRODUCTION

Owing to its high input impedance, low parasitic capacitance, and ease of integration, power LDMOS is the key component in smart power integrated circuits (SPICs), which is widely applicated in converters, automotive and so on [1]–[2]. High breakdown voltage ($BV$) and low specific on-resistance ($R_{on,sp}$) are the two major designing targets for power MOSFETs to achieve superior system performances. However, owing to the "Silicon Limit" relationship of $R_{on,sp} \propto BV^{2.5}$ [3], the $R_{on,sp}$ increases rapidly with the increasing $BV$ and then results into high power dissipation. To improve the tradeoff relationship between the $BV$ and $R_{on,sp}$, typical Reduced surface field (RESURF) technology [3]–[4] and superjunction (SJ) technology [5]–[8] are widely adopted. These two technologies introduce P-type region into the N-drift to modulate the electric field distribution to achieve high $BV$, and to enhance the depletion effect to increase the N-drift doping concentration ($N_d$) and then decrease the $R_{on,sp}$. But the $R_{on,sp}$ is still mainly depended on the $N_d$, because the current is transferred in the neutral drift region. To further decrease the $R_{on,sp}$ and relieve the dependence of $R_{on,sp}$ on $N_d$ at a certain extent, the concept of accumulation-mode LDMOS (ALDMOS) is proposed and studied in [9]–[11]. Since it forms high density electron accumulation layer at N-drift surface to provide an additional low resistance path in the on-state, its current is transferred in both the neutral drift region and accumulation layer. Reference [11] demonstrates the advantages of ALDMOS on decreasing the $R_{on,sp}$, even though its N-drift length ($L_D$) is not fully utilized to sustain the voltage in the off-state. That means the tradeoff relationship between the $BV$ and $R_{on,sp}$ could be further improved by optimizing the $L_D$.

Based on our previous work of ALDMOS [11]–[12], this paper further analyses and illustrates a novel ALDMOS with two separated integrated diodes (SID) by simulations and experimental results. The measured results show that this novel SID ALDMOS decreases the $R_{on,sp}$ by 33.7% compared with the triple RESURF LDMOS at the same $BV$.

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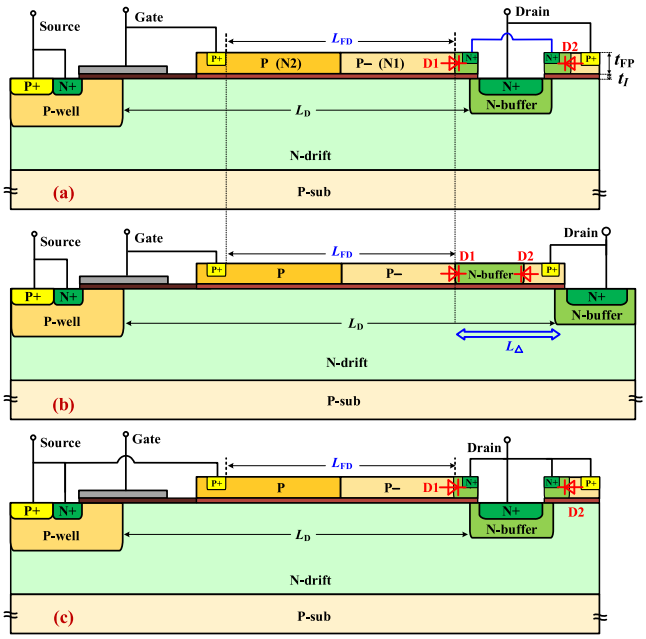


**FIGURE 1.** Schematic cross-section view of (a) the proposed accumulation-mode LDMOS with two separated integrated diodes (SID ALDMOS), (b) the accumulation-mode LDMOS with two adjacent integrated diodes (AID ALDMOS) and (c) the LDMOS with two separated integrated diodes (SID LDMOS).

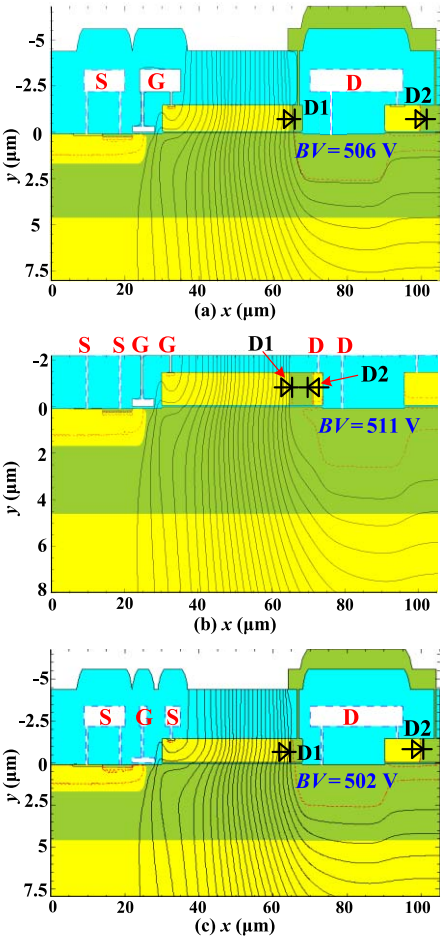


**FIGURE 2.** Process simulation results of equipotential contours distribution (20V/contour) at breakdown voltage for (a) SID ALDMOS, (b) AID ALDMOS and (c) SID LDMOS.

## II. STRUCTURE AND MECHANISM

Fig. 1(a) illustrates the schematic cross-section view of the accumulation-mode LDMOS featuring two separated integrated diodes (SID ALDMOS), wherein the diode D1 and D2 are located on both side of the drain N+ region and connected through metal. For our previous accumulation mode LDMOS with adjacent integrated diodes (AID ALDMOS) as shown in Fig. 1(b) [11], the diode D1 and D2 are directly connected and both located upon the N-drift region. For both the SID and AID ALDMOS, the anode of diode D1 and D2 are connected to the gate and drain electrode, respectively. Obviously, the SID ALDMOS shortens the N-drift length ($L_D$) as the blue arrow shown in the Fig. 1(b), because the location of diode D2 is redefined. As shown in Fig. 1(c), for LDMOS featuring two separated integrated diodes (SID LDMOS), the anode of diode D1 and D2 are connected to the source and drain electrode instead.

In the off-state with $V_{GS} = 0$ and $V_{DS} > 0$, the three devices shown in Fig. 1 share almost the same working mechanism with D1 reverse biased and D2 forward biased [10]–[11]. Thus, the step-doped P-type region of diode D1 assists in depleting the N-drift and modulates the electric field distribution to improve the $N_d$ and the $BV$. In the on-state with $V_{GS} > V_{th}$ and $V_{GD} > 0$, both the SID and AID ALDMOS could accumulate high density electrons layer at the N-drift surface with diode D1 forward biased and D2 reverse biased, so as to achieve ultralow $R_{on,sp}$. While SID LDMOS doesn't form accumulation electron layer in the on-state, because its anode of diode D1 is connected to the source electrode instead of the gate electrode.

Fig. 2 depicts the equipotential contours distributions at breakdown voltage for the SID ALDMOS, AID ALDMOS and SID LDMOS. With the same $L_{FD} = 31$ $\mu$m of diode D1, the SID ALDMOS and SID LDMOS with the same $L_D = 40$ $\mu$m achieve almost the same $BV$ values as that of AID ALDMOS with $L_D = 51$ $\mu$m. Furthermore, Fig. 3 illustrates the N-drift surface lateral component of electric field ($E_x$) distributions at breakdown voltage for the three devices. Obviously, the $E_x$ value for AID ALDMOS below diode D2 region (labeled as the blue arrow) is almost zero, which means this part of drift length is not involved to sustain the $BV$. By redefining the location of diode D2 into the drain electrode region, the N-drift of SID ALDMOS and LDMOS are shortened and better utilized to sustain the same $BV$ level.

Fig. 4 compares the electron density distribution along the N-drift surface in the on-state for the SID ALDMOS, AID ALDMOS and SID LDMOS. It is notable that both SID and AID ALDMOS exhibit high accumulation electron density at the N-drift surface, which is about two orders higher than that of SID LDMOS and the N-drift doping concentration

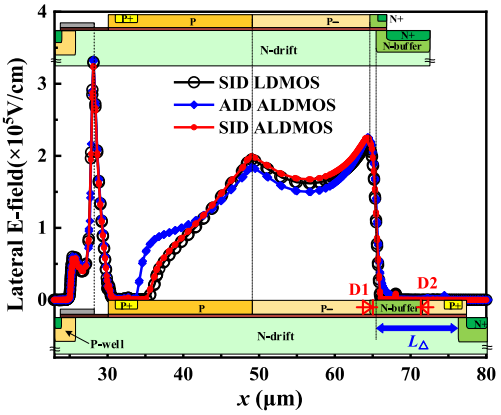


**FIGURE 3.** Lateral component of the electric field distribution at N-drift surface at breakdown voltage for the SID LDMOS, AID ALDMOS and SID ALDMOS.

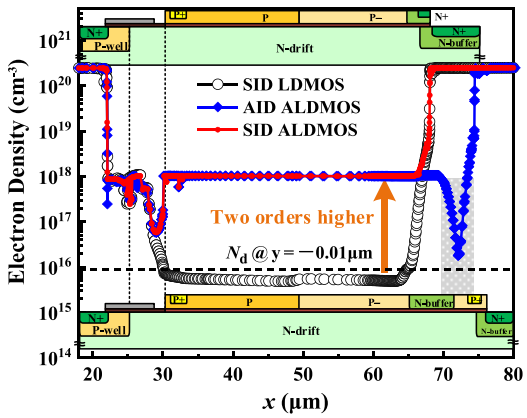


**FIGURE 4.** Electron concentration distribution at N-drift surface in the on-state with $V_{GS}$ = 15V and $V_{DS}$ = 0.5V.

($N_d$). Note that there is no accumulation electron layer in the N-drift of SID LDMOS. Moreover, the SID ALDMOS owns continuous electron accumulation layer at drain side, while the AID ALDMOS shows discontinuous electron accumulation layer below the diode D2 region shown as the gray region. Therefore, combing the shorter N-drift length and continuous accumulation electron layer, the proposed the SID ALMDOS could achieve lower $R_{on,sp}$ and maintain the same *BV* level.

## III. RESULTS AND DISCUSSION

Fig. 5 shows the key fabrication processes and parameters for the SID ALDMOS. The N-drift phosphorus implantation is firstly fulfilled and then the two wafers are bonded, so as to share the high temperature annealing at 1150°C for 6 hours. It's worthy note that each wafer surface is prematurely formed with a 30nm oxide layer by dry thermal oxide process before wafer bonding, so as to ensure the quality of the oxide and the carrier mobility in the drift surface. After the formed SOI layer CMP thinning down to 1.5$\mu$m with an oxide layer thickness of 60nm, the first step-doped implantation (dosage N1) for the P-region of diode D1 is carried

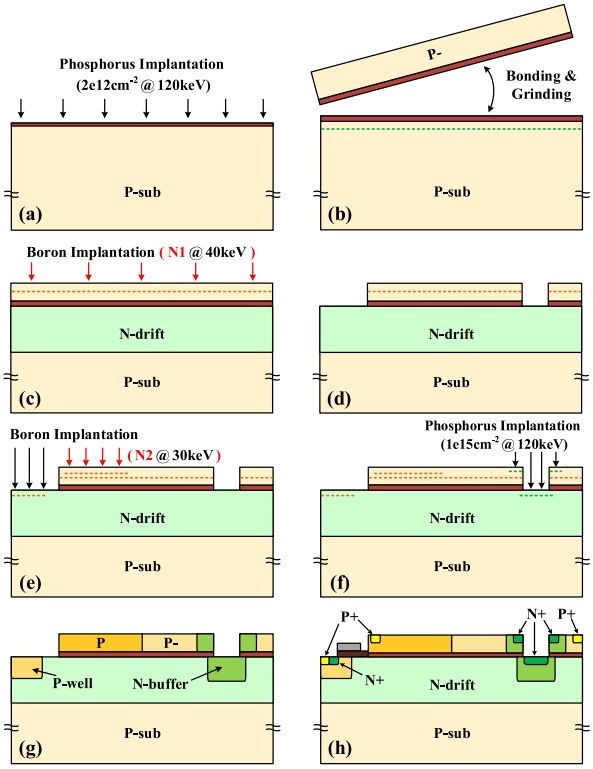


**FIGURE 5.** Key fabrication processes for SID ALDMOS. (a) N-drift phosphorus implantation, (b) wafer bonding and grinding, (c) first step-doped boron implantation, (d) part SOI region etching, (e) P-well and second step-doped boron implantations, (f) N-buffer phosphorus implantation via one mask, (g) high temperature annealing, (h) form the gate structure, N+/P+ implantation and electrode formation of gate, source and drain.

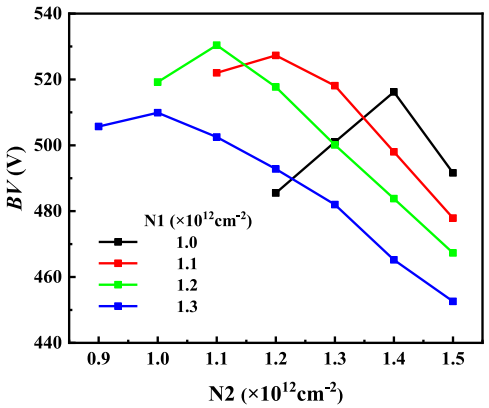


**FIGURE 6.** Simulated *BV* as a function of the two step-doping dosage N1/N2.

out without mask. Then the formed SOI layer is selectively etched to remain the diodes region. The second step-doped implantation (dosage N2) for the P-region of diode D1, the P-well and the N-buffer implantations are carried out orderly, followed by an annealing process at 1150°C for 90 minutes to activate and drive in the dopants. Then the gate structure is formed and the rest steps are to conduct the N+/P+ implantations and form the device electrodes and so on.

Fig. 6 shows the influences of the first and second step-doping dosage (N1 and N2) on the *BV*. For a given N1 value,

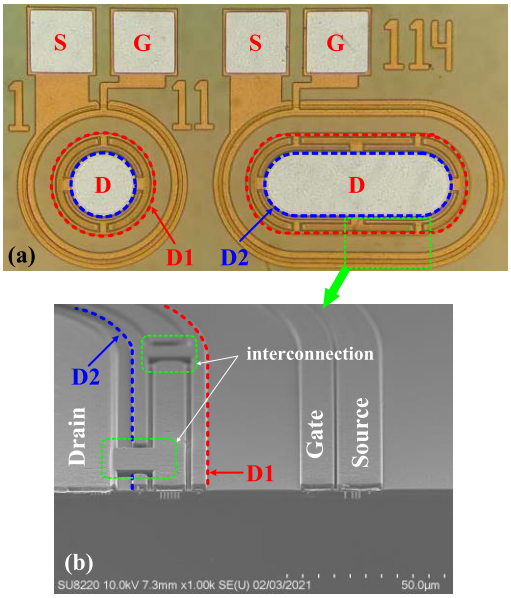


**FIGURE 7.** (a) Micro-photos of the fabricated SID ALDMOS with circle and track layout. The locations of the diode D1 and D2 are labeled as red and blue dash lines, respectively. (b) SEM image of the cross-sectional view.

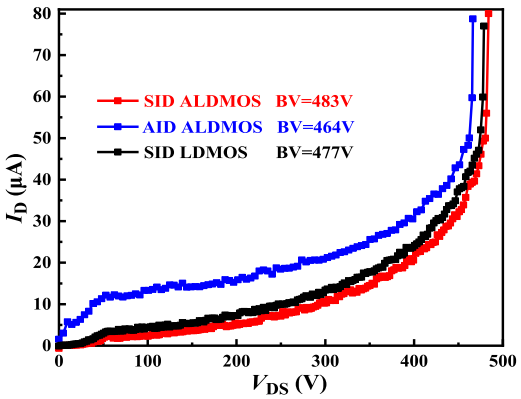


**FIGURE 8.** Measured breakdown characteristics for the three devices.

the *BV* firstly increases and then decreases with the increasing N2 value. Based on the charge balance principle, the N2 value corresponding to maximum *BV* of each curve decreases with the increasing N1 value. Too high or too low dosage causes premature breakdown around the gate side in the field plate structure or N-drift region. In this work, the optimized dosages are set as N1/N2 = $1.1/1.2\times10^{12}$ cm$^{-2}$ by considering the process deviations and compatibilities.

Fig. 7 illustrates the micro-photos and SEM image of the fabricated SID ALDMOS. It can be seen clearly that the diode D1 and D2 are inter-connected through one metal layer. Moreover, the diode D2 is relocated under the drain contact region, which is beneficial to decrease the drift length and then save the device area.

Fig. 8 depicts the measured breakdown characteristics of the three devices. With the same length $L_{FD}$ = 31 $\mu$m, the novel SID ALDMOS and SID LDMOS realize a little higher *BV* of 483V and 477 than 464V of AID ALDMOS, because

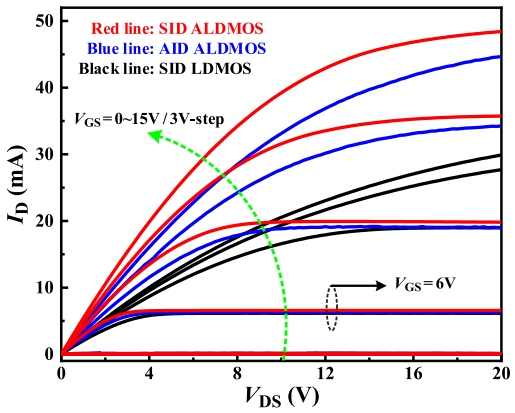


**FIGURE 9.** Measured output characteristics for the three devices.

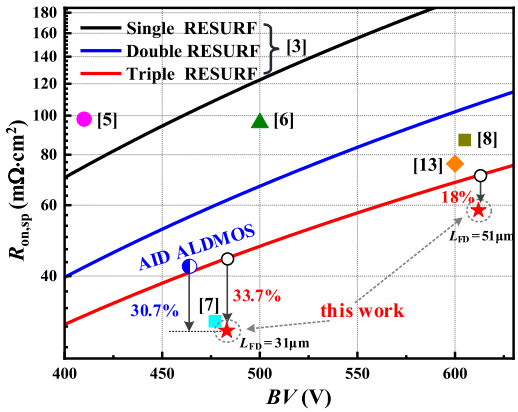


**FIGURE 10.** Comparison of trade-off relationship between the *BV* and $R_{on,sp}$ among different devices.

the SID structure is beneficial to suppress the leakage current induced by the parasitic PNP transistor formed by the AID structure. Fig. 9 compares the output characteristics among the three devices. Obviously, the SID LDMOS shows the lower output currents than other two devices, because it doesn't form accumulation layer in the on-state as shown in Fig. 3. On the other hand, as the SID ALDMOS forms continuous accumulation layer at the drain side and owns shorter drift length $L_D$ for the same *BV* level, it demonstrates higher saturation current than AID ALDMOS. For high voltage power LDMOS devices, it's a universal way to calculate the $R_{on,sp}$ with the area of N-drift part [7]. Therefore, with an N-drift area of $1.6\times10^{-4}$ cm$^2$ and $1.84\times10^{-4}$ cm$^2$ for SID LDMOS/ALDMOS and AID ALDMOS in track layout (shown in Fig. 7), the extracted $R_{on,sp}$ of the SID ALDMOS is 29.3 mΩ·cm$^2$, which is 30.7% and 49.6% lower than 42.3mΩ·cm$^2$ of AID ALDMOS and 58.1 mΩ·cm$^2$ of the SID LDMOS fabricated at the same time, respectively. Thus, The SID ALDMOS achieves much higher figure of merit (FOM = $BV^2/R_{on,sp}$) of 7.96 MW/cm$^2$ than 5.09 MW/cm$^2$ of AID ALDMOS and 3.92 MW/cm$^2$ of SID LDMOS.

As illustrated in Fig. 10, the proposed SID ALDMOS achieves superior tradeoff relationship between the *BV* and

$R_{on,sp}$. Compared with the Triple RESURF LDMOS at the same $BV$ values, the proposed SID ALDMOS devices decrease the $R_{on,sp}$ by 33.7% and 18% respectively.

## IV. CONCLUSION

This work presents a novel ALDMOS with two separated integrated didoes above the drift surface by simulations and experiments. By redefining the location of the integrated diode D2, the novel SID ALDMOS could shorten the drift length to sustain the same $BV$ level and form continuous accumulation layer at the drain side, achieving superior trade-off relationship between the $BV$ and $R_{on,sp}$. The measured results demonstrate that the SID ALDMOS achieves $R_{on,sp}$ of 29.3 m$\Omega$·cm$^2$ and $BV$ of 483V, with a high FOM value of 7.96 MW/cm$^2$. The SID ALDMOS reduces the $R_{on,sp}$ by 30.7% and 49.6% compared with the AID ALDMOS and SID LDMOS, respectively.

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