Received 27 May 2021; revised 21 July 2021; accepted 16 September 2021. Date of publication 23 September 2021; date of current version 30 September 2021.
The review of this article was arranged by Editor C. Bulucea.

Digital Object Identifier 10.1109/JEDS.2021.3114751

Design and Numerical Verification of a Gate-Controlled Lateral Thyristor for Low-Light Level Detection

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This work was supported by the National Natural Science Foundation of China under Grant 61734004.

ABSTRACT Thyristors operated at switching point are highly sensitive to external physical signals such as light or temperature. However, due to the instability of sensitive switching point, conventional thyristors are commonly used as optical switches and hardly applied for low-light level detection. In this work, a silicon-based gate-controlled lateral thyristor (GC-LT), which takes advantage of high sensitivity at low-light, is studied by numerical simulation. A thyristor photodetector circuit and a novel super-off Reset operation method are also proposed to bias the GC-LT over the switching point quickly and allow the photodetector to be operated in a monotonic dynamic multi-sampling mode to achieve high sensitivity to low-light. Simulation results show that the Reset time can be shortened to <10 μs without trigging the GC-LT. The trigger time of the photodetector is sensitive to the optical power density ranging from 1×10^{-9} to 2.5×10^{-6} W/cm^2. Furthermore, the average optical gain is about 8.0-6.3, approximately one order of magnitude higher than that of the Si pinned photodiode.

INDEX TERMS Thyristor, photodetector, low-light level detection, operation method, multi-sampling, optical gain.

I. INTRODUCTION

The present-day silicon-based charge-coupled devices (CCDs) and complementary metal-oxide-semiconductor (CMOS) devices are the mainstream technologies for imaging sensors. CCDs has been the dominating imaging technology owing to the superior quantum efficiency and low readout noise [1], [2]. On the other hand, CMOS imaging sensors are preferred in consumer and industrial imagers because of low power consumption, high resolution and low cost [3]–[6].

In low-light level imaging area, conventional CMOS imaging sensors based on photodiodes face great challenges due to their low quantum efficiency [3]. To achieve low-light level detection, highly responsive photodetectors, such as avalanche photodiodes (APDs) and phototransistors, have been developed [7]–[13]. The high responsivity of APDs originates from their high gain factors (several hundreds or even higher) as a result of electron avalanche. However, the circuit overhead, the high operation voltages, and the avalanche noise limit the application areas of APDs [7], [8].

Phototransistors also have higher responsivity than photodiodes owing to the internal gain [9]–[13]. However, the photocurrent at low-light level is insufficient to set conventional phototransistors to the forward amplification operation region and thus the conversion gain deteriorates abruptly when the incident optical power decreases [9]. Some improved phototransistors, such as punchthrough enhanced phototransistors and gate-controlled lateral phototransistors, have been proposed to improve the sensitivity to light, but the improvement in conversion gain results in high dark current [12], [13].

In this paper, we report a different approach that uses a novel thyristor-based device for low-light level detection. Thyristors, with an intrinsic bi-stable feature for

electrical conduction, have mostly been used to develop bi-stable optical controlled electrical switches [14]–[16]. Some researchers have used thyristors as long wavelength infrared photodetectors that operated at the off-state with low dark currents [17]. However, when operated at the off-state, thyristors exhibit low responsivity to light because they are essentially reversed p-n junctions that have low quantum efficiency. More importantly, studies illustrate that thyristors could achieve high amplification factors when biased at the switching point [18]–[20]. However, it is impractical to set thyristors to work at the switching point exactly because of the inherent instability and the inevitable process variations.

To avoid this problem, we propose a novel gate-controlled lateral thyristor (GC-LT) structure and a new thyristor photodetector circuit. A super-off *Reset* operation method is developed to bias the GC-LT over the switching point quickly and allow the photodetector to be operated in a monotonic dynamic multi-sampling mode, which operates as a diode, a transistor and a thyristor sequentially in one sampling period. The GC-LT configuration, the photodetector circuit, the operation mode and the principle of photo-response are presented. Numerical simulation is performed to validate the proposed GC-LT device and investigate the electrical characteristics.

II. DEVICE CONFIGURATION AND OPERATION PRINCIPLE

A. BACKGROUND OF THYRISTORS

A conventional thyristor consists of four alternating layers of p-type and n-type semiconductor materials, as shown in Fig. 1(a). It is an unidirectional device and only conducts current in forward direction. Fig. 1(b) illustrates its forward static current-voltage (I-V) characteristics. It can be operated in four states by applying different forward voltages. The first state, curve I in Fig. 1(b), is an off-state that is achieved by applying the anode with a voltage (V_a) positive to the cathode. In such a condition, the emitter junctions J_1 and J_3 are slightly forward biased and the intermediate collector junction J_2 is reverse biased. In this off-state, the thyristor is essentially equivalent to a reversed p-n junction (a diode) with a small reverse saturation current (I_S).

As V_a increases, the forward biased voltages between the bases and the emitters (V_{BE}) of the emitter-base junctions J_1 and J_3 increase consequently. And the internal cross-coupled n^+pn/pnp^+ transistors work in a forward mode, resulting in the second state that has an increased anode current, as shown by curve II. If V_a is larger than the switching voltage V_{SW}, the thyristor is operated in the on-state, as shown by curve IV. In the on-state, the emitter-base junctions J_1 and J_3 are forward biased, and the collector junction J_2 turns to slightly forward biased. Under this condition, the internal n^+pn/pnp^+ transistors work in a saturation amplification mode, representing the forth state. As the on-state current is limited only by the two forward biased junctions J_1 and J_3, the thyristor essentially works as two parallel rectifying diodes. Since the forward on-state resistance is rather low, the voltage between the anode and cathode drops rapidly

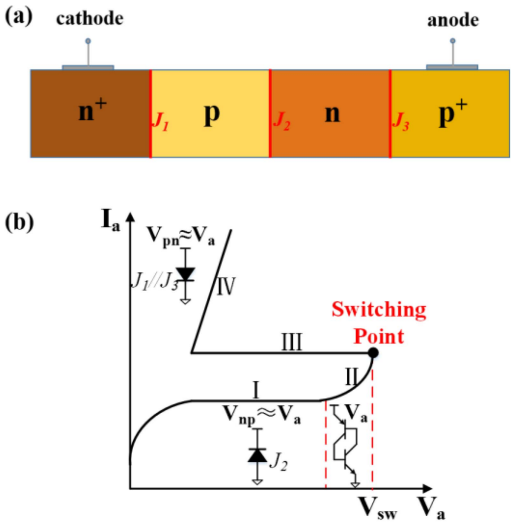

FIGURE 1. Conventional thyristor and I-V curves. (a) Structure of a conventional thyristor, (b) Forward static I-V characteristics and abstract states.

and the transition from curve III to curve IV is very sharply, represented by the negative resistance hysteretic curve III. Due to the small voltage range in curve II and the variation of the switching point, conventional thyristors can only be operated as either an open-circuit switch or a rectifying diode, depending on the biased voltage.

The operation curves indicate that if a thyristor can be operated exactly at the switching point, large amplification factors and high sensitivity to external signals such as light can be achieved [18]–[20]. The high amplification capability is attributed to the fact that the thyristor operates as two cross-coupled bipolar transistors, as shown in the inset in Fig. 1(b). The two transistors force each other to conduct to saturation as they are connected in a regenerative feedback loop. Unfortunately, it is extremely difficult, even impossible, to operate thyristors at the transition region because of the inherently unstable characteristics at the switching point. Even if a thyristor can be biased at the unstable point after elaborate adjustment, it is impractical to use thyristors in large scale array for imaging because the inevitable process fluctuations cause the bias condition of each thyristor different from others.

B. DEVICE CONFIGURATION AND OPERATION PRINCIPLE

Fig. 2(a) shows the configuration of the new GC-LT and a photodetector circuit. The GC-LT consists of three control gates namely G1, Gate, and G2 and four doping regions in sequence of n^+-p-n-p^+. The n^+ and p^+ regions act respectively as the n-emitter (cathode) and p-emitter (anode), and the intermediate N-well and P-sub act as the n-base and p-base, respectively. Like a normal thyristor, the n^+-p-n-p^+ regions can also work as two cross-coupled bipolar transistors, which the collector of the pnp^+ (n^+pn) transistor is connected to the base of the n^+pn (pnp^+) transistor [16]. The intermediate control gate, labeled as Gate, is a polysilicon gate coupled capacitively to the N-well and P-sub regions

through the gate oxide. Two sidewall control gates, G1 and G2, locate at the two sides of the intermediate gate with G1 on the P-sub region and G2 on the N-well region. These two gates are used to adjust the amplification characteristics of the two cross-coupled bipolar transistors and the time to trigger the detector (defined as T_{SW}).

To bias the GC-LT near the switching point for high sensitivity to light, a circuit consisting of a GC-LT, a nMOSFET M1 and two pMOSFETs M2 and M3 is proposed, as shown in Fig. 2(a). M1 and M2 act as selection transistors and M3 act as a reset transistor. It should be noted that the total parasitic capacitor ($C_1 + C_S$) at the anode is larger than the parasitic capacitor C_2 at the N-base electrode because of the large external sampling capacitor C_S.

Fig. 2(b) shows the equivalent static current-voltage characteristics of the proposed device. The key factor is that the hysteresis curve with a switching point is changed to a monotonic curve by using the super-off operation method in reset mode. This allows the GC-LT to be operated in a multi-sampling mode including diode, transistor, and thyristor sampling modes to improve the sensitivity to light.

Fig. 2(a) illustrates the super-off *Reset/Sampling* operation sequences and the corresponding equivalent devices/circuits. In the initial *Reset* period, M3 is turned on to charge the anode to a voltage V_a higher than the switching voltage V_{SW}. Simultaneously, M1 and M2 are turned on so that the p-base region and n-base region are shorted with the n^+ region and the p^+ region, respectively. The intermediate p-n junction J_2 is reverse biased, and then M1 and M2 are turned off to establish the multi-sampling mode. Owing to the capacitance booster effect of the gate-drain parasitic capacitance C_2, the gate closing signal of M2 raises the potential of the n-base region to the level higher than that of the p^+ region. Therefore, the emitter-base junction J_3 is slightly reverse biased and the thyristor is in a super-off state, corresponding to curve I' in Fig. 2(b) with $V_a > V_{SW}$.

With the proposed super-off *Reset* operation method, the GC-LT can be quickly set to diode sampling mode at the beginning. The dark current and the photocurrent generated in the intermediate p-n junction J_2 raise the potential of the p-base region and reduce the potential of the n-base region to accelerate the bias of the emitter-base junctions J_1 and J_3 from reverse to zero and then to forward. The cross-coupled n^+pn/pnp^+ transistors turn to work in forward amplification mode and the GC-LT gradually shifts to transistor or thyristor sampling mode corresponding to curve II'. Specifically, at the beginning of state II', the gain of the pnp^+ transistor is rather low, and the n^+pn transistor plays a dominating role, leading the GC-LT to work in transistor sampling mode. With the increase in the positive bias of emitter-base junction J_3, the amplification capability of the pnp^+ transistor enhances gradually, and the GC-LT turns to thyristor sampling mode with the two cross-coupled transistors acting as regenerative feedback amplifiers. Ultimately, the GC-LT can be triggered into the on-state (IV'). It needs to be noted that the transistor and thyristor sampling modes achieve a large current gain to

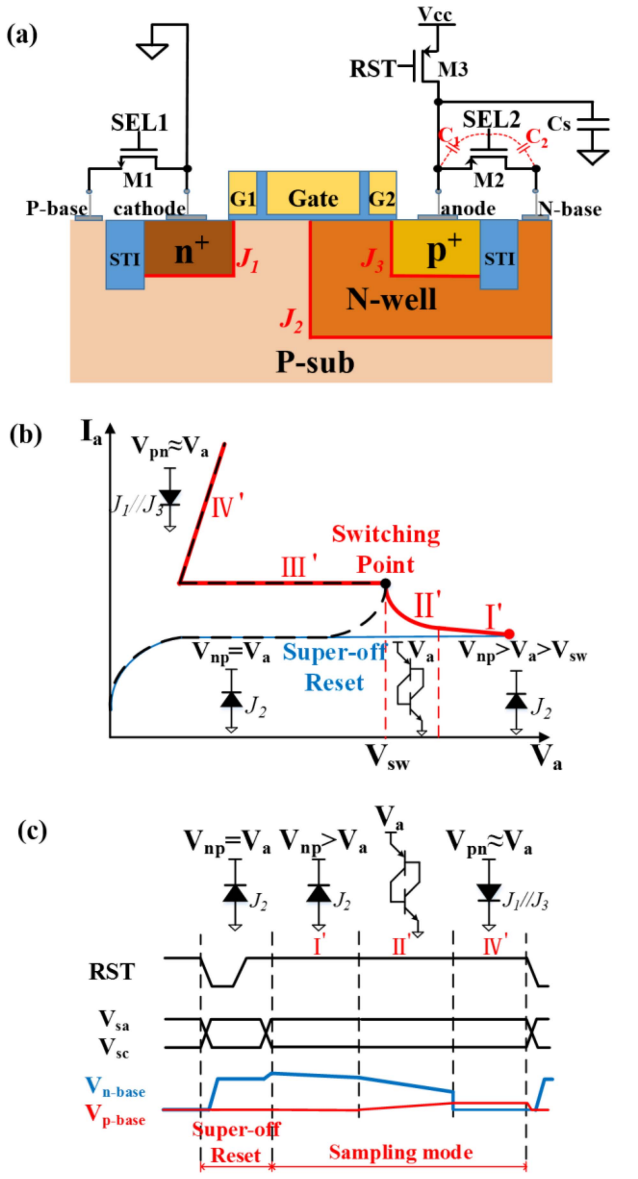

FIGURE 2. Configuration and the operation principle of the proposed gate-controlled lateral thyristor device. (a) Configuration of the GL-LT and schematic of the photodetector circuit, (b) Equivalent static current-voltage characteristics, (c) Dynamic operation schemes and state schematic.

photocurrent, so the trigger time T_{SW} is sensitive and directly affected by the photocurrent. Obviously, the optical power density can be quantitatively characterized by detecting the trigger time of the GC-LT.

C. NUMERICAL SIMULATION

The GC-LT and the thyristor photodetector circuit are numerically simulated using the Synopsys Sentaurus two-dimensional (2D) device simulator. Fig. 3 shows the model of the GC-LT in 0.35 μm CMOS process as well as the photodetector circuit. The incident light is added to the top surface of the GC-LT using the simulator. The mobility models consider the effects of impurities, surface roughness, carrier scattering, and high field rate saturation. The

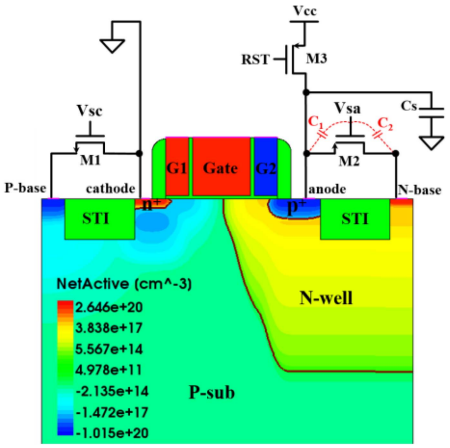

FIGURE 3. **The main part structure of the GC-LT and schematic of the photodetector circuit in this work.**

TABLE 1. **Simulation parameters for the GC-LT and the photodetector circuit.**

Quantity	Symbol	Value
Gate length	L_{Gate} (μm)	0.5
Sidewall gate length	L_{G1},L_{G2} (μm)	0.2
Doping concentration	N_{n+} (cm^{-3})	1×10^{20}
	N_{p+} (cm^{-3})	1×10^{20}
	$N_{N\text{-}well}$ (cm^{-3})	3×10^{17}
	$N_{P\text{-}sub}$ (cm^{-3})	3×10^{17}
Cross-section area	S_{cs} (μm^2)	3×1
Incident light wavelength	λ (nm)	550
Optical power density	P_{in} (W/cm^2)	1×10^{-9}~2.5×10^{-6}
Absorption coefficient	α (cm^{-1})	2×10^{-4}
Power supply voltage	V_{cc} (V)	4.5
Temperature	T (℃)	25
Transmittance of STI	A (%)	100

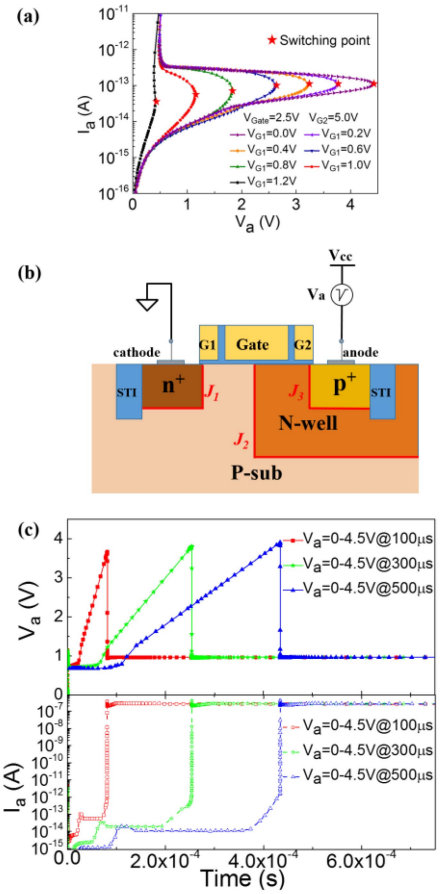

FIGURE 4. **(a) The forward static I-V characteristics of the GC-LT at different V_{G1}. (b) Configuration of the traditional *Reset* operation method. (c) The anode voltages and currents of the GC-LT (V_{G1} = 0 V) under the traditional *Reset* method.**

STI means shallow trench isolation and allows visible light to pass through. The parameters used in the simulation are listed in the Table 1.

III. RESULTS AND DISCUSSIONS

A. DYNAMIC RESET/SAMPLING OPERATION CHARACTERISTICS

Fig. 4(a) shows the forward static I-V characteristics of the GC-LT at different V_{G1}. The switching voltage is about 4.4 V when the V_{G1} is 0 V. And the switching voltage decreases with the increase of V_{G1}. Similar to the traditional *Reset* method of the photodiodes, we bias the operating point by applying reset pulse to the anode directly, as shown in Fig. 4(b).

To illustrate the relationship between the trigger time and the reset time, we set 100 μs, 300 μs and 500 μs respectively for V_a to rise from 0 to 4.5 V linearly. Fig. 4(c) shows that the GC-LT is triggered at 81 μs, 254 μs and 434 μs. The anode voltage finally rises to about 3.65 V, 3.81 V and 3.91 V, respectively. The maximum anode voltages rise slightly with the increase of the reset time, but still could not reach the switching voltage (V_{SW} = 4.4 V). The instability of switching point is not only related to inevitable process variations, but also affected by the reset time. Therefore, it is impractical to set thyristors to work at the switching point exactly and quickly using the traditional *Reset* method.

Fig. 5(a) shows the simulated electrical characteristics of the GC-LT operated in the dynamic super-off *Reset/Sampling* scheme (V_{G1} = 0 V). The anode voltage could be set to 5.4 V higher than the switching voltage (V_{SW} = 4.4 V). And the anode current is $<10^{-13}$ A, indicating that the GC-LT is super-off state (I'). Moreover, it is worth noting that the *Reset* time could be shortened to <10 μs without trigging the GC-LT. The capacitive booster effect is used to bias the GC-LT at super-off state (I') to establish the multi-sampling mode quickly. The emitter-base junction J_3 gradually changes from reverse bias to positive bias (II') due to the leakage current. The GC-LT is triggered (IV') when the current injected into the n-base region is sufficient to trigger the cross-coupled bipolar transistors to regenerative feedback amplification. Since the leakage current is as low as *fA* level, it takes a relatively long time to trigger the GC-LT. This trigger period, defined as dark trigger time (T_0),

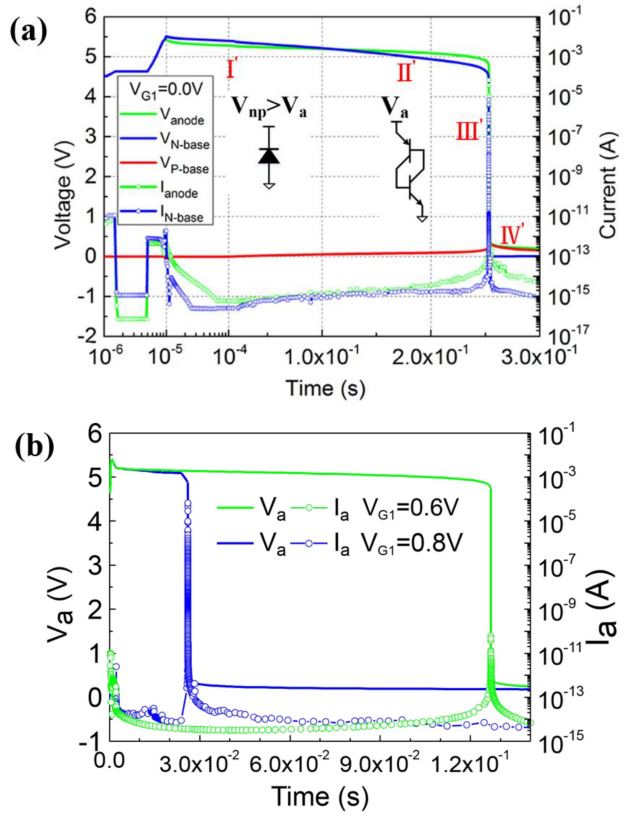

FIGURE 5. Electrical characteristics of GC-LT under the dynamic super-off *Reset/Sampling* operation scheme with (a) $V_{G1} = 0$ V, and (b) $V_{G1} = 0.6$V/0.8V.

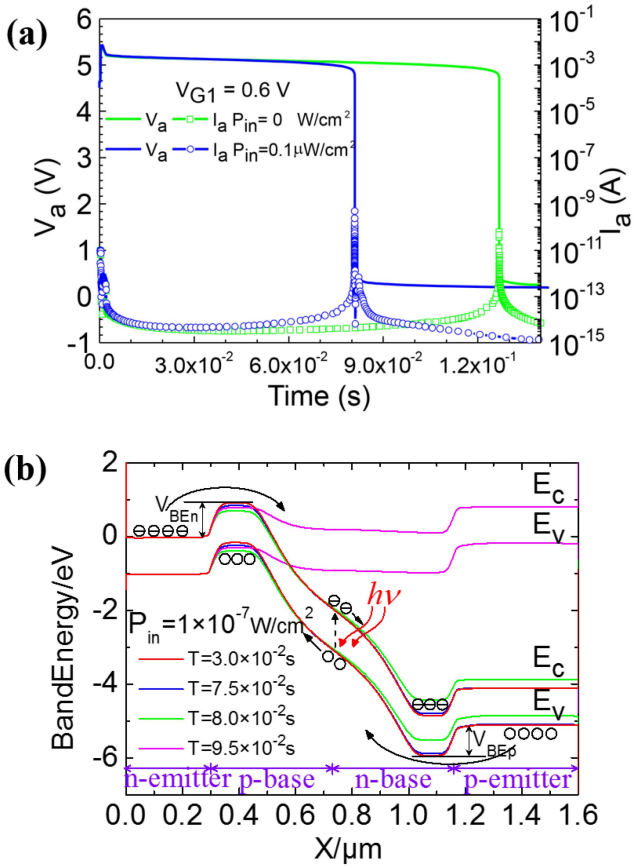

FIGURE 6. Photo-response characteristics of the GC-LT with optical power density $P_{in} = 1 \times 10^{-7}$ W/cm^2. (a) Photo-response as anode voltage V_a and anode current I_a of GC-LT. (b) The energy band diagram at different time under illumination.

is the detection window for the multi-sampling mode. As shown in Fig. 5(a), the simulated detection window is about 255 ms at $V_{G1} = 0.0$ V, implying that operation in this mode causes poor frame rates.

As shown in Fig. 5(b), the leakage current is about 3 fA/10 fA and the detection window time reduces to 127 ms/26 ms at $V_{G1} = 0.6$ V/0.8 V, respectively. It is obvious that higher V_{G1} can turn on the parasitic nMOSFET M_{G1} and induce an extra sub-threshold pull-down current I_{pd} to accelerate the trigger of the GC-LT, which therefore reduce the detection window time. This implies that the detection window can be adjusted through the sidewall control gate voltage V_{G1}. To ensure an appropriate frame rate and a low leakage current, $V_{G1} = 0.6$ V is chosen in the following numerical simulation.

B. PHOTO-RESPONSE CHARACTERISTICS

Fig. 6(a) shows the simulated anode voltage V_a and current I_a in response to a constant incident optical power density of 1×10^{-7} W/cm^2 to characterize the photo responsivity of the GC-LT. The trigger time dramatically reduces from 127 ms to 81 ms, approximately 36.2% reduction, indicating that the GC-LT is rather sensitive to low-level light. Fig. 6(b) illustrates the energy band diagram at different sampling time. The photo-carriers are generated in the depletion region of the intermediate p-n junction J_2 under illumination and swept into the p-base/n-base region under the electric field introduced by V_a.

Fig. 6(b) also shows that the accumulation of the majority carriers in the p-base/n-base region leads to the decrease in the barrier height ϕ_{BEn}/ϕ_{BEp}, resulting in amplified electron/hole currents injection to the n-base/p-base regions. The amplified electron/hole currents contribute to the decrease in the barrier height ϕ_{BEn}/ϕ_{BEp}. The regenerative feedback process ultimately causes the GC-LT to be triggered and switched on. Compared with conventional photodiodes, the GC-LT employs photo-thyristor to collect and amplify the photocurrent. This configuration has a high sensitivity to low-level light owing to the regenerative feedback amplification effect of the cross-coupled bipolar transistors.

Since a thyristor can be treated as two cross-coupled bipolar transistors, the photocurrent feedback amplification process in the GC-LT is simulated and the results are illustrated in Fig. 7(a), where i_a is the anode current, i_{ph} is the photocurrent, i_G is the generation current of reverse biased junction J_2, and i_{pd} is the optimized pull-down current of parasitic M_{G1}. β_n and β_p correspond to the photocurrent gains of the cross-coupled n^+pn and pnp^+ transistors, respectively.

TABLE 2. Comparison of the GC-LT with the photodiode, the phototransistors and the avalanche photodiode.

Reference	This work	[21]	[22]	[23]	[24]	[25]	[26]
Device type	GC-LT#	Pinned photodiode*	Conventional phototransistor#	Punchthrough enhanced transistor#	Partially-gated phototransistor#	Heterojunction phototransistor#	Avalanche photodiode#
Pixel size(μm^2)	3×1	2×2	12×12	2.5×2	10×2.5	10×10	10×20
Power supply voltage (V)	4.5	2.0	1.2	1.5	4.0	2.0	8.2
I_{dark} (A)	3×10^{-15}	3×10^{-17}	1.7×10^{-12}	1×10^{-7}	1×10^{-12}	1×10^{-9}	2.6×10^{-15}
Optical gain	8.0 to 6.3	0.74	11.1 to 1	N/A	3.9 to 1	9.24 to 1	228.6
Optical power density range (W/cm^2)	2.5×10^{-6} to 1×10^{-9}	4.5×10^{-4} to N/A	~2.8×10^{-2} to ~1×10^{-8}	5.4×10^{-2} to 3.8×10^{-8}	N/A	1.15×10^{-3} to N/A	N/A

*. *Experimental results.* #.*simulation results.*

It needs to be noted that the adjustment through the sidewall control gate G1 causes the base region of the n^+pn transistor narrower than that of the pnp^+ transistor, resulting in $\beta_n > \beta_p$.

As shown in Fig. 7(a), the anode current can be calculated by,

$$i_a = \left[(i_G + i_{ph})(1+\beta_n) + i_{pd}\right] \cdot (1+\beta_p) \cdot \frac{1}{1-\beta_n\beta_p} \quad (1)$$

At the beginning of the sampling mode, the photocurrent gain β_n and β_p are rather small ($\beta_n \to 0$, $\beta_p \to 0$) because the emitter-base junctions J_1 and J_3 are reverse biased. The anode current can be simplified as,

$$i_a \approx i_G + i_{ph} + i_{pd} \quad (2)$$

Equation (2) indicates that the anode current is the sum of the generated current in the intermediate p-n junction J_2, the photocurrent and the pull-down current when the sampling mode is established. The GC-LT shifts to the diode sampling mode and the amplification effect is relatively weak. With the accumulation of holes in the p-base region, the emitter-base junction J_1 gradually changes to positive bias, resulting in the increase of β_n while β_p is still approximate to zero. The GC-LT changes to the transistor sampling mode, where the n^+pn transistor plays a leading role in photocurrent amplification. The anode current is equivalent to the amplification current of the n^+pn transistor,

$$i_a \approx \left(i_G + i_{ph}\right) \cdot (1+\beta_n) + i_{pd} \quad (3)$$

Then, the emitter-base junction J_3 changes from reverse bias to positive bias with the decrease in the n-base potential, and the photocurrent gain β_p of the pnp^+ transistor increases gradually. The GC-LT enters into the thyristor sampling mode. When $\beta_n\beta_p \to 1$, the anode current $i_a \to \infty$, and then the GC-LT is triggered and switched on.

Fig. 7(b) shows the anode current I_a and the fitting current components according to Eq. (1), when the optical power density is 1×10^{-7} W/cm^2. The dashed lines indicate the fitting current components, where I_{rst} is the post-reset current after *Reset* operation; I_{dio} is the sum of the generated current,

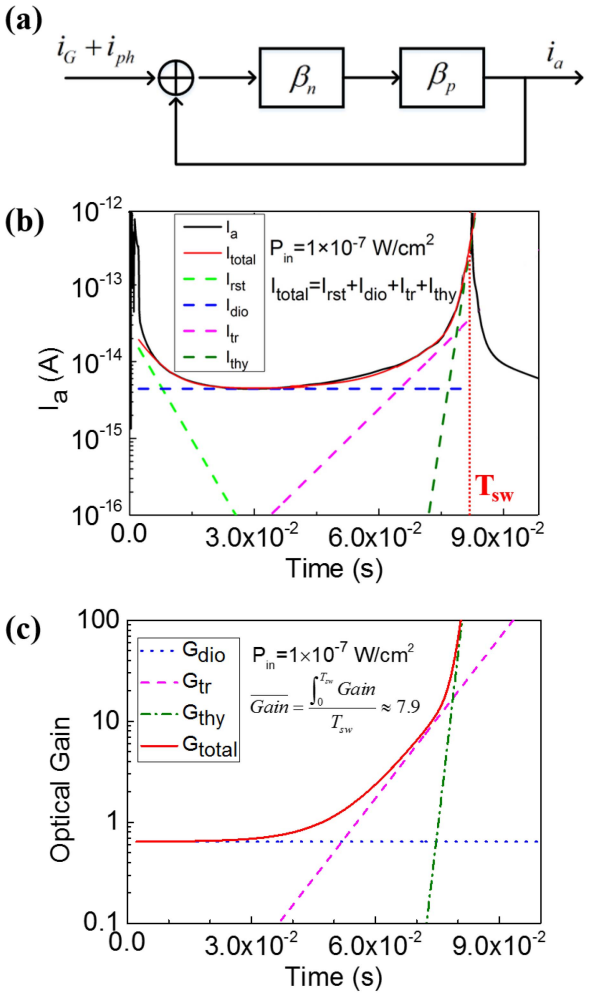

FIGURE 7. The photocurrent feedback amplification process in the GC-LT when the optical power density is 1×10^{-7} W/cm^2. (a) Feedback amplification model, (b) photo-response as anode current I_a and the fitting current components, and (c) optical gain.

the photocurrent and the pull-down current, corresponding to the initial diode sampling mode with $\beta_n \to 0$ and $\beta_p \to 0$. I_{tr} can be considered as the amplified photocurrent in the

n^+pn transistor sampling mode with $\beta_n > 0$, while $\beta_p \to 0$. I_{thy} represents the trigger current in the thyristor sampling mode with $\beta_n\beta_p \to 1$. The sum of the four fitting current components I_{total} is in good agreement with the simulated anode current I_a.

The optical gain is defined as the ratio of the number of electrons collected under illumination to the number of incident photons,

$$Gain = \left(\frac{i_a - i_{dark}}{q}\right) \Big/ \left(\frac{P_{in}}{h\nu}\right) \tag{4}$$

where P_{in} is incident optical power, $h\nu$ is incident photon energy, q is the charge of an electron, and i_{dark} represents the dark current without incident light.

Fig. 7(c) shows the optical gain when the optical power density is 1×10^{-7} W/cm^2. The initial optical gain is about 0.67, which is the typical value of diode sampling with 70% quantum efficiency at 550 nm. The average gain during the whole *Sampling* period is 7.9, about 11.8 times of that in diode sampling mode, representing the average amplification effect on the photocurrent during the total sampling mode.

C. OPTICAL POWER SPECTRUM

Fig. 8(a) shows the photo-response characteristics of anode voltage V_a and anode current I_a at different optical power densities. It is obvious that the time to trigger and switch the detector on has a quantitative relationship with optical power density. The trigger time difference ΔT is normalized to describe the relationship between the switch time and the optical power density. According to Fig. 8(a), the normalized trigger time difference under illumination is,

$$\Delta T = T_0 - T_{sw} \tag{5}$$

where T_0 and T_{sw} are the switch time without and with incident light, respectively.

Fig. 8(b) shows the relationship between the normalized trigger time difference ΔT and the optical power density P_{in}. It shows that ΔT is sensitive to the optical power density ranging from 1×10^{-9} to 2.5×10^{-6} W/cm^2, which means that the dynamic range is about 68 dB. The average optical gain at different optical power densities is also studied. As shown in Fig. 8(c), the optical gain of the GC-LT could still be distributed in 8.0-6.3 under a wide range of optical power density, even with a low-light level of 1×10^{-9} W/cm^2.

The simulated performances are compared in Table 2 with the photodiode, the phototransistors and the avalanche photodiode. The GC-LT has an average optical gain of 8.0-6.3, about one order of magnitude higher than that of the pinned photodiode [21]. The maximum optical gain of the GC-LT is lower than that of the phototransistor, but the maximum optical gain of the phototransistor is obtained under the high optical power density [22]–[25]. More specifically, for the heterojunction phototransistor, the maximum optical gain is 11.1 when the optical power density is 2.8×10^{-2} W/cm^{-2}.

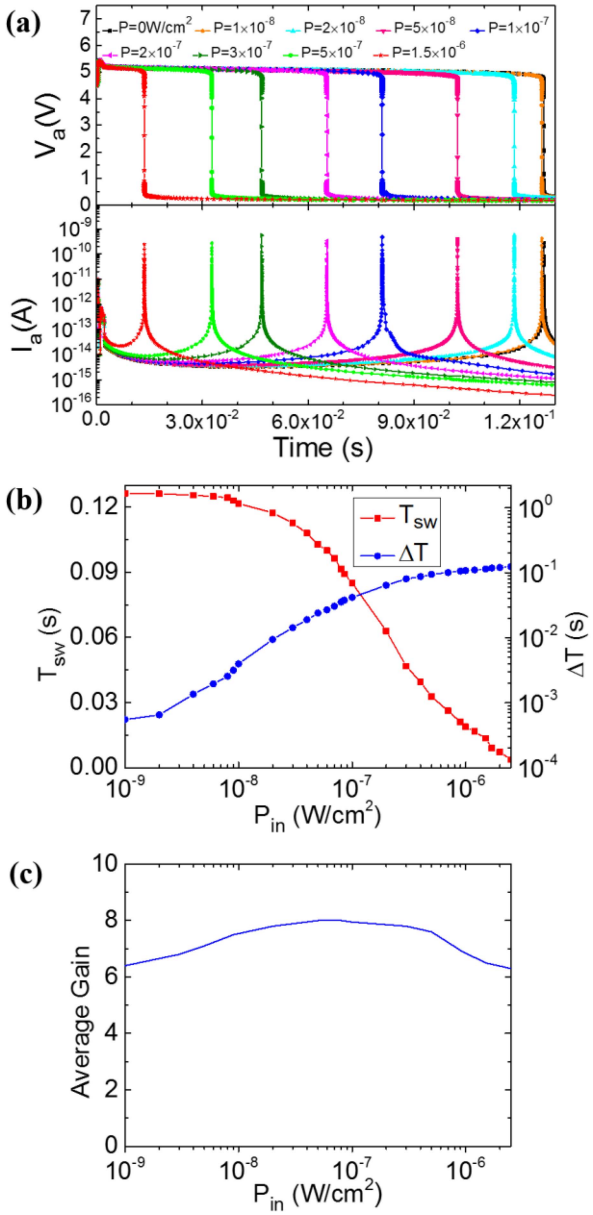

FIGURE 8. Photo-response characteristics of the GC-LT at different optical power densities. (a) Photo-response as anode voltage V_a and anode current I_a of the GC-LT operating at $V_{G1} = 0.6$ V, (b) the relationship between the trigger time T_{sw} and the optical power density P_{in}, and (c) the average optical gain.

However, its optical gain drops to only 1.0 when the optical power density decreases to 1×10^{-8} W/cm^{-2} [22]. In contrast, the optical gain of the GC-LT could still be distributed in 8.0-6.3 under a wide range of optical power density, even with a low-light level of 1×10^{-9} W/cm^2. Moreover, it is worth noting that the dark current of the GC-LT is approximately 3 fA, which is 3-7 orders of magnitude lower than phototransistors [22]–[25]. Although the GC-LT has an inferior low-light level detection capability to APDs [26], it surpasses APDs on circuit overhead, operation

voltage and noise, allowing it to be used as imaging arrays that are difficult for APDs [7], [8].

IV. CONCLUSION

A novel gate-controlled lateral thyristor structure and a thyristor photodetector circuit are proposed for low-light level detection. A super-off *Reset* operation method is developed to bias the GC-LT over the switching point quickly and allow the photodetector circuit to be operated in a monotonic dynamic multi-sampling mode to improve the sensitivity to low-light detection. Numerical simulation is performed to investigate the electrical characteristics of the GC-LT and demonstrates the operation mechanism. The trigger time of the photodetector is sensitive to the low-light level between 1×10^{-9} and 2.5×10^{-6} W/cm^2 with an average optical gain of 8.0-6.3. All these indicate that the GC-LT could be a promising candidate for the low-light level detection.

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