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Demonstration of Low-Temperature Fine-Pitch Cu/SiO_2 Hybrid Bonding by Au Passivation

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ABSTRACT Fine pitch Cu/SiO_2 hybrid bonding has been successfully demonstrated at a low temperature of 120 °C, a breakthrough, using Au passivation method in this work. To explore the bonding mechanism of passivation structures for hybrid bonding in details, Cu-Cu direct bonding with Au passivation on both wafer-level and chip-level has been discussed, including analyses of AFM, SAT, TEM, electrical measurements, and reliability test. Cu/SiO_2 hybrid bonding with the fine pitch structure with stable electrical performance can be achieved at low bonding temperature under an atmospheric environment. Accordingly, this Au passivation scheme for Cu/SiO_2 hybrid bonding with excellent bonding quality, low thermal budget, and high reliability shows a great feasibility for the 3D IC and heterogenous integration applications.

INDEX TERMS 3D integration, Cu bonding, wafer-level bonding, flip-chip bonding, Au passivation.

I. INTRODUCTION

Since the first transistor has been invented to flourish the semiconductor industry, the development of the transistors has followed Moore's law [1], leading to continuous advancement in performance of integrated circuits (ICs). However, miniaturization of the transistors rapidly increases the complexity of interconnection layouts, which causes the serious RC delay and mainly challenges performance of ICs when the feature size approaches to sub-10-nm regime. Three-dimensional integrated circuit (3D IC) is considered as the promising technology to further reduce form factor, interconnection length, power consumption, and RC delay of ICs [2]–[3].

Bonding technology is one of the key techniques to realize 3D stacking. There are three bonding methods developed to meet the requirements for interconnect with finer pitch, including solid-liquid interdiffusion (SLID) bonding, anisotropic conductive film/paste (ACF/ACP), and metal/dielectric hybrid bonding, as shown in Fig. 1. SLID with underfill materials is the most commonly used solution, while intermetallic compounds (IMC) are formed during the SLID bonding process, leading to challenges of reliability, structural stress, and electromigration [4]–[6]. In addition, squeeze out of solders (Sn or In) and the filling capacity of underfill material results in challenges to further shrink the pitch between bonding bumps, as shown in Fig. 1(a). ACF, composed of conductive particles (CPs) and the polymer dielectric film, is another method to realize bonding of the fine pitch structure. As shown in Fig. 1(b), the CPs as the interconnection materials can connect wafers or chips during the bonding process, and the polymer dielectric film can isolate the bonded pads. However, electrical properties and reliability of ACF structures are challenged by the concentration of CPs [7]–[9].

Without the shortcomings of SLID and ACF, metal/dielectric hybrid bonding (Fig. 1(c)) is considered as the most promising technology to realize integration circuits with high interconnection density and high performance. In addition, Cu as metal interconnect for hybrid bonding can provide excellent electrical resistance, anti-electromigration, and thermal conductivity. However, oxidization of Cu induces a requirement of strict bonding conditions, such as high bonding temperature and high vacuum environment,

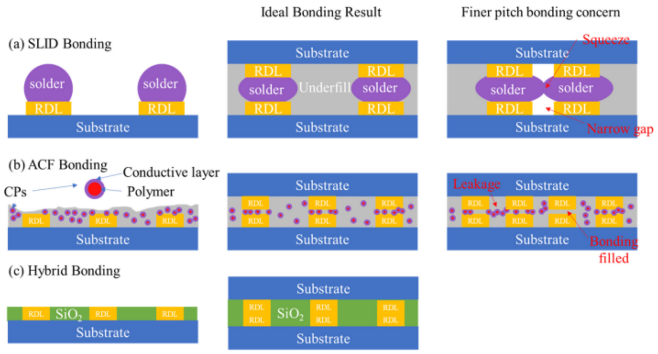

FIGURE 1. Schematic illustration of current bonding technologies for interconnect with finer pitch, (a) SLID bonding; (b) ACF bonding; (c) hybrid bonding.

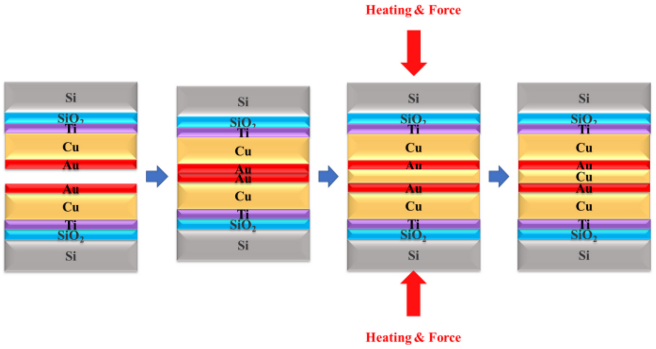

FIGURE 2. Schematic illustration of Cu-to-Cu bonding with the passivation layer.

which causes the problems of thermal budget, structural reliability, wafer warpage for the bonding structures [10]. Therefore, the method to reduce Cu-Cu bonding temperature is important to improve the feasibility of Cu/dielectric hybrid bonding for the applications in 3D IC, involving high bandwidth memory (HBM), quantum compute, fifth-generation mobile networks (5G) and artificial intelligence (AI) chips.

In the previous studies, the scheme using metal passivation was proposed to reduce bonding temperature of Cu-Cu bonding [11]–[13]. In [11], 10 nm Ti deposited on the Cu surface as passivation was first applied in the Cu-Cu bonding structure. The Ti layer can protect inner Cu from the oxidation and reduce the bonding temperature to 180 °C, while the oxidation of Ti was observed to increase the specific contact resistance of the bonding structure. Based on this research, Pd as metal passivation was investigated to further improve Cu-Cu bonding [12]. With a 10 nm Pd passivation layer on Cu surface, Cu-Cu bonding can be successfully implemented at 150 °C, and the specific contact resistance of the structure can be reduced from 10^{-4} Ω.cm^2 (with Ti passivation) to 10^{-7} Ω.cm^2. Nevertheless, Pd was still unable to resist oxidation completely during the thermal process [14], limiting the electrical performance and reliability of the bonding structure. In addition, this wafer-level bond scheme requires a long bonding duration at high vacuum condition. Bonding conditions for short duration or low vacuum are still desired for 3D and heterogeneous integration.

In this paper, Au as the passivation material has been successfully demonstrated for both wafer-level and chip-level Cu-Cu bonding, which can completely protect Cu surface from the oxidation and reduce the bonding temperature to 120 °C. The schematic of this bonding method is shown in Fig. 2. Meanwhile, SiO_2 bonding with the pretreatment of diluted HF solution has been discussed. Accordingly, Cu/SiO_2 hybrid structure with the fine pitch of 5 μm has been successfully bonded at 120 °C under the atmosphere environment by using the Au passivation method.

II. BONDING MECHANISM INVESTIGATION

A. SIO_2 BONDING WITH DHF PRETREATMENT

SiO_2 as the thin-organic dielectric layer is commonly used in the semiconductor industry. In addition, SiO_2 is compatible with the damascene process for the fabrication of Cu RDL. Thus, SiO_2 is selected as dielectric for hybrid bonding in this study. Traditional SiO_2-SiO_2 bonding requires a high bonding temperature over 1000 °C to achieve the promising bonding quality [15]–[16]. However, high temperature will lead to the run-out misalignment and cause the stress issue during the hybrid bonding process. Therefore, a low temperature bonding process for SiO_2 is highly demanded by the semiconductor industry.

Accordingly, the plasma pretreatment has been proposed to enable SiO_2-SiO_2 bonding at a low bonding temperature [16]–[18]. Because an O atom is coordinated by two Si atoms in the molecular structure of SiO_2 and an N atom is coordinated by three Si atoms in the molecular structure of Si_3N_4, the O atom can be substituted by the N atom during the N_2 plasma pretreatment. Thus, reconstruction and stabilization of the metastable oxynitride bonding layer can occur to form the surface with more dangling bonds and lower bonding energy [19]. However, for the hybrid bonding structure, the plasma pretreatment may damage the surface of metal region, and this method needs a high vacuum environment of 10^{-5} torr.

In addition to the plasma pretreatment, the diluted hydrofluoric acid (DHF) solution has been studied for the SiO_2 bonding process [20]–[22]. After rinsing by DI water, the surface of SiO_2 can terminate with Si-OH groups, as shown in Fig. 3, because the HF solution can react with Si-O-Si and Si-OH groups to form Si-OH, Si-F groups, and dangling defects on the surface [21]. During the bonding process, Si-OH and Si-F groups on the bonding surfaces can contact with each other and produce the strong hydrogen bonds. The bonding energy of hydrogen bonds between hydrogen and fluorine is 60-170kJ/mol, which is comparable with covalent bond [22]. Furthermore, two Si-OH groups can form a Si-O-Si covalent bond even at room temperature, providing low temperature SiO_2-SiO_2 bonding. In the previous studies, it has been demonstrated that 1% concentrations of

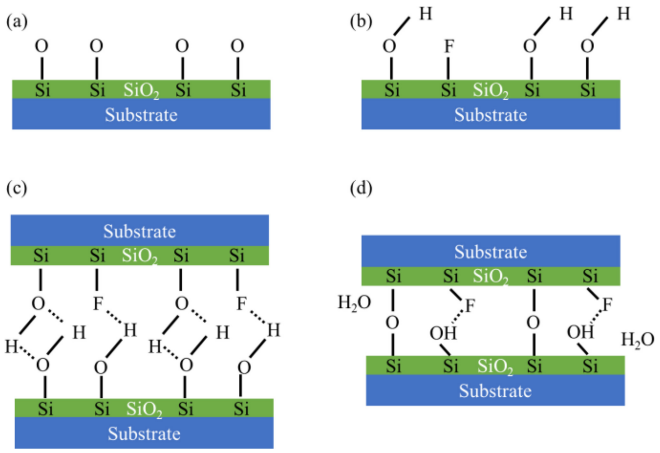

FIGURE 3. Mechanism of SiO_2 bonding with DHF pretreatment.

HF in DHF solution can enable SiO_2-SiO_2 bonding with the higher bonding strength [22]. For the hybrid bonding structure, the DHF solution can not only improve the SiO_2 bonding process, but also remove the native oxides on the metal region. Thus, the DHF solution has been used for Cu/SiO_2 bonding in this study.

B. CU-CU DIRECT BONDING WITH AU PASSIVATION LAYER

To achieve Cu-Cu bonding in the passivation scheme, Cu atoms have to diffuse through the passivation layer. In previous studies, the grain boundary diffusion coefficient of Cu in Au (1.2×10^{-16} m^2/s) is much larger than that of Au in Cu (1.2×10^{-17} m^2/s) at 220 °C [23]–[24]. On the basis of these studies, the corresponding diffusion lengths have been calculated by Dai, indicating that the diffusion length of Cu in Au (4.8 nm) is longer than that of Au in Cu (0.40 nm) and Cu in Cu (0.30 nm) at 300 °C for 1 hour [25]. Accordingly, the Au passivation layer can further assist diffusion of Cu atoms at the low bonding temperature, which is beneficial for the passivation scheme.

An annealing experiment was designed and performed to simulate the bonding process, and the inter-diffusion behavior in the process has been observed by Auger electron spectroscopy (AES). In the Auger depth profiles, before annealing, Cu was protected from oxidation by depositing a 10 nm Au layer on the surface, as shown in Fig. 4(a). After nitrogen annealing at 400 °C for 1 hour, Cu atoms can easily diffuse through the 10 nm Au layer, as shown in Fig. 4(b), verifying the two outstanding properties of the designed bonding structure in this experiment: the unimpeded Cu diffusion in the Au layer, and the ability of Au layer to protect the inner Cu layer from oxidation.

The flatness of the bonding surface has a great impact on the bonding quality. Thus, surface roughness of the samples before bonding is characterized by the atomic force microscope (AFM) analysis, as shown in Table 1 and Fig. 5(a), indicating that surface roughness of Cu with Au passivation

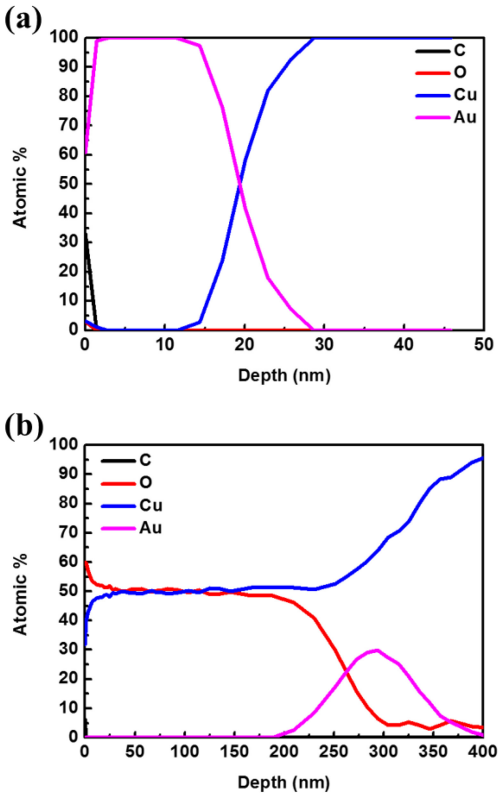

FIGURE 4. Auger depth profiles of the Cu layer with Au passivation. (a) Before heating. (b) After heating at 400 °C for 60 min.

TABLE 1. The surface roughness of bonding surface with different passivation thickness.

Au thickness (nm)	*Ra (nm)*	*Rq (nm)*	*Z-range (nm)*
0	2.55	3.18	28.00
5	2.36	2.94	26.10
10	1.92	2.41	21.80
20	2.42	3.01	24.90

layer is smoother than that of only Cu layer. In Fig. 5 (b), the mean roughness (Ra) of the bare Cu sample is 2.55 nm, while Ra of the samples with 5 nm, 10 nm, and 20 nm Au passivation can be reduced to 2.36 nm, 1.92 nm and 2.42 nm, respectively. Meanwhile, the values of root mean square roughness (RMS, Rq) of the samples follow the same trend as Ra. With 10 nm Au passivation on the Cu surface, the flattest surface can be obtained, and the 10 nm thickness of Au is accordingly used as passivation in this study.

III. LOW TEMPERATURE CU-CU BONDING DEMONSTRATION AND BONDING INTERFACE ANALYSIS

A. WAFER-LEVEL BONDING AND BONDING INTERFACE ANALYSIS

The illustration of the designed structure in Fig. 1 includes SiO_2/Ti/Cu/Au layers on a 4-inch Si wafer. After the RCA cleaning process, 500 nm SiO_2 layer was deposited

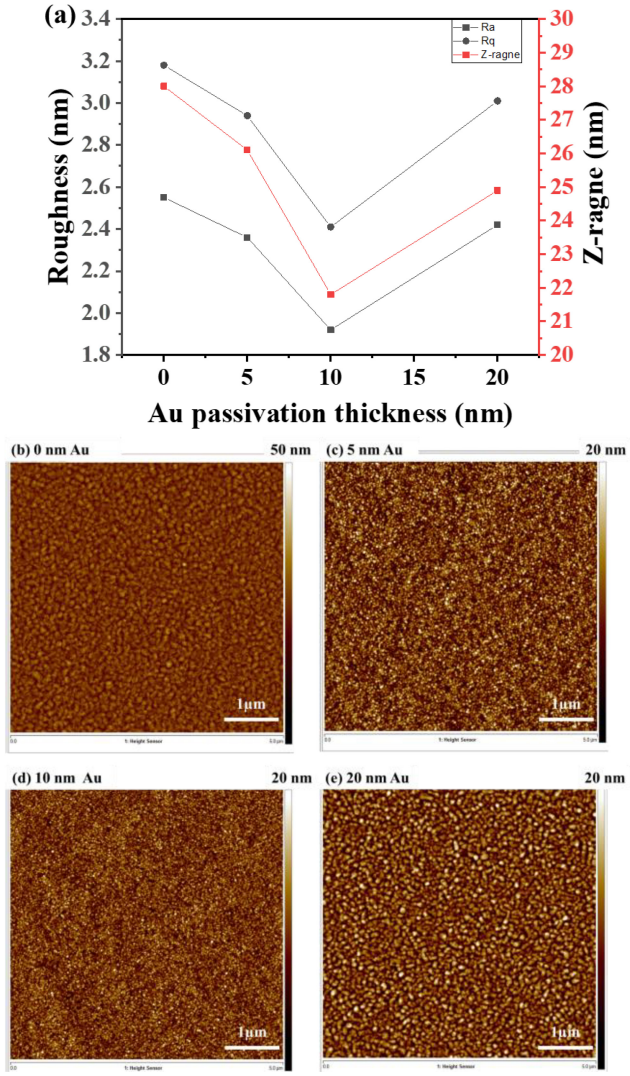

FIGURE 5. RMS/Ra Roughness of controlled Cu samples depending on the thickness of the Au passivation layer.

by thermal oxidation. For the metallic process, 25 nm Ti layer, 300 nm Cu layer and 10 nm Au layer were deposited by E-gun evaporation consecutively as the adhesion layer, re-distribution layer (RDL), and passivation layer. Due to the protection of Au, a wet-process to pre-clean the bonded surface before the TCB process can be bypassed. Next, wafer-level bonding of the structures was performed at 120 °C for 50 minutes under the applied pressure of 1.27 MPa and a low vacuum environment of 10^{-2} Torr. The Scanning Acoustic Tomography (SAT) analysis has been performed to verify the uniformity of the wafer-level bonding results, as shown in Fig. 6(a), where the darker area in the SAT image represents the better bonding quality. Although some white bubbles are observed due to particles inevitably generated during fabrication in the laboratory, most of the bonding area is dark in the image, meaning that successful bonding can uniformly distribute over the wafer. In addition, the scanning electron

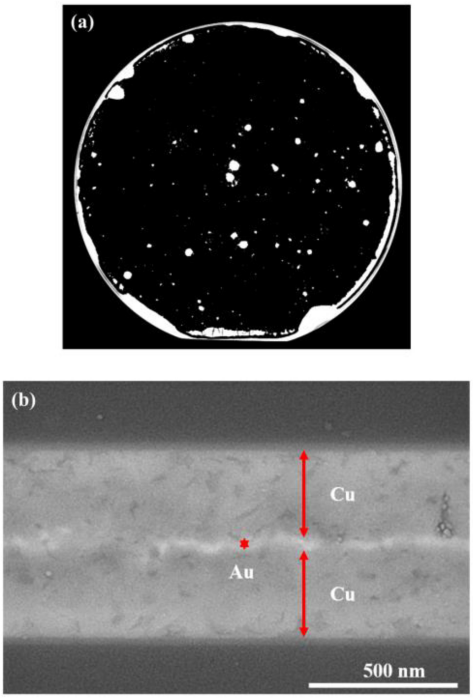

FIGURE 6. Wafer-level bonding at 120 °C. (a) SAT analysis. (b) SEM image.

microscope (SEM) image of the bonding result is shown in Fig. 6(b). There is no void observed at the bonding interface, providing another clear evidence for the good bonding quality.

Both transmission electron microscope (TEM) and energy dispersive X-ray spectroscopy (EDX) analysis are further performed in this study to analyze the inter-diffusion behavior of metal after the TCB process, as shown in Fig. 7. According to the EDX analysis, Cu atoms can gradually diffuse through the Au-rich layer into the bonding surface and achieve the bonding process. As a result, a continuous Cu-rich layer is obviously observed at the interface.

After demonstrating the bonding process at wafer level, the bonded samples were diced into 1 × 1 cm^2, followed by conducting the pulling test. As shown in Fig. 8, under the 16.4 kgf pulling strength, the sample was broken up at the interface of fixed glue rather than the bonding interface, which means that the real bonding strength is higher than the measured value.

B. CHIP-LEVEL BONDING AND ELECTRICAL PERFORMANCE

After verifying the quality and the morphology of bonding surface, both the electrical performance measurement and the reliability test are further performed to examine the bonding feasibility. The modified kelvin structure for specific contact resistance and daisy chain structure for series resistance were designed and fabricated by the lift-off process at wafer level, followed by dicing wafer into 5 × 5 mm^2 for top dies and 10 × 10 mm^2 for bottom dies. As shown in Table 2, with a 20 kg applied bonding force, the chip-level bonding

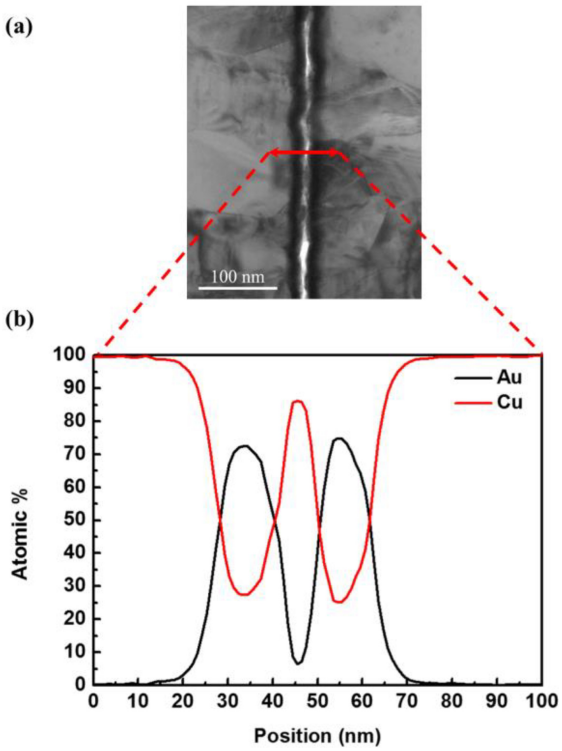

FIGURE 7. (a) TEM image of Cu-Cu bonding with Au passivation and the EDX scanning position. (b) Corresponding EDX analysis.

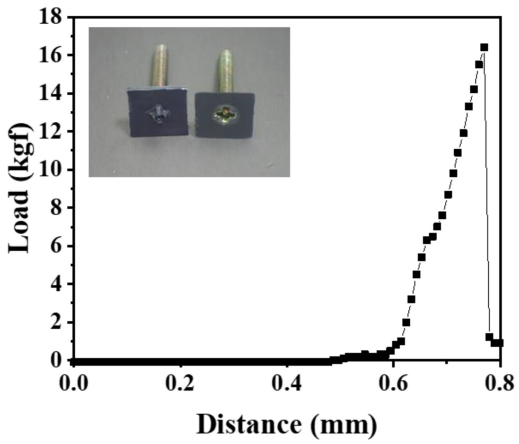

FIGURE 8. Result of the Pulling test for the samples with 1 × 1 cm^2 size.

TABLE 2. Design of experiment and bonding results.

	15 sec	*60 sec*	*90 sec*
100°C	×	×	△
120°C	×	△	✓
150°C	✓	✓	✓

× : Fail △: Partially bonded ✓ : Successfully bonded

structure has been successfully bonded under ultra-low thermal budget (at 120 °C for 90 s and at 150 °C for 15 s) and the atmospheric environment by the flip-chip bonder.

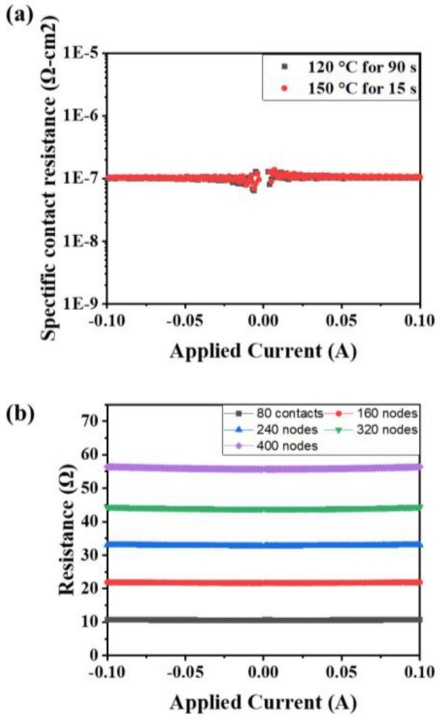

FIGURE 9. The electrical performance of (a) modified kelvin structure and (b) daisy chain structure. The bonding condition of daisy chain structure is 150 °C for 15 s.

The electrical measurement of the modified kelvin structure is shown in Fig. 9(a). The specific contact resistance of the chip-level bonding structure can maintain about 1×10^{-7} Ω.cm^2, which is better than the bonding structures with Pd and Ti passivation proposed in previous works. In addition, the daisy chain structure is designed with 400 contact nodes and 20 × 20μm^2 bonded area of each node. The electrical measurement of the daisy chain structure is shown in Fig. 9(b), indicating the bonding structure can provide the stable series resistance and uniform bonding yield.

Furthermore, thermal cycling test (TCT) and unbiased highly accelerated stress test (unbiased HAST) were performed in the severe environment to validate the reliability of this bonding scheme. The TCT, representing the ability to withstand mechanical stress induced by thermal variation of the bonding structure, applies the standard of JESD22-A104B, which is determined by applying extremely low and high temperatures from −55 °C to 125 °C. After TCT for 250, 500, 1,000, and 2,000 loops, as shown in Fig. 10(a), the bonded structure can maintain a specific contact resistance around 1×10^{-7} Ω.cm^2 with negligible deterioration. Besides, the unbiased HAST was performed to determine the reliability of the bonding structure under specific thermal and humidity environment. Following the standard of JESD22-A118, the high temperature of 85 °C and high relative humidity of 85% was applied to the samples. As shown in Fig. 10(b), the specific contact resistance of the

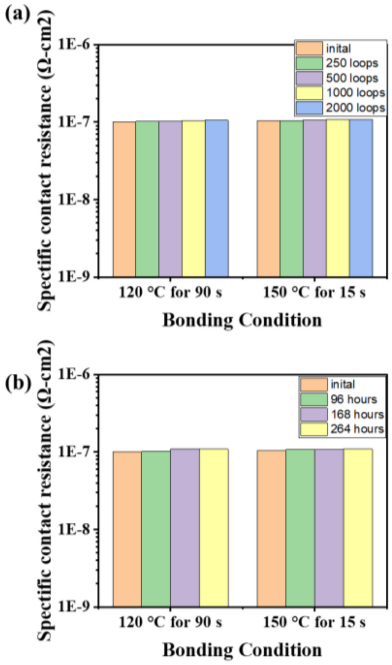

FIGURE 10. The electrical performance and reliability test of modified kelvin structure: (a) TCT, (b) unbiased HAST.

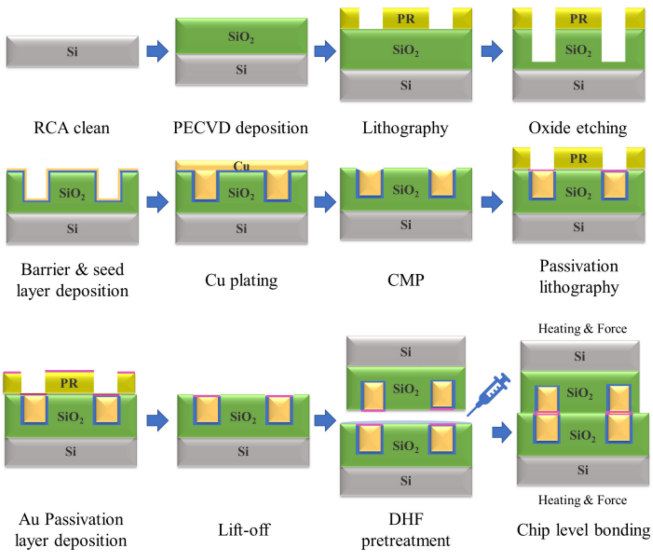

FIGURE 11. Process flow of hybrid bonding.

bonding structure has only very slight change after unbiased HAST for 96, 168, and 264 hours, verifying tolerance of the structure against thermal and moisture erosion.

IV. CU/SIO2 HYBRID BONDING PROCESS DEMONSTRATION

A. PROCESS FLOW

After low temperature Cu-Cu direct bonding with Au passivation and SiO_2-SiO_2 bonding has been discussed in details, the Cu/SiO_2 hybrid bonding structure sample were fabricated by a standard single damascene process with 8-inch wafer. As shown in Fig. 11, after RCA clean, a layer of

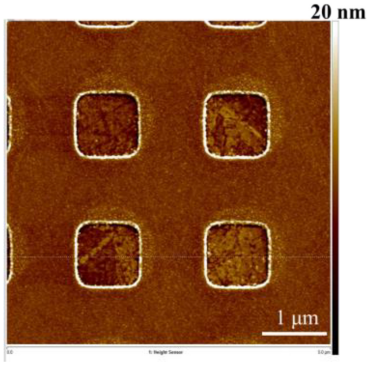

FIGURE 12. The AFM result of hybrid bonding surface.

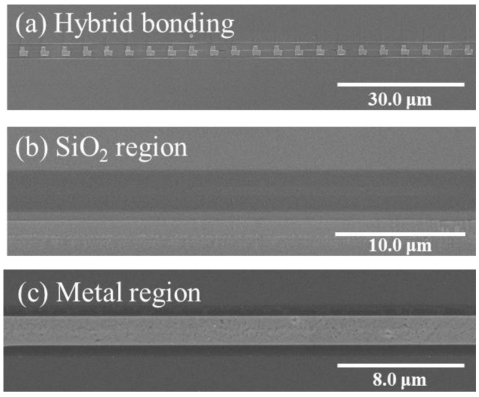

FIGURE 13. SEM images of bonding interface (a)hybrid region; (b)SiO_2 region; (c)metal region.

1 μm SiO_2 was deposited on the wafer by PECVD, followed by a lithography process to define the metal region. Next, the deposition of barrier layer and seed layer, as well as electrical planting Cu and chemical-mechanical polish were performed. Finally, through the lift-off process, the 10-nm Au passivation layer was deposited using E-gun evaporation on the Cu surface. Fig. 12 shows that the RMS of surface roughness is about 2 nm. The wafers were singulated into 5×5 mm^2 for top chips and 15×15 mm^2 for bottom chips. After alignment in the flip-chip bonder, the 10 μL DHF solution was dripped on the bottom chip, and then the structures were bonded with a 20kg bonding force at 120℃ for 180s under the atmospheric environment.

B. BONDING RESULT

The bonded structures were sent for analyses of interface inspection and electrical measurement. As shown in Fig. 13(a), the successful hybrid bonding structure with the fine pitch of 5 μm can be observed in the SEM images. In Fig. 13(b) and (c), the bonding interface of both SiO_2 and metal region disappears, indicating the excellent bonding results. Meanwhile, the measured shear strength of 2.65 MPa of this bonding structure can further verify the good bonding quality. In addition, as shown in Fig. 14, electrical performance of the hybrid bonding structure

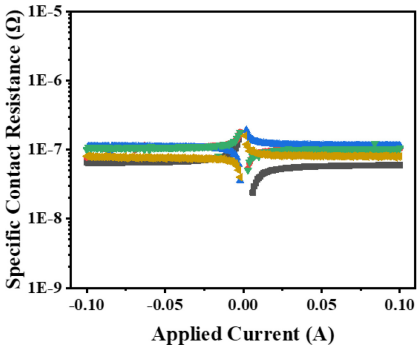

FIGURE 14. **The electrical performance of modified kelvin structures.**

TABLE 3. **Comparison of different low temperature bonding method.**

	[11]	*[12]*	*This work*	
Bonding technology	Ti Passivation	Pd Passivation	Au Passivation	Au Passivation/ SiO_2 hybrid
	W2W	W2W	W2W/C2C	C2C
Bonding temperature (°C)	180	150	120	120
Bonding Environment	10^{-5} Torr	10^{-5} Torr	10^{-2} Torr	Atmosphere
Specific contact resistance (Ω·cm²)	7×10^{-4}	2×10^{-7}	1×10^{-7}(C2C)	1×10^{-7}

shows a specific contact resistance around 10^{-8} Ω.cm^2, which also validates the high bonding quality and feasibility.

V. CONCLUSION

In this paper, low temperature Cu/SiO_2 hybrid bonding with the fine pitch of 5 μm has been successfully demonstrated using the Au passivation method. To investigate Au passivation for low temperature bonding in details, Cu direct bonding with Au passivation is bonded at both wafer-level and chip-level. Accordingly, the inter-diffusion mechanism between the Cu layer and Au passivation layer is confirmed at low temperature (120°C). Furthermore, it is shown that in addition to protect Cu from oxidation, a 10 nm Au passivation layer can greatly improve the surface roughness. The good and uniform bonding quality is verified by the analyses of SAT, SEM, TEM, and the pulling test. Meanwhile, chip-level bonding using this Au passivation scheme can be achieved under ultra-low thermal budget (120 °C for 90 s, 150 °C for 15 s). All the limited-testing samples pass the reliability test of 2,000 TCT or 264 hours unbiased HAST.

In summary, compared with other passivation materials, as shown in Table 3, Au passivation can provide the lowest bonding temperature and the best electrical performance for the Cu bonding structure. Based on these results, Cu/SiO_2 hybrid bonding with Au passivation can be achieved at 120 °C for 180 s, and the excellent bonding results have been validated by the analyses of SEM and electrical performance. Therefore, with its ultra-low thermal budget, better bonding quality, and reliability assessments, Au passivation bonding method for low temperature Cu/SiO_2 hybrid bonding is the promising choice for heterogeneous integration and advanced packaging applications.

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