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A Novel Split-Gate-Trench MOSFET Integrated With Normal Gate and Built-In Channel Diode

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ABSTRACT A novel split-gate-trench MOSFET integrated with normal gate and built-in channel diode (BCD) in the same trench is proposed and simulated with Sentaurus TCAD in this paper. Compared with the conventional SGT MOSFET (C-SGT MOS) and conventional SGT MOSFET with built-in channel diode (CBCD-SGT MOS), the proposed MOSFET exhibits superior performances, such as smaller turn-on voltage and lower reverse recovery charges when working in the third quadrant, and reduced gate charge and gate-to-drain charge when working in the first quadrant. With the negligible degradation of the on-state resistance, significant improvements in the figures of merit can be obtained. What's more, obvious uniform forward and reverse conduction current distribution of proposed structure is observed compared to CBCD-SGT MOS although two types of devices are both featuring BCD structure, which could increase the robustness of device when working in high-power and high-frequency applications.

INDEX TERMS Split-gate-trench MOSFET, built-in channel diode, reverse recovery characteristics, figure of merit, current distribution.

I. INTRODUCTION

In power electronic systems, power semiconductor devices play a gradual important role in handling high voltage, high-current, high-frequency signals, and large-power management [1]. Compared with conventional vertical double-diffused MOSFET (VDMOS), split-gate-trench MOSFET (SGT MOS) has a better compromise between on-state resistance (R_{on}) and breakdown voltage (BV), and is more appropriate in high-frequency switching circuits [2]–[6]. In the inverter and boost converter applications, the source-to-drain parasitic body diode is always used for freewheeling [7]–[9]. However, the bipolar characteristics of body diode mean that device must result in poor reverse recovery performances due to excess minority carries in the drift region, thus causing extra power losses. Over the last few decades, a series of approaches have been proposed to work out this problem [10]–[19]. For example, anti-paralleled external diode is the most popular method but it causes extra output capacitance and parasitic inductance [10], [11]. Carrier lifetime control technology can improve the turn-off characteristics but causes degradations of R_{on} and drain to source leakage current (I_{DS}) [12], [13]. Another solution is integrating Schottky diode but it causes larger degradations of I_{DS}, integration level, and high temperature characteristics [14]–[19]. Recently, a novel technology for power MOSFET with built-in channel diode (BCD) has been proposed to solve such a problem [20]–[23]. O. Häberlen and his team proposed a conventional SGT MOS with BCD (CBCD-SGT) which is arranged one BCD and three normal cells alternately, as shown in Fig. 1 (b) [24], to improve the DC-DC conversion efficiency. However, this structure has the problem that the current is not uniform in the forward and reverse conduction.

Based on that conception, a novel SGT MOS integrated with normal gate and BCD in the same trench (PBCD-SGT MOS) is proposed in this paper, as shown in Fig. 1 (c). On

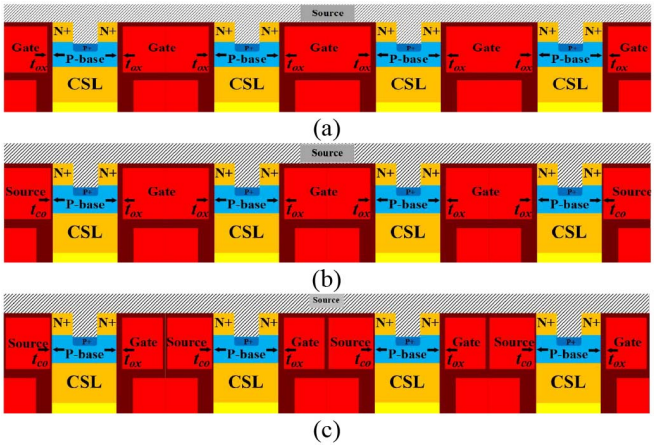

FIGURE 1. Schematic cross sections of (a) C-SGT MOS, (b) CBCD-SGT MOS and (c) PBCD-SGT MOS.

the one hand, the PBCD-SGT MOS has better conduction current distribution compared with CBCD-SGT MOS, which ensures the robustness of the device. On the other hand, superior forward and reverse performances are observed when the device working in the third quadrant due to the unipolar conduction of BCD, such as the decrease of the turn-on voltage, reverse recovery charge and reverse recovery time with the thinner dummy gate oxide thickness (t_{co}). In addition, the decreased capacitance and improved figures of merit ($R_{on} \times Q_G$ and $R_{on} \times Q_{GD}$) can be obtained when the device working as a MOSFET, which indicates the proposed structure has significant advantages in high-frequency applications.

II. DEVICES STRUCTURE AND PARAMETERS

The schematic cross sections of the conventional SGT MOS (C-SGT MOS), CBCD-SGT MOS and PBCD-SGT MOS are shown in Fig. 1. The thickness and doping concentration of the epitaxial layer are 4.5 μm and 5×10^{15} cm^{-3}. Consequently, 3 μm trench depth, 0.6 μm trench width, and 0.33 μm field oxide layer thickness is chosen to obtain *BV* higher than 60 V. The mesa width between each trench is 0.5 μm, resulting in a single cell pitch of 1.7 μm. The t_{co} is thinner than the 75 nm gate oxide thickness (t_{ox}), to achieve a lower BCD turn-on voltage. Other detailed parameters are shown in Table 1. Furthermore, the detailed fabrication processes of the proposed structure are shown in Fig. 2.

For simulating the static and dynamic performances of SGT MOSFET, there are some models that should be included in TCAD tools, such as the doping dependence for Shockley-Read-Hall recombination and auger recombination, neglected interface states between Si and SiO_2, and avalanche model of van Overstraeten – de Man for *BV* simulation, which is based on:

$$\alpha(F_{ava}) = \gamma a \exp(-\frac{\gamma b}{F_{ava}}) \quad (1)$$

TABLE 1. Device parameters for simulation.

Device Parameters	C-SGT MOS	CBCD-SGT MOS	PBCD-SGT MOS	Unit
Unit cell pitch	1.7	1.7	1.7	μm
Epitaxy thickness	4.5	4.5	4.5	μm
Epitaxy doping	5×10^{15}	5×10^{15}	5×10^{15}	cm^{-3}
Trench depth	3	3	3	μm
Trench width	0.575	0.575	0.575	μm
t_{ox}	50	50	50	nm
t_{co}	-	10 ~ 50	10 ~ 50	nm
P-base depth	0.5	0.5	0.5	μm
P-base doping	5×10^{17}	5×10^{17}	5×10^{17}	cm^{-3}
CSL depth	0.4	0.4	0.4	μm
CSL doping	1×10^{16}	1×10^{16}	1×10^{16}	cm^{-3}
P-plus doping	5×10^{18}	5×10^{18}	5×10^{18}	cm^{-3}
N-plus doping	1×10^{19}	1×10^{19}	1×10^{19}	cm^{-3}

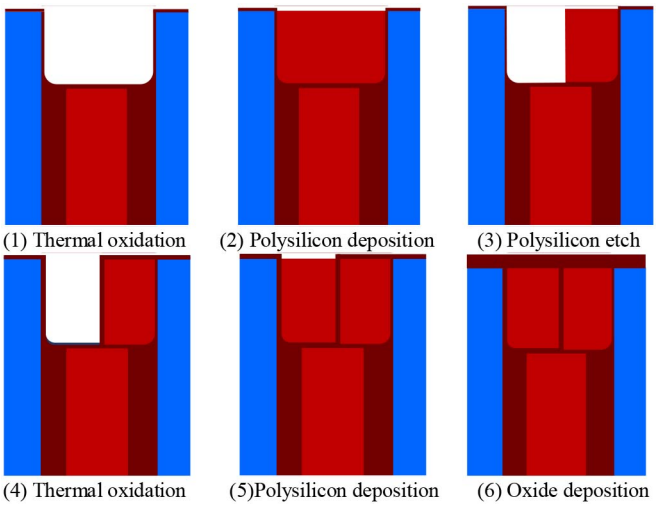

FIGURE 2. Process flow for the PBCD-SGT MOS.

TABLE 2. Coefficients for van Overstraeten–de Man model.

Name	Electrons	Holes	Unit
a	7.03×10^{5}	1.582×10^{6}	cm^{-1}
b	1.231×10^{6}	2.036×10^{6}	V/cm
HbarOmega	0.063	0.063	eV

with:

$$\gamma = \frac{\tanh\left(\frac{\hbar\omega_{op}}{2kT_0}\right)}{\tanh\left(\frac{\hbar\omega_{op}}{2kT}\right)} \quad (2)$$

The factor with the optical phonon energy $\hbar\omega_{op}$ expresses the temperature dependence of the phonon gas against which carriers are accelerated. The coefficients *a*, *b*, and $\hbar\omega_{op}$, as measured by van Overstraeten and de Man are given in Table 2, which is used to express the electron- and hole-impact ionization coefficients [25]. The area factor in +z direction is set as 1.47×10^7 μm to obtain active area of

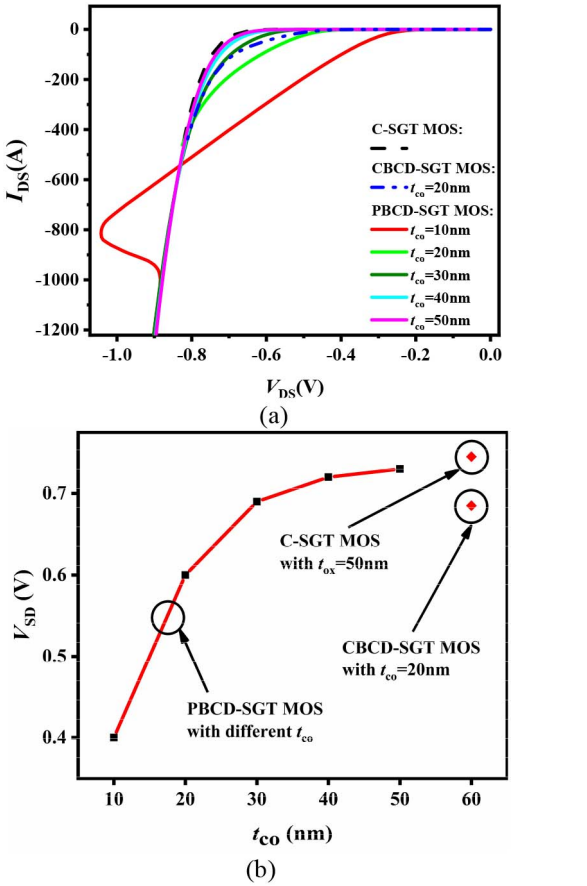

FIGURE 3. (a) The reverse conduction characteristics of the C-SGT MOS, CBCD-SGT MOS, and PBCD-SGT MOS, (b) The forward on-state voltages of the SGT MOSFETs with different t_{co} at I_{SD} = 100A/cm^2.

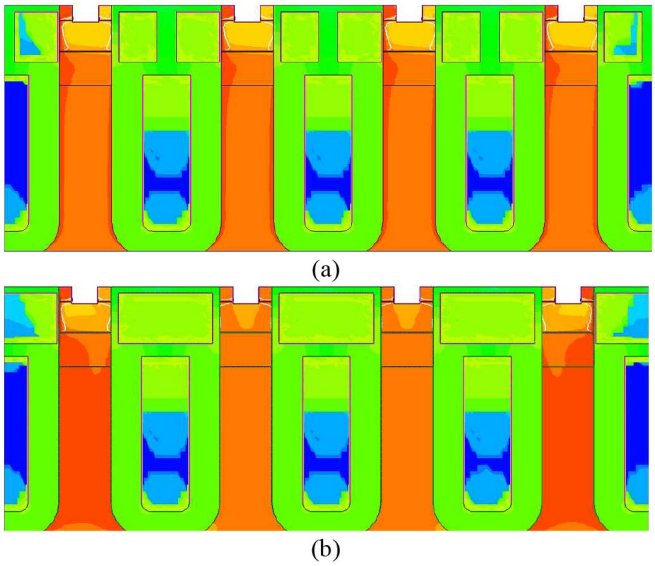

FIGURE 4. The total current density contribution of (a) PBCD-SGT MOS and (b) CBCD-SGT MOS when the reverse conduction current is 100 A/cm^2.

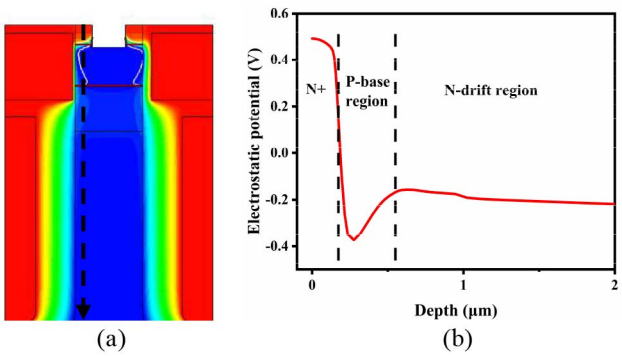

FIGURE 5. (a) Potential distribution of proposed MOSFET with t_{co} = 20 nm at I_{SD} = 100 A/cm^2, (b) Potential profile along the dotted line.

1 cm^2 for all structures when the linear cell topology is considered.

III. RESULTS AND DISCUSSIONS

The third quadrant reverse conduction characteristics of the C-SGT MOS, CBCD-SGT MOS and PBCD-SGT MOS at $V_{GS} = -5$ V are plotted in Fig. 3 (a). The C-SGT MOS turns on at about 0.72 V, the CBCD-SGT MOS with $t_{co} = 20$ nm turns on at about 0.61 V, whereas PBCD-SGT MOS with $t_{co} = 20$ nm turns on at about 0.48 V, which is much lower than that of the former two. Meanwhile, smaller reverse turn-on voltage of proposed MOSFET can be obtained with the thinner dummy gate oxide, such as 0.33 V at $t_{co} = 10$ nm and 0.71 V at $t_{co} = 60$ nm. While an approximately linear region is observed in the reverse conduction characteristic, indicating the unipolar conduction of the MOSFETs with BCD. The proposed structure reaches $I_{SD} = 100$ A/cm^2 at 0.4, 0.6, 0.69, 0.72 and 0.73 V forward on-state voltage (V_F) with $t_{co} = 10$, 20, 30, 40 and 50 nm, respectively, as shown in Fig. 3(b). It should be noted that, although the smaller reverse turn-on voltage is characterized in the device with $t_{co} = 10$ nm, the snap-back in I-V curve, as shown in Fig. 3(a), may cause current non-uniformities among the paralleled cells [20]. The relatively larger t_{co} (20 nm) can eliminate the snap-back feature, so 20 nm thickness of dummy gate oxide is selected to research in this paper, unless otherwise specified.

Compared with CBCD-SGT MOS, PBCD-SGT MOS has higher density of BCD and more uniform reverse conduction current distribution, as shown in Fig. 4, resulting in a lower turn-on voltage and higher robustness with the same thickness of dummy gate.

The electrostatic potential along the dotted arrow of the proposed MOSFET with BCD in Fig. 5 (a) is extracted in Fig. 5(b). Although dummy gate and P-base are both contacted to source electrode, the former has the same electrostatic potential as N+ region, which is much higher than that of P-base region when the device working in the third quadrant, resulting in a stronger inversion layer formed with a smaller positive V_D. This inversion layer provides a current path from source to drain. The processes of reverse turn-on can be divided into two steps: (a) the MOS-channel

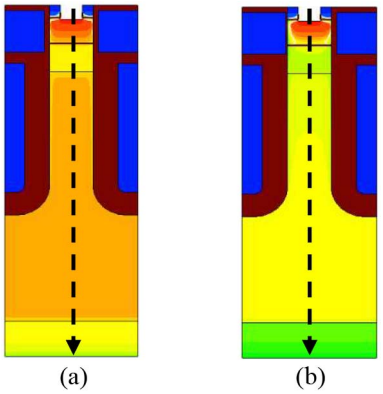

FIGURE 6. Hole density distributions of MOSFET (a) with and (b) without BCD structure at $I_{SD} = 100A/cm^2$.

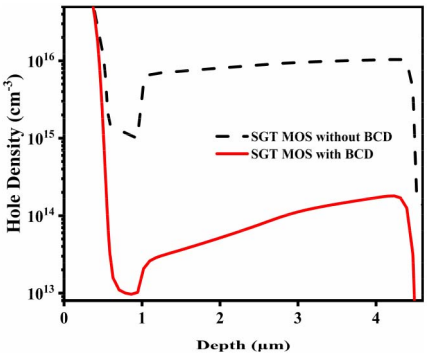

FIGURE 7. Hole density profiles along the depth of the studied MOSFETs at $I_{SD} = 100\ A/cm^2$.

diode unipolar turns on during low positive V_{SD} (about $0.3 \sim 0.6$ V) applied on dummy gate; (b) both of the body diode and BCD turn on when V_{SD} reaches about 0.7 V.

Fig. 6 shows hole density at $I_{SD} = 100$ A/cm^2 of the SGT MOSFETs with and without BCD structure. The minority carrier (hole) concentration profiles along the dotted arrow are illustrated in Fig. 7. The hole density of the MOSFET with BCD structure is about 5×10^{13} cm^{-3}, which is much lower than 7×10^{13} cm^{-3} hole density of the MOSFET without BCD, indicating a unipolar conduction in the reverse conduction process.

The static parameters are also investigated as shown in Fig. 8, such as BV and output characteristic curves. The C-SGT MOS, CBCD-SGT MOS and PBCD-SGT MOS have similar BVs, because the changes in the trench top structure don't influence the depletion distribution. The R_{on} extracted from output characteristic curves of three types of MOSFETs at $I_{DS} = 100$ A/cm^2 are 0.77, 0.8 and 0.84 mΩ·cm^2, respectively, with less than 10% differences. The components of total on-state resistance for the three types of devices are listed in Fig. 9. It is shown that the drift region resistance occupies the most part of the on-state resistance (above 90%) for these three cases, and the slight increase of R_{ON} for the CBCD-MOS and PBCD-MOS, as compared to the C-SGT MOS, is attributed to the enhanced channel and accumulation resistance, due to the sacrifice of channel density. The total

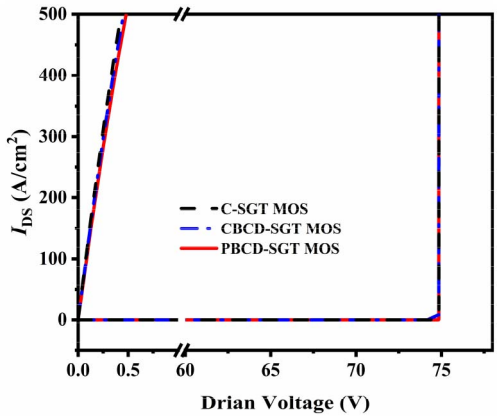

FIGURE 8. Breakdown voltage and output characteristic curves of C-SGT MOS, CBCD-SGT MOS and PBCD-SFT MOS, respectively.

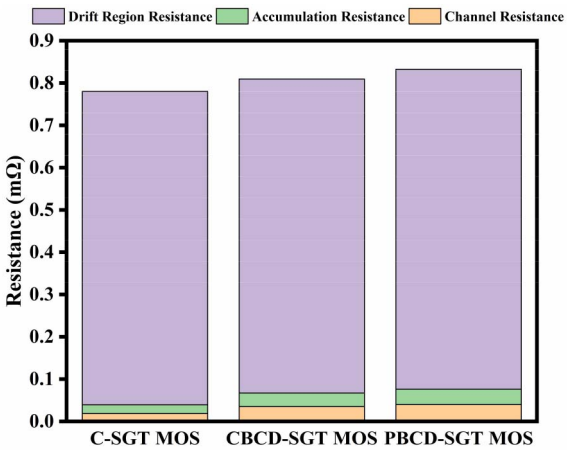

FIGURE 9. The components of the on-resistance of the three types of devices.

current density during forward conduction of three types of devices are shown in Fig. 10. In BCD-SGT MOSFETs, the reverse currents go across dummy gate channel and then spread to CSL more sufficiently because of relative high doping concentration, resulting in the decrease of R_{on}. Meanwhile, PBCD-SGT MOS has an obvious uniform current distribution than CBCD-SGT MOS due to the changes of the top structure, which optimizes the robustness of the devices. What's more, a lower saturation current caused by the reasons mentioned above could be seen as an advantage of strengthening short-circuit ruggedness [26].

The gate charge characteristics curves and corresponding test circuit are illustrated in Fig. 11. The values of gate charge (Q_G) extracted at $V_{GS} = 10$ V of C-SGT MOS, CBCD-SGT MOS and PBCD-SGT MOS are 496.4, 336.3 and 296 nC/cm^2, whereas the gate-to-drain charges (Q_{GD}) are 50, 40 and 20 nC/cm^2, respectively. The Q_G and Q_{GD} of PBCD-SGT MOS are improved by 12% and 50% than those of CBCD-SGT MOS, which indicates the proposed structure is more suitable for high-frequency applications although the two types of devices both have BCD structure. As a consequence, the figure of merit $R_{on} \times Q_G$ and $R_{on} \times Q_{GD}$

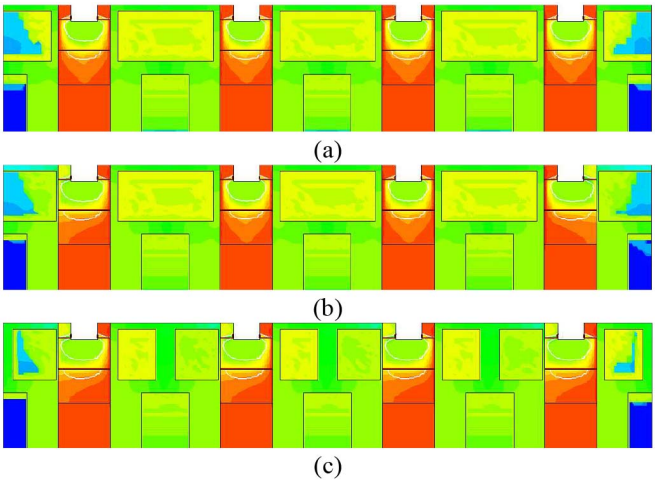

FIGURE 10. Forward conduction current density distribution of (a) C-SGT MOS; (b) CBCD-SGT MOS; (c) PBCD-SGT MOS, respectively, at I_{DS} = 100 A/cm^2.

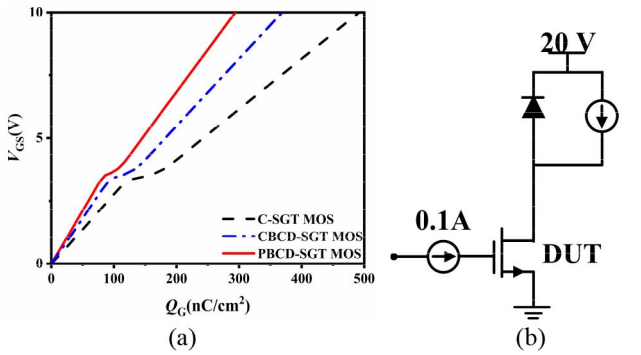

FIGURE 11. (a) Gate charge characteristic curves of C-SGT MOS, CBCD-SGT MOS and PBCD-SGT MOS, and (b) corresponding testing circuit.

TABLE 3. Performances comparison.

Device Parameters	C-SGT MOSFET	CBCD-SGT MOSFET	PBCD-SGT MOSFET	Unit
V_F	0.745	0.685	0.6	V
BV	74	74	74	V
R_{on}	0.77	0.8	0.84	mΩ·cm^2
Q_G	496.4	336.3	296	nC/cm^2
Q_{GD}	50	40	20	nC/cm^2
$R_{on} \times Q_G$	421.9	293	225	mΩ·nC
$R_{on} \times Q_{GD}$	42.5	32	15.2	mΩ·nc
C_{ISS}	35	27	19	nf/cm^2
C_{RSS}	110	70	30	pf/cm^2

of proposed structure are enhanced by a factor of 1.87 and 2.97 than that of C-SGT MOS. Other characteristics of the devices are settled in Table 3.

Fig. 12 shows the *C-V* characteristics curves of three types of MOSFET. The input capacitance (C_{ISS}) of C-SGT, CBCD-SGT and PBCD-SGT MOSFETs are 35 nF/cm^2, 27 nF/cm^2 and 19 nF/cm^2, whereas reverse capacitance (C_{RSS}) are

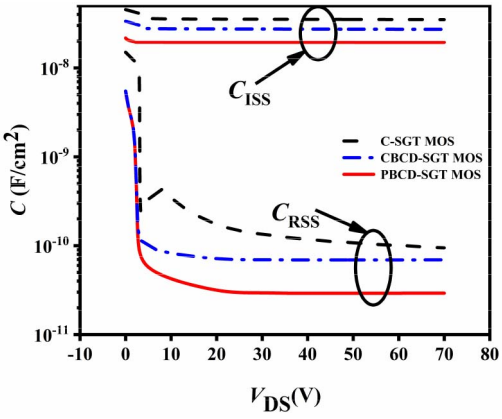

FIGURE 12. C_{Iss} and C_{Rss} curves of C-SGT MOS, CBCD-SGT MOS and PBCD-SGT MOS.

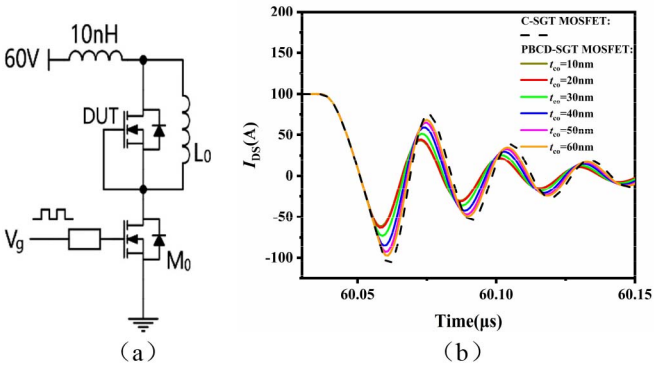

FIGURE 13. (a) Test circuit configuration for the reverse recovery characteristics, where 60V SGT-MOS is used as M_0, (b) simulated reverse recovery characteristic curves of conventional and proposed devices with different t_{CO}. and (c) reverse recovery characteristics of C-SGT MOS, CBCD-SGT MOS, and PBCD-SGT MOS with different turn-off current.

110 pF/cm^2, 70 pF/cm^2 and 30 pF/cm^2, respectively. Lower C_{ISS} and C_{RSS} mean the shorter charge and discharge time, which is important for high-frequency circuits.

The reverse recovery test circuit and characteristic curves are shown in Figs. 13 (a) and (b). In the test circuit, the C-SGT MOS, CBCD-SGT MOS and PBCD-SGT MOS are used as the device under test (DUT), respectively. Whereas another C-SGT MOS is used as the bottom device (M_0). The test processes can be divided into three steps: (1) the inductance L_0 keeps charging when the M_0 turns on with high-level square wave signal of gate; (2) square wave signal turns into low level, M_0 shuts off and the parasitic body diode and/or BCD of DUT turns on; (3) square wave signal turns into high level again, parasitic body diode and/or BCD shuts down and reverse recovery characteristic curves of conventional and proposed devices with different t_{co} can be extracted, as shown in Fig. 10(b). Because of unipolar conduction and thinner dummy oxide thickness, the MOSFET with BCD structure eliminates excess carrier extraction process to achieve superior reverse recovery time (t_{rr}) and peak reverse recovery current (I_{RRM}). The I_{RRM} of the parasitic body diode and BCD are 102.5 A/cm^2

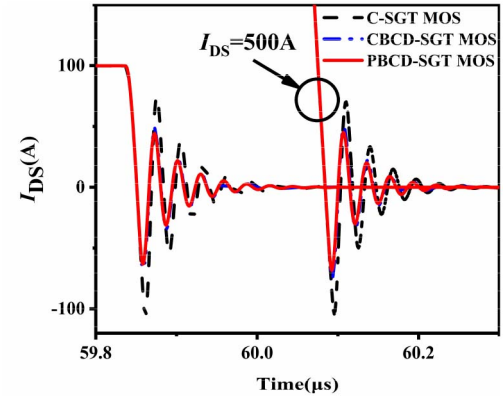

FIGURE 14. Reverse recovery characteristics of C-SGT MOS, CBCD-SGT MOS, and PBCD-SGT MOS with different turn-off current.

and 61.3 A/cm^2, respectively. The I_{RRM} of proposed structure has smaller value with thinner dummy gate thickness, such as 46.94 A/cm^2 at $t_{co} = 10$ nm and 71.61 A/cm^2 at $t_{co} = 60$ nm, which is attributed to earlier establishment of inversion layer. These advantages are also applicable to the case of high turn-off current, such as $I_{SD} = 500$ A/cm^2, as shown in Fig. 14. The plasma in the epitaxial layer of C-SGT MOS must be removed when the diode turns off, leading to higher Q_{RR} [27]. The unipolar conduction of PBCD-SGT MOSFET does not exist such questions. According to calculation, the Q_{RR} of C-SGT and MOSFET with BCD structure are 1.28 A/cm^2 and 0.65 A/cm^2, improved nearly 50 %.

The CBCD-SGT MOS and PBCD-SGT MOS are both given out to achieve BCD structures performances. The former can be fabricated with no excessive accurate equipment due to farther distance between dummy gate and MOSFET gate, whereas the latter has uniform cell structures but needs a higher technology level. Significantly, the latter structure has better forward and reverse current distribution consistency, which contributes to high-power and high-frequency applications. Compared with CBCD-SGT MOS, the PBCD-SGT MOS also shows a series of advantages, such as lower Q_{rr}, turn-on voltage of reverse recovery, current distributions when working as a diode, and lower Q_{rr}, better figure of merit, input and reverse capacitances when working as a MOSFET.

IV. CONCLUSION

A novel SGT MOSFET integrated BCD and gate polysilicon in the same trench is proposed and researched through TCAD simulations in this paper. Compared with C-SGT MOS and CBCD-SGT MOS, the proposed MOSFET exhibits superior performances by virtue of unipolar conduction due to dummy gate and thinner t_{co} when working in the third quadrant, such as reduced V_F, I_{RRM}, and Q_{rr}, which solves the problem of weak reverse recovery ability of SGT MOSFET. Meanwhile, when the device works as an MOSFET, the Q_G, Q_{GD}, C_{ISS} and C_{RSS} are largely decreased. Along with the insignificant changes in BV, V_{th} and R_{on}, the outstanding figure of merits can be obtained, resulting in improving the efficiency of SGT MOSFET. Although both the CBCD-SGT MOS and PBCD-SGT MOS have BCD structure, the latter shows more uniform forward and reverse conduction current distributions, better electrical parameters, and less energy loss, which are good for the device working in high-power and high-frequency applications.

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