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Non-Pad-Based in Situ In-Operando CDM ESD Protection Using Internally Distributed Network

MENGFU DI, CHENG LI, ZIJIN PAN, AND ALBERT WANG (Fellow, IEEE)

Department of Electrical and Computer Engineering, University of California at Riverside, Riverside, CA 92521, USA

CORRESPONDING AUTHOR: M. DI (e-mail: mdi002@ucr.edu)

This is an extended paper to a report at IEEE EDTM2021 [8].

ABSTRACT Charged device model (CDM) electrostatic discharge (ESD) protection is an emerging design challenge to ICs at advanced technology nodes. It was recently reported that the traditional pad-based CDM ESD protection methods are fundamentally faulty, which causes uncertainties in CDM ESD protection designs, testing and failure analysis. Re-thinking of on-chip CDM ESD protection becomes imperative for complex ICs implemented in advanced technologies. This paper reports a disruptive CDM ESD protection method utilizing non-pad-based internally-distributed ESD protection network as a robust in situ in-operando CDM ESD protection solution. The proposed internal-distributed CDM ESD protection mesh network can be realized using interposer or through-silicon-via (TSV) ESD protection structures to achieve local 3D CDM ESD protection via heterogeneous integration. The new concept was validated using an internal-CDM-protected oscillator IC implemented in a foundry 45nm silicon-on-insulator (SOI) technology.

INDEX TERMS CDM, ESD, internal distributed, TSV, interposer.

I. INTRODUCTION

Performance and reliability are the two corner stone attributes required for ICs, which often require subtle design trade-off in practical chip designs. On-chip ESD protection remains a major IC reliability design challenge [1]–[3]. Particularly, CDM ESD failures are increasingly harmful to large complex chips in advanced IC technologies and CDM ESD protection design becomes very challenging at beyond-28nm technology nodes [4]. For decades, the classic pad-based on-chip ESD protection scheme has been widely used for almost all ESD protection designs, which work effectively to protect ICs against the external-oriented "from-external-to-internal" types of ESD events, such as human body model (HBM), machine model (MM) and International Electrotechnical Commission (IEC) ESD test models [1]. Nevertheless, while the pad-based ESD protection method has been the default solution for CDM ESD protection, its effectiveness is becoming increasingly questionable due to the fact that CDM ESD protection remains notoriously uncertain and unreliable in designs, testing and field failure analysis, in spite of all CDM ESD protection design efforts [5]–[7]. Recently, it is reported that conventional pad-based CDM ESD protection method may be theoretically wrong because CDM ESD phenomena are internal-oriented and "from-internal-to-external" in nature [7]. In addition, traditional in-plane side-by-side ESD protection designs not only consume significant Si die area, but also are extremely layout-unfriendly, particularly for large and high-pin-count chips in beyond-28nm IC technologies [4]. This paper, extended from a conference report [8], discusses a disruptively new non-pad-based internally distributed CDM ESD protection concept, which is demonstrated in an oscillator IC designed and fabricated in a 45nm SOI CMOS process. Design of novel interposer and through-silicon-via (TSV) based internal-distributed CDM ESD protection mesh networks are also presented.

II. INTERNAL-DISTRIBUTED CDM ESD PROTECTION

It is important to understand that CDM ESD phenomena are entirely different from HBM ESD events in nature. In principle, HBM ESD is an external-oriented event where electrostatic charges stored in a human body can be discharged into an IC, causing ESD damage to the chip. Correspondingly,

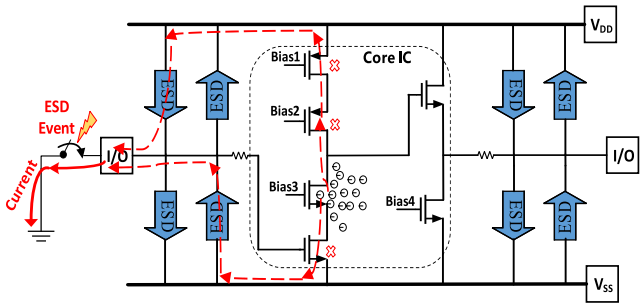

FIGURE 1. Illustration of traditional pad-based CDM ESD protection scheme where internally stored charges may cause internal CDM ESD failures (marked X) when discharging from their internal locations to external GND through ESD devices at pads.

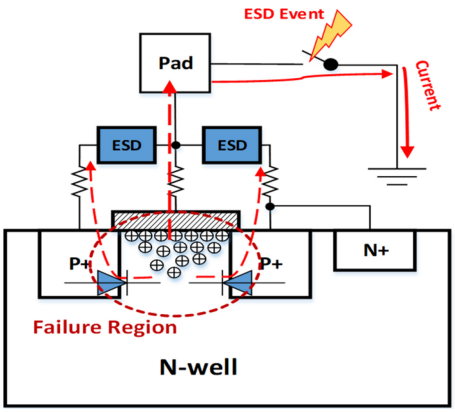

FIGURE 2. An exemplary case shows possible internal CDM ESD failure at SD junction or gate in a pad-based CDM ESD protection scenario.

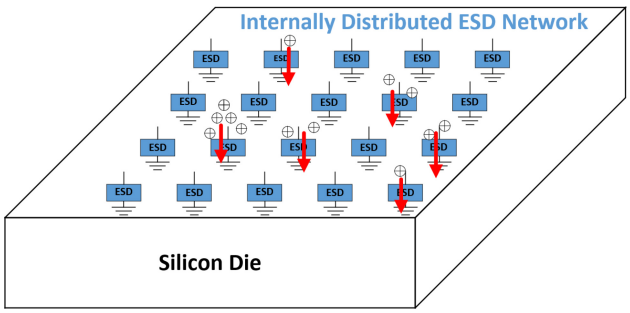

FIGURE 3. Illustration of the new internal-distributed CDM ESD protection method for ICs.

the classic pad-based on-chip ESD protection follows a "from-external-to-internal" protocol, meaning, properly designed ESD protection devices are connected to each pad, which will be triggered by an incident ESD transient and provides a conduction path from the pad to ground (GND) to shunt the incoming HBM ESD pulse, hence protecting the IC from ESD damage. Essentially, a pad-connected ESD protection device serves as a "guard" at the "door" to prevent any alien electrostatic charges (i.e., the intruders) from getting into the IC die. This ESD protection principle works nicely for all external-oriented ESD events, such as HBM, MM and IEC ESD events. In the contrary, a CDM ESD event is an internal-oriented phenomenon where electrostatic charges are introduced into an IC part via various ways during its full lifespan, such as triboelectric generation or field induction, and the static charges created can be stored inside an IC die in random and distributed manners, anywhere and being time variant. It is this "anytime anywhere" feature that makes CDM ESD phenomena completely different from HBM ESD events, which, theoretically, disqualifies the classic pad-based ESD protection method from offering CDM ESD protection. Fig. 1 illustrates the conventional pad-based CDM ESD protection scheme where the ESD protection devices at pads are supposedly to provide ESD protection against CDM ESD transients. Unfortunately, even if a perfect pad-based ESD protection network exists on a chip, during an CDM ESD event, since the internally stored electrostatic charges are randomly located in a distributed way, these static charges must find their routes from where they stay to selected pad(s) to be discharged into GND. Obviously, as the stored electrostatic charges find their way out, they have to run through an IC core following an "from-internal-to-external" protocol, and apparently, it is entirely possible that internal CDM ESD failures (voltage or current breakdown) may occur even if the pad-based ESD protection devices function perfectly in ESD discharging [7]. Fig. 2 depicts another possible CDM ESD failure case where substantial electrostatic charges are stored locally around a large MOSFET and some static charges will inevitably run through an S/D junction or a Gate along any ESD discharging path, resulting in internal CDM ESD failure regardless of the pad-based ESD protection network. Moreover, the industrial standard field-induction CDM (FICDM) testing method is an over-simplified short-time accelerated charge induction technique, which cannot truthfully model the real-world CDM ESD charging and storing procedures (i.e., random distribution across a chip), hence, the true CDM discharging phenomenon, therefore adding another factor to the uncertainty of CDM ESD failures in design, testing and field application phases [6]. Therefore, the classic pad-based CDM ESD protection method is believed to be fundamentally faulty [7].

Understanding that electrostatic charges are introduced to an IC anytime and can be stored inside the IC randomly in a distributed manner, a new non-pad-based internally distributed CDM ESD protection technique is devised for *in situ in-operando* ESD protection on a chip [8]. As depicted conceptually in Fig. 3 illustrates the new concept of internally distributed CDM ESD protection mesh network to deal with the nature of internal charge distribution, which is addressed by a unique Smart Partitioning technique that can intelligently partition the IC die according to circuit functions, layout floor plan, as well as device properties and sizes. The internal-distributed CDM ESD protection mesh comprises smaller-sized ESD protection devices, designed and embedded inside the IC die, which are placed at selected internal nodes per the smart portioning protocol according to the internal/local CDM charge distribution. Therefore, as electrostatic charges are generated and accumulated internally and locally, and when they locally reach to a given local

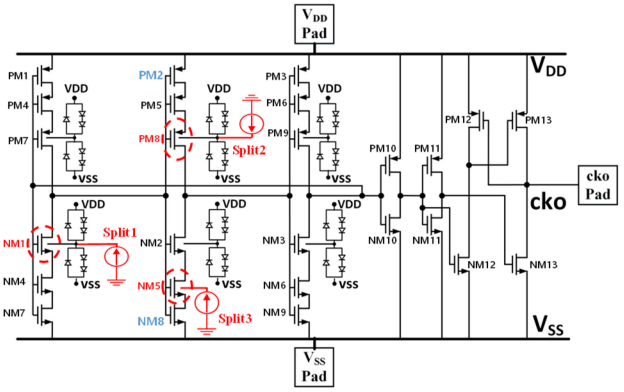

FIGURE 4. **A 3-stage oscillator IC designed in a 45nm SOI CMOS where the large MOSFETs (NM1, NM2, NM3, PM7, PM8 & PM9) likely hold a large number of static charges locally. An internally distributed CDM ESD mesh is designed with smaller ESD protection devices connected to selected internal nodes according to smart partitioning. There are no pad-based ESD protection devices on the chip. CDM ESD simulation has three splits reflecting varying internal charge distribution and different CDM zapping source locations: Split-1 for NM1, Split-2 for PM8 and Split-3 for NM5.**

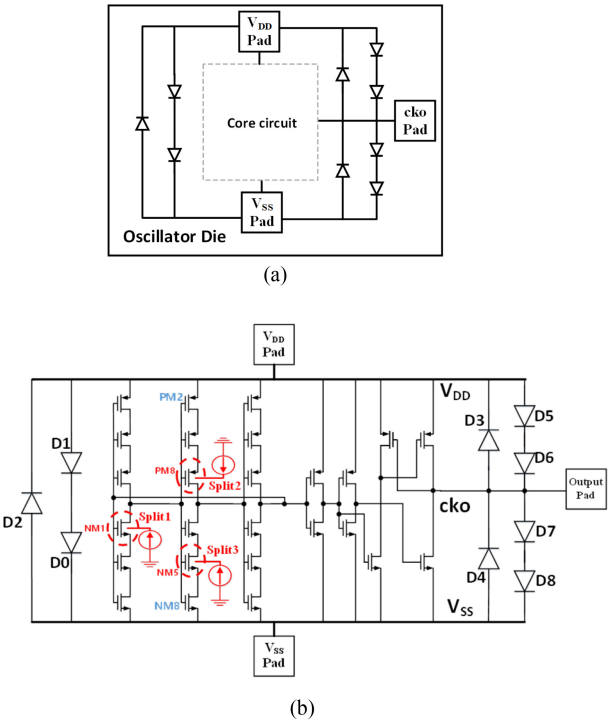

FIGURE 5. **A traditional pad-based CDM ESD protection scheme for the same oscillator IC shown in Fig. 4 as a comparison: (a) diagram for full-chip ESD protection network, and (b) oscillator schematic. The same three splits are simulated: Split-1 for NM1, Split-2 for PM8 and Split-3 for NM5.**

potential threshold (corresponding to a certain amount of static charges), the internal/local ESD protection device will be triggered off to form a low-R conduction path to a local GND, therefore, the electrostatic charges will be discharged locally without having to collectively flow through the internal die to find their ways to GND for ESD discharging. Therefore, the new internally distributed ESD protection mesh can provide adequate whole-chip CDM ESD protection in a *in situ in-operando* fashion. Consequently, the new internal-distributed CDM ESD protection mesh network can effectively address the "from-internal-to-external" CDM ESD phenomena that could not be handled by any traditional pad-based ESD protection methods. It is worth noting that, due to internal and dynamic charge distribution, substantially smaller ESD protection devices may suffice to handle the same level of CDM ESD transient compared to larger ESD protection devices needed in a traditional pad-based ESD protection scheme. This translates into reduced layout size consumed by ESD protection structures.

The new internally distributed CDM ESD protection technique was first validated by chip level simulation using a CDM-protected 3-stage oscillator IC designed in foundry 45nm SOI CMOS technology. Fig. 4 shows the schematic for the 3-stage oscillator IC where six large MOSFET devices (NM1, NM2, NM3, PM7, PM8 and PM9) are identified as the main storage bins of the internal electrostatic charges on the chip, reflecting varying internal static charge distribution. Per the smart partitioning rule, smaller-sized internal/local ESD protection structures will be placed at the internal circuit nodes associated with these large MOSFETs. The internal ESD protection structures used in this work are anti-parallel ESD protection diodes that form the internally distributed CDM ESD protection mesh network. For comparison, Fig. 5 shows a traditional pad-based CDM ESD protection network for the same oscillator IC using same ESD protection diodes of larger size. The CDM ESD design target is 500V CDM (failure current I_{t2}~10A), which requires the ESD diode being 360μm wide (finger width) for the pad-based ESD design. It is worth to note that, since an internal ESD protection device only needs to handle much smaller amount of locally accumulated static charges that is a small fraction of the total amount of electrostatic charges expected for the whole chip for the same ESD protection level, these internal ESD protection devices are much smaller than that of pad-based ESD protection structures. Accordingly, for the new internal-distributed CDM ESD protection mesh, the internal ESD protection diode features a smaller size of 60μm in width, hence, dramatically reducing the ESD-induced design overhead.

SPICE ESD circuit simulation was conducted for the two CDM ESD protected oscillator IC cases shown in Fig. 4 and Fig. 5 using a new near-real-world CDM ESD discharging circuit model and simulation method recently proposed to overcome the problem of FICDM ESD model [7]. Fig. 4 depicts the CDM ESD simulation deck that features a new non-pad-based internal-distributed CDM ESD protection mesh network comprising internal CDM ESD diodes connected to the large charge storage devices, NM1, NM2, NM3, PM7, PM8 and PM9. Fig. 5 shows the comparison case featuring traditional pad-based CDM ESD protection network. For both cases, the IC dies are pre-charged before CDM ESD discharging. Three CDM ESD discharging splits were studied in CDM ESD simulation to reflect the nature of varying internal static charge distribution, hence CDM

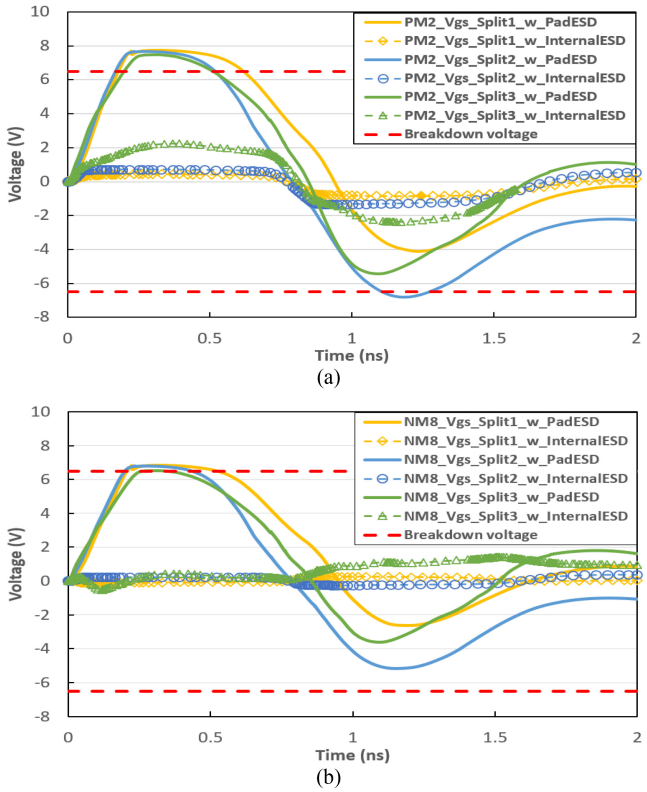

FIGURE 6. Exemplary transient voltage analysis for V_{GS} of PM2 and NM8 of the ICs under equivalent 50V CDM ESD zapping: (a) gate breakdown failures occur in the IC using classic pad-based CDM ESD protection network, and (b) the IC using the new internal-distributed CDM ESD protection mesh passed CDM ESD zapping.

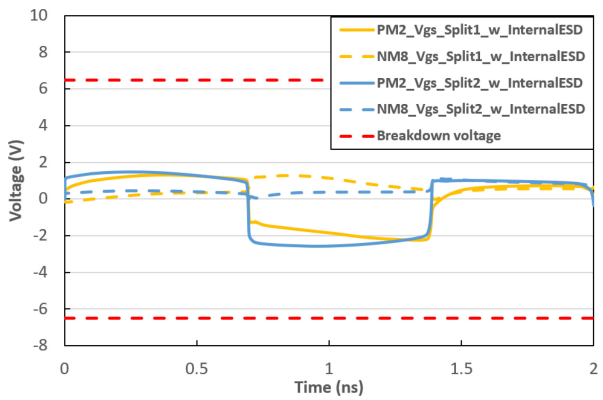

FIGURE 7. Exemplary transient voltage analysis for V_{GS} of PM2 and NM8 of the ICs under 500V CDM ESD zapping shows now voltage breakdown failure in the IC using the new internal-distributed CDM ESD protection mesh network.

ESD discharging scenarios where discharging initiated by charges at different internal locations: Split-1 for charges stored in NM1, Split-2 for charges stored at PM8 and Split-3 for charges accumulated at NM5. Note that Split-3 reflects a general situation where static charges may be randomly accumulated at NM5, which is not a main charge storage bin though. Fig. 4 models near-real-world CDM ESD discharging where internal charges stored in NM1, PM8 and

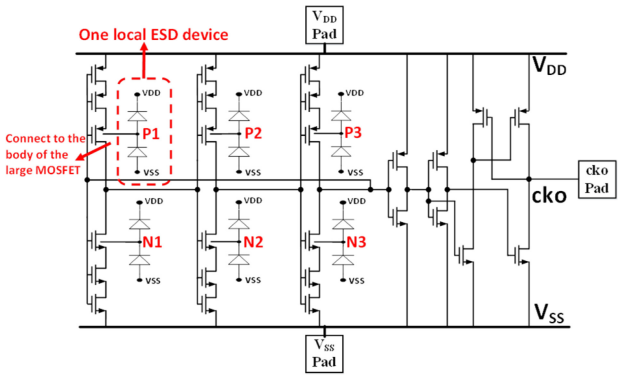

FIGURE 8. Schematic for an oscillator demo IC featuring internal-distributed CDM ESD protection mesh and fabricated in a 45nm SOI CMOS.

NM5 are discharged by grounding the V_{DD} pad. As a comparison, Fig. 5 depicts traditional CDM ESD discharging where internal charges will be discharged to the V_{DD} pad through the pad-based ESD protection devices. It is expected that different CDM ESD discharge paths will act in the three splits shown in Fig. 4 and Fig. 5. During CDM ESD simulation, CDM ESD stimuli of varying strengths are used to evaluate different CDM ESD discharging capabilities of the Splits. The CDM ESD failure criterion used is the gate voltage breakdown ($|V_{GS}|$ or $|V_{GD}|$) of any MOSFET, which is BV_{OX}~6.5V for the 45nm SOI process used in this work. Fig. 6 presents the transient CDM discharging voltage waveforms by SPICE for exemplar MOSFETs, PM2 and NM8, for the splits under 50V CDM ESD zapping where the equivalent internal/local pulse strength is about 2% of 50V when zapped at a pad. It is observed that CDM ESD voltage breakdown failures occurred at the gate of PM2 and NM8 for the IC case of using traditional pad-based CDM ESD protection; however, the IC using new internal-distributed CDM ESD method passed 50V CDM ESD zapping. To further evaluate the ESD protection capability of the new internal-distributed CDM ESD mesh network, CDM ESD pulse strength increases in CDM ESD simulation for the IC case of Fig. 4, and Fig. 7 shows that it can survive 500V CDM ESD zapping without any gate breakdown failure. This chip-level CDM ESD circuit simulation proves that the new internally distributed CDM ESD protection concept is effective.

A simplified oscillator IC, as depicted in Fig. 8, was designed and fabricated in a foundry 45nm SOI CMOS using the new internal-distributed CDM ESD protection method as a demo. The internally distributed CDM ESD protection net consists of simple ESD protection diodes that are placed at the internal circuit nodes associated with the six large MOSFETs (P1, P2, P3, N1, N2 and N3), being the main local static charge storage bins reflecting internal charge distribution in real ICs. Fig. 9 shows the measured output voltage waveform for the fabricated oscillator IC. Due to lack of commercial CDM ESD zapping tester in our lab, we chose to conduct VFTLP stressing test to evaluate CDM ESD protection for the fabricated IC dies. The VFTLP tester used

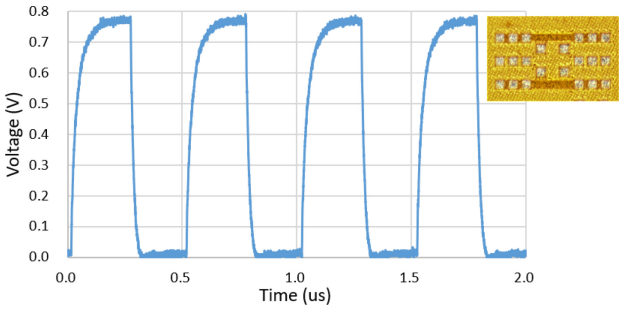

FIGURE 9. **Measured output waveform of the oscillator IC fabricated in a 45nm SOI. Inset is a die photo.**

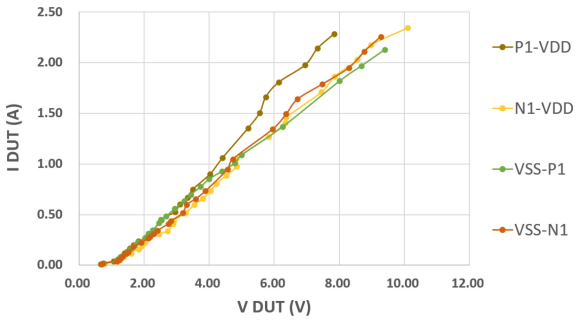

FIGURE 10. **Measured ESD discharge I-V curves for the IC with internally distributed CDM ESD protection mesh by applying VFTLP pulses to the internal nodes.**

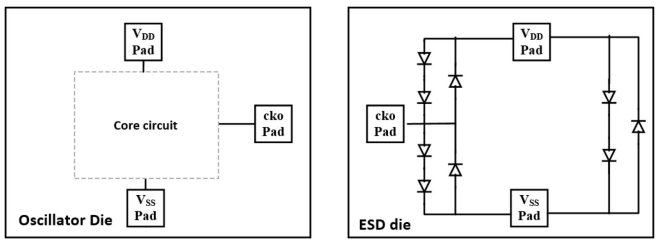

FIGURE 11. **Illustration of interposer-based internal-distributed CDM ESD protection solution utilizing two dies: (a) an active core IC die, and (b) a dedicated interposer CDM ESD protection die.**

is Barth 4012 VFTLP+ model. During VFTLP testing, the GS probe was applied directly to the internal circuit nodes where the internal-distributed CDM ESD protection diodes are connected. Therefore, VFTLP testing can effectively and adequately check if the internal CDM ESD devices can respond to the ultrafast CDM ESD pulses and provide CDM ESD protection internally and locally. Fig. 10 presents exemplar CDM ESD discharging I-V curves at various internal circuit nodes stressed by VFTLP pulse routines, which clearly shows that the internal-distributed CDM ESD protection didoes can effectively discharge the CDM ESD pulses in VFTLP test, to the CDM level of higher than I_{t2}∼2A. The demo circuit, while simple, readily validated that the new internal-distributed CDM ESD protection method works in real Si, which will be further improved in our on-going designs.

III. INTERPOSER AND TSV-BASED INTERNAL-DISTRIBUTED ESD PROTECTION

The new internal-distributed CDM ESD protection method can be realized in some novel ways for added benefits. Traditionally, on-chip ESD protection utilizes large co-planar ESD protection structures in a side-by-side manner, i.e., in-plane layout design with the core IC circuitry, which causes substantial ESD-induced design overhead (i.e., ESD-induced parasitic capacitance, leakage, and noises, as well as Si area consumed by large ESD protection devices and IC layout difficulty) [1], [2], [9]. In general, higher ESD protection robustness makes the ESD design overhead problem even worse. We recently devised two novel 3D ESD protection techniques, interposer ESD protection and TSV-based ESD protection [10], [11], which are utilized to further improve the new internal-distributed CDM ESD protection method.

In 3D IC packaging, an interposer is a separate Si substrate used to host complex metal interconnects to electrically connect multiple IC dies into a system-in-a-package (SiP). An interposer-based ESD protection technique works as following: all large and troublesome ESD protection structures are removed from the IC die and are placed in a separate interposer Si substrate, resulting in one active die for the IC core only and an interposer die housing the complex ESD protection network as illustrated in Fig. 11 for traditional pad-based ESD protection designs. The two dies are then interconnected vertically together for an ESD-protected chip, equivalent to the chip shown in Fig. 5. Before processing the flip chips, solder bump must be carefully added onto the bond pads of interposer ESD die as shown in Fig. 12. Solder bumps can be easily deposited on the bond pads during foundry fabrication. Solder bumps have various functions: 1) to provide electrical connections for the two dies, 2) to provide thermal conduction for ESD-generated heat, and 3) to provide mechanical support to the flip-chips. The interposer ESD die is flipped over so that its bond pads face down, and are aligned with and bonded to the matching pads on the active IC die. the interposer ESD protection method was validated experimentally using a single-pole four-throw (SP4T) RF switch IC deigned and fabricated in a 45nm SOI, with the prototype dies shown in Fig. 13. The no-ESD SP4T core circuit die has four outputs (O1, O2, O3 and O4) requiring ESD protection, which is provided by a separate interposer ESD die. The signal pads and ground pads (G, for GSG testing) are aligned in design for solder bump bonding following a flip-chip bonding process shown in Fig. 14. The interposer ESD protection technique is perfectly suitable for the new internal-distributed CDM ESD protection method for improved CDM ESD robustness. Using the oscillator IC shown in Fig. 4 as an example, all internal-distributed anti-parallel ESD protection didoes originally embedded in the IC die are removed from the SP4T chip, making it an ESD-free active IC die only. These ESD protection didoes are designed into a separate interposer die dedicated to ESD protection that houses the required internal-distributed

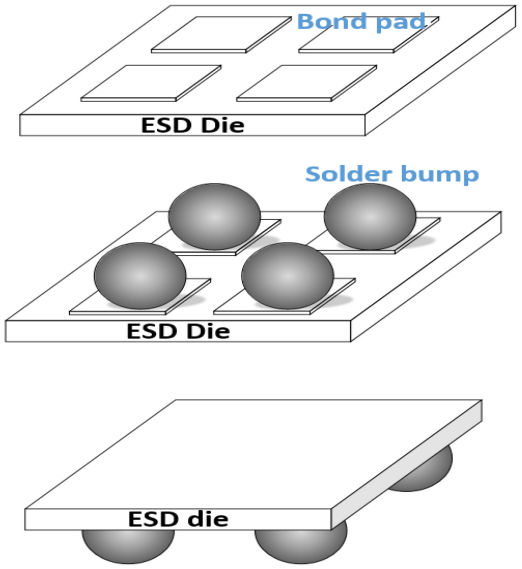

FIGURE 12. Illustration of making an interposer-based CDM ESD protection using solder bumps for connection to an active IC core die.

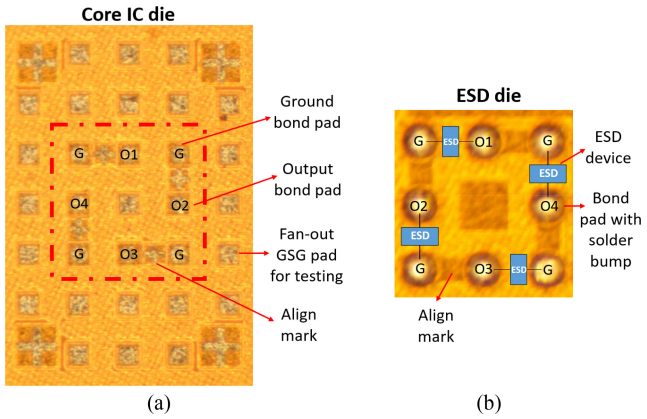

FIGURE 13. Die photos for an exemplar two-die interposer-based internal-distributed CDM ESD protection design fabricated in a 45nm SOI: (a) active SP4T core IC die, and (b) an interposer CDM ESD protection die.

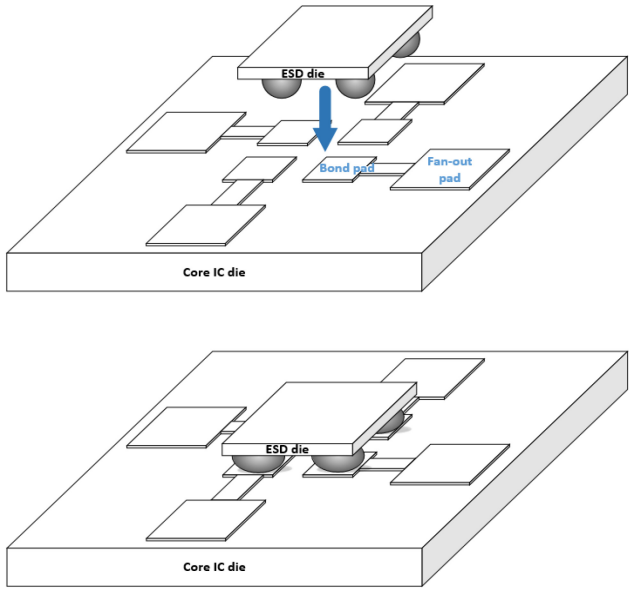

FIGURE 14. A SiP process flow for a SP4T RF switch IC utilizing interposer-based internal-distributed CDM ESD protection, featuring bump bonding.

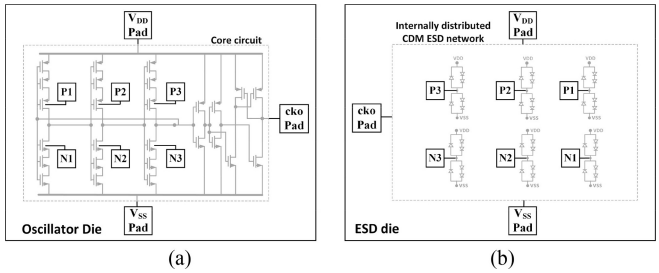

FIGURE 15. Illustration of a two-die interposer-based internal-distributed CDM ESD protection design for an exemplar oscillator IC in 45nm SOI: (a) active oscillator core IC die, and (b) interposer CDM ESD protection die for internal-distributed CDM ESD protection.

CDM ESD protection mesh network. The oscillator core die is modified to have the selected internal nodes (P1, P2, P3, N1, N2 & N3) ready for ball bonding with the interposer CDM ESD protection die, using small internal "pads" according to the solder bumps used. The two-die design is illustrated in Fig. 15 for the no-ESD core die and dedicated interposer CDM ESD protection die. The two dies are bonded together through 3D heterogeneous integration to deliver the full ESD-protected oscillator IC with internal-distributed CDM ESD protection. Compared to realizing internal-distributed CDM ESD protection using conventional in-plane side-by-side ESD protection devices, the flip-chip interposer-based internally distributed CDM ESD protection method offers many benefits: 1) Because the ESD protection devices are "taken out" of the core circuit die, the area budget can be greatly reduced which is vitally important to complex chips. 2) Correspondingly, the ESD-induced parasitic capacitance, leakage and noises can be significantly minimized. 3) With the entire ESD protection network in a separate interposer ESD die, smart partitioning will allow a more widely distributed CDM ESD protection mesh network that will further improve full-chip CDM ESD protection capability while using smaller-sized ESD protection devices. 4) Obviously, the solder bumps also serve to dissipate ESD-induced heat more efficiently. 5) The interposer CDM ESD protection die can be readily replaced, hence substantially mitigate the product costs possibly caused by the unavoidable CDM ESD failures. 6) The flip chip process is a very mature 3D heterogeneous integration technology. In short, the benefit of using dedicated interposer-based internal-distributed CDM ESD protection technology is potentially significant. Clearly, the interposer-based internally distributed CDM ESD protection scheme theoretically does no consume any Si area on an IC die.

Another alternative solution to the traditional in-plane side-by-side ESD protection method is to use in-hole (TSV like) vertical ESD protection structure. In principle, a deep TSV-type hole can be etched into a Si substrate that houses

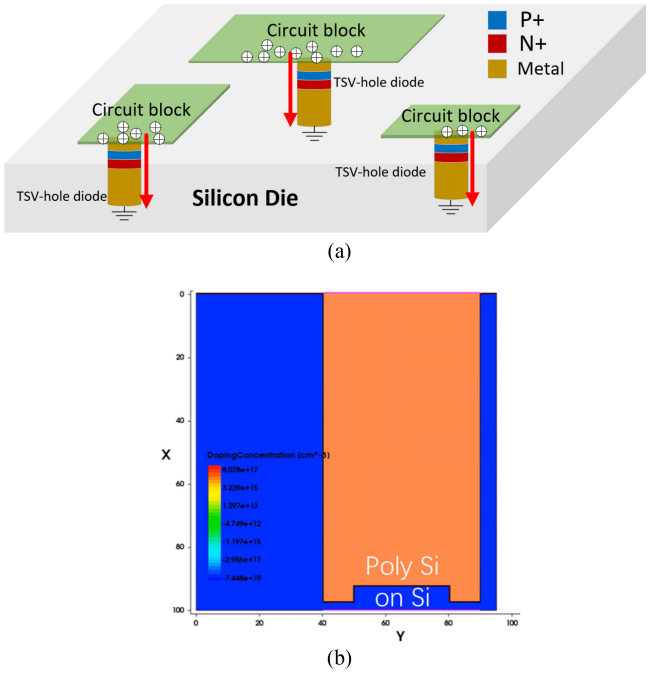

FIGURE 16. **Concept of the new in-TSV ESD protection diode for distributed ESD protection: (a) concept view, and (b) cross-sectional view by TCAD.**

a truly vertical ESD protection diode. Unlike conventional in-plane planar ESD protection structures that require careful lateral electrical connection (metals or diffusion regions), an in-TSV ESD protection diode has one terminal connected to an overhead pad and the other electrode vertically and directly connected to a local GND to the backside of the substrate. The innovative in-TSV ESD protection diode concept is depicted in Fig. 16 and recently validated experimentally where a vertical poly-Si PN junction ESD protection diode is formed inside a deep TSV hole in CMOS [11]. From Fig. 16a, it is obvious that the novel in-TSV ESD protection diodes can be utilized to construct the new internal-distributed CDM ESD protection mesh network in CMOS ICs. Compared to the internal-distributed CDM ESD protection scheme using traditional in-plane side-by-side planar ESD protection devices, the in-TSV type internally distributed CDM ESD protection design offer several key advantages: First, it dramatically reduce the Si area consumed by ESD protection devices and their lateral diffusion interconnects, ideally zero extra die area needed because an in-TSV ESD protection diode is placed under the active IC die. Second, it is very layout-friendly due to its true 3D structural nature. Third, since an in-TSV ESD protection diode can be readily placed locally under any transistor on a die, it allows great freedom to construct a comprehensive internal-distributed CDM ESD protection mesh on an IC die. Fourth, the local and vertical interconnects to in-TSV ESD protection diodes can significantly improve ESD discharging efficient that also helps to minimize ESD heating. Fifth, the local vertical metal pillar serves to dissipate any ESD-generated heat efficiently. In summary, the new in-TSV based internal-distributed CDM ESD protection scheme is a very efficient full-chip CDM ESD protection technology.

The concept of in-TSV ESD protection structure is validated experimentally using a new CMOS-compatible process in our cleanroom facility, which can be readily transferred to foundry processes. Referring to Fig. 16, the process starts creating a deep TSV-like hole (not a through-substrate hole as a TSV though) in a Si substrate. To etch a high aspect ratio in-TSV hole in our cleanroom with limited processing tools, we developed a unique process module to first etch a 100μm-deep ring into Si wafer, which is followed by thermal oxidation to form a SiO_2 layer covering the inner wall of the deep hole. Next, a center Si pillar (heavy P-doped) inside the TSV-like hole was created by deep reactive ion etch (RIE). A poly-Si layer (ideally, single-crystal Si is preferred) was then deposited on top of the p-type center Si pillar inside the deep hole, which was then N-doped by ion implantation. A vertical poly-Si PN junction ESD protection diode was finally created inside the TSV hole that is connected by metals (TSV metal pillar) for testing. While the fabrication process seems to be a little involving due to our cleanroom facility limitation, such in-TSV ESD protection didoes can be easily made in any foundry CMOS flows. Due to our process limitation in high aspect-ratio etching, the prototype device has a diameter of 400μm inside a TSV hole of 100μm deep, shown in Fig. 17. To characterize CDM ESD protection function of the prototype vertical in-TSV ESD didoes, VFTLP test should be used for CDM ESD test. However, it is extremely difficult to add GS (ground-signal) pads, required for VFTLP testing, on the demo device due to our cleanroom limitation. Instead, the fabricated in-TSV ESD protection diode samples were characterized by TLP testing (Barth 4002 TLP tester) to prove that the new vertical TSV-like ESD diode structure works for ESD protection. Fig. 18 depicts the TLP-measured transient ESD discharging I-V curves for prototype in-TSV ESD protection diodes, which clearly demonstrate the expected ESD discharging I-V characteristics and very low leakage. The multiple-sample testing results obtained also serve to show the desired function uniformity and stability of the prototype vertical in-TSV ESD protection didoes. The extracted ESD triggering voltage is V_{t1}~2.0V and the ESD thermal breakdown current is I_{t2}~13mA for the poly-Si diode prototypes. In terms of device construction, PN junction creation, impurity doping, and metal interconnects, the prototype in-TSV ESD protection diode fabricated in our cleanroom are yet to be optimized. The prototype devices are for proof of concept purpose only.

The new TSV-based internally distributed CDM ESD protection technique was also verified by chip-level ESD simulation using the same oscillator IC described preciously. Considering that the in-TSV ESD diode prototypes were made in our cleanroom facility, not available in any commercial foundries yet, the validation was conducted by CDM ESD simulation similar to the procedures discussed earlier. Fig. 19 shows the schematic for the 3-stage

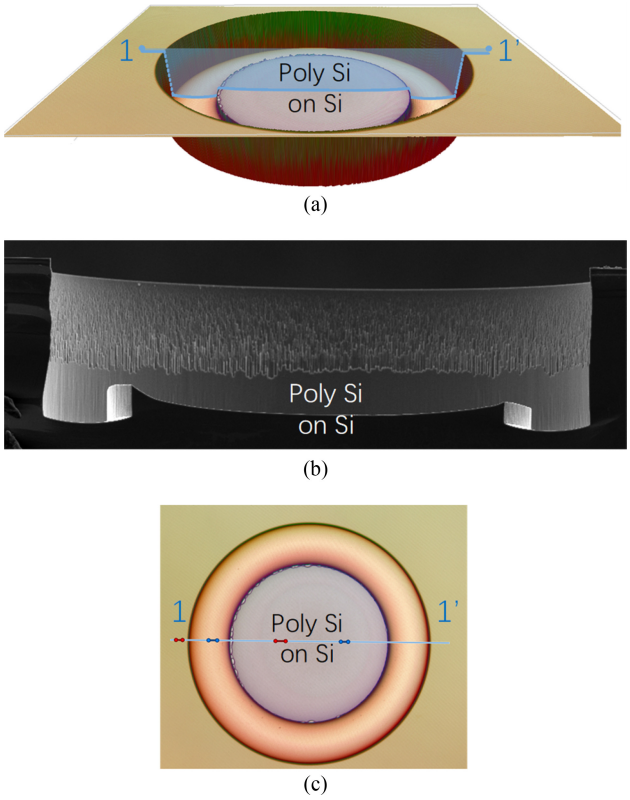

FIGURE 17. Images for prototype in-TSV poly-Si/Si PN diode ESD protection diode fabricated inside a 100μm deep TSV hole: (a) a 3D image by confocal microscope, (b) a cross-section view along 1-1′ cutline of the PN diode by SEM, and (c) a top view of in-hole ESD diodes by optical microscope along 1-1′ cutline.

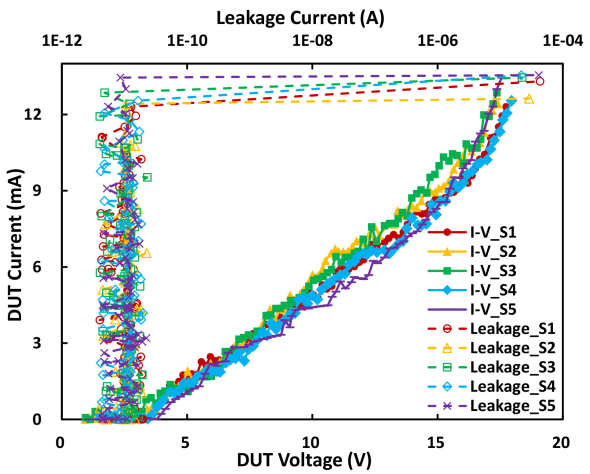

FIGURE 18. TLP-measured transient ESD discharging I-V curves for prototype in-TSV ESD diodes confirm the ESD protection function and low ESD-induced leakage.

oscillator IC designed in a 45nm SOI CMOS where the internal-distributed CDM ESD protection mesh network was formed by in-TSV ESD protection diodes. Similarly, the in-TSV ESD protection diodes are connected between the internal/local nodes and local GND to emulate the function of the in-TSV ESD protection diodes. Per smart partitioning,

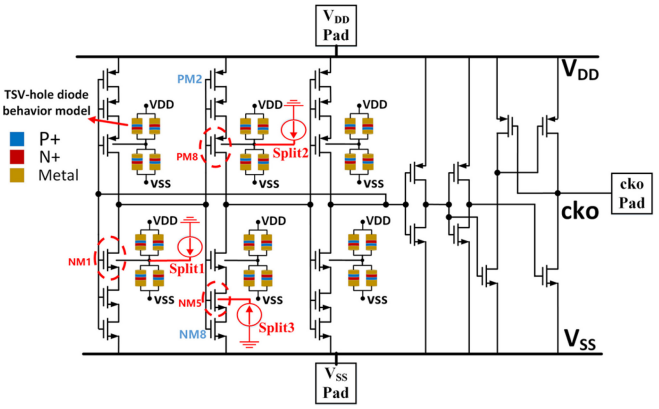

FIGURE 19. A 3-stage oscillator IC designed in 45nm SOI with TSV-based internally distributed CDM ESD network.

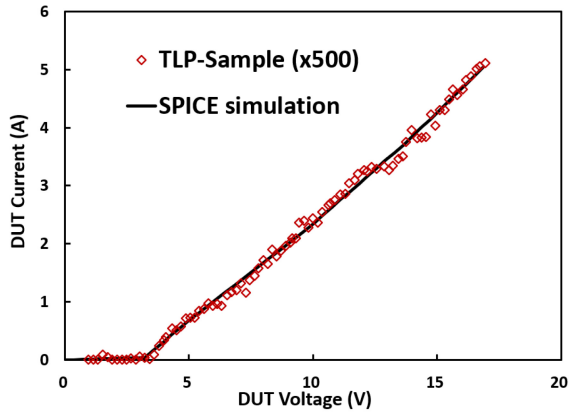

FIGURE 20. An exemplar TSV-like ESD protection diode of practical size is created using the diode behavioral model extracted from TLP testing for the prototype in-TSV ESD protection diode fabricated.

the concerned internal nodes are NM1, NM2, NM3, PM7, PM8 and PM9, which are considered to be the main internal charge storage bins. ESD protection device behavioral models were developed for the prototype in-TSV ESD diodes fabricated [12]. For meaningful full-chip CDM ESD simulation, larger in-TSV ESD protection diodes of about 500 times of the prototype fabricated were used in chip-level CDM ESD simulation utilizing the ESD diode behavioral models extracted as shown in Fig. 20. Chip-level CDM ESD protection simulation was conducted for the oscillator IC with three splits similar to that discussed before, i.e., modeling the CDM ESD discharging initiated by internal charges stored at NM1 (Split-1), PM8 (Split-2) and NM5 (Split-3), which are discharged against the grounded V_{DD} pad as shown in Fig. 19. Fig. 21 presents the transient CDM discharging voltage waveforms by SPICE for the exemplar MOSFET PM2 and NM8 under CDM ESD zapping of pulse strength equivalent to 50V CDM ESD stressing at pads, ~2% of the pulse when zapping internally. Compared with the results shown in Fig. 6, the IC die using the TSV-based internally distributed CDM ESD protection network passed equivalent 50V CDM zapping without any gate breakdown failure. The CDM ESD

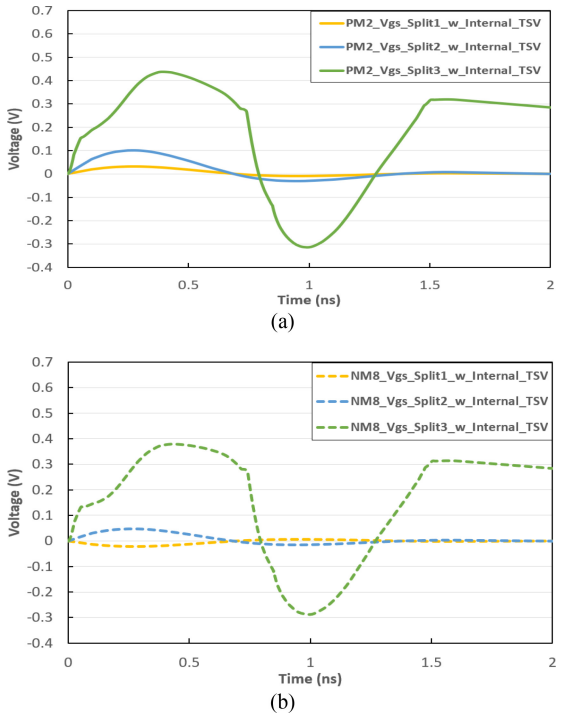

FIGURE 21. Exemplary transient voltage analysis for V_{GS} of PM2 and NM8 of the ICs using TSV-based internal-distributed CDM ESD protection network under equivalent 50V CDM ESD zapping: (a) gate breakdown failures occur in the IC using classic pad-based CDM ESD protection network, and (b) the IC using the new internal-distributed CDM ESD protection mesh passed CDM ESD zapping.

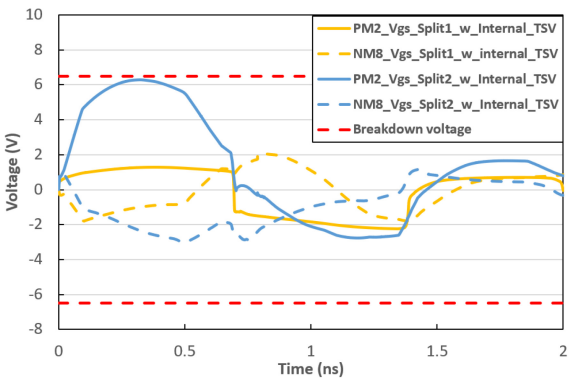

FIGURE 22. Exemplary transient voltage analysis for V_{GS} of PM2 and NM8 of the ICs using TSV-based internal-distributed CDM ESD protection network passes 350V CDM ESD zapping without gate voltage breakdown failure.

zapping level was then increased to evaluate the CDM ESD protection potential, which indicates that the chip can sustain ~350V CDM ESD zapping without reaching to BV_{OX}~6.5V in 45nm SOI CMOS as depicted in Fig. 22. It is worth-noting that, while the TSV-based internally distributed CDM ESD protection is partially validated experimentally, the new technology is still in its infancy and significant research in currently on-going to better understand its mechanisms and improve its performance. Obviously, the TSV-based internally distributed CDM ESD protection design can dramatically reduce the die area normally consumed by ESD protection structures.

IV. CONCLUSION

This paper reports a comprehensive study of a novel non-pad-based internally distributed CDM ESD protection technique, which aims to overcome the design uncertainties in full-chip CDM ESD protection designs associated with the faulty traditional pad-based CDM ESD protection methods. Further improvements can be achieved by using novel interposer or TSV-like ESD protection structures to form the internal-distributed CDM ESD protection mesh network. The internally distributed CDM ESD protection concept is validated by both ESD simulation and partial experiments with prototype IC designed in 45nm SOI CMOS. The novel internally distributed CDM ESD protection method, especially in interposer and TSV formats, can dramatically reduce the die area normally consumed by large pad-based ESD protection structures, hence, partially resolving the ESD-induced design overhead problem. The actual benefit of layout reduction for a chip is entirely depending on a specific IC design. The new CDM ESD protection technique has the potential to provide robust on-chip CDM ESD protection for complex ICs in advanced technologies.

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