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Erratum to "Effect of the Blocking Oxide Layer With Asymmetric Taper Angles in 3-D NAND Flash Memories"

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In [1], the following sentence on p. 774, second column, is revised as follows.

"We propose optimal etching profiles that can improve the uniformity of the electrical characteristics between cells, and we discuss the reasons for changes in the threshold voltage shift (ΔV_T) due to changes in the etching profile."

On p. 776, in the first sentence of the first full paragraph, the space between 'ΔV_T' should be deleted and is should appear as follows:

ΔV_T.

REFERENCES

[1] J. G. Lee, W. J. Jung, J. H. Park, K.-H. Yoo, and T. W. Kim, "Effect of the blocking oxide layer with asymmetric taper angles in 3-D NAND flash memories," *IEEE J. Electron Devices Soc.*, vol. 9, pp. 774–777, 2021.

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