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Sensitivity Improvement of a Fully Symmetric Vertical Hall Device Fabricated in 0.18 μm Low-Voltage CMOS Technology

HAIYUN HUANG[1] AND YUE XU[2] (Member, IEEE)

1 College of Electronics and Information, Hangzhou Dianzi University, Hangzhou 310018, China
2 College of Electronic and Optical Engineering, National and Local Joint Engineering Laboratory of RF Integration and Micro-Assembly Technology, Nanjing University of Posts and Telecommunications, Nanjing 210023, China

CORRESPONDING AUTHOR: Y. XU (e-mail: xuyue_cd@163.com)

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ABSTRACT This paper proposes a new implementation method to significantly improve the magnetic sensitivity of a fully symmetric vertical Hall device (FSVHD) based on low-voltage CMOS technology. The FSVHD consists of four identical three-contact vertical Hall elements (3CVHE) and each 3CVHE is located in a low-doped deep n-well. The terminals of the 3CVHE are n^+ implanted in an n-well and a p^+ implantation in a p-well is performed to act as a trench between two adjacent n^+ contacts, enabling Hall current flowing deeply for sensitivity improvement. The influence of the geometry sizes on magnetic sensitivity is exploited utilizing TCAD simulation to obtain the optimized device structure in a 0.18 μm CMOS standard technology. The experimental results reveal that the proposed FSVHD with a p^+/p-well trench can attain an improved voltage-related sensitivity of 8.4 mV/VT, which is about 70% higher than that of a conventional FSVHD without a trench in the same CMOS fabrication process, while offset and noise are not degraded. The proposed p^+/p-well implantation trench is a good solution to enhance the sensitivity of a low-voltage CMOS VHD with a low manufacturing cost.

INDEX TERMS Vertical hall device, magnetic sensitivity, trench, standard CMOS technology.

I. INTRODUCTION

Integrated Hall magnetic sensors fabricated in Complementary Metal Oxide Semiconductor (CMOS) technology have broadly used in automobiles, industrial controls, and consumer electronics for various applications, such as contactless encoding, current sensing, and position detection, etc [1]–[5], where the accurate measurement of the magnetic field is required. There are two kinds of integrated Hall devices. One is the conventional horizontal Hall devices (HHDs), which can detect the magnetic field perpendicular to the device plane [6]. The other is the vertical Hall devices (VHDs), which are sensitive to the two in-plane magnetic field components parallel to the surface of the chip [7]. In combination with horizontal Hall plates, CMOS VHDs are convenient to realize the integrated 3D Hall probes for linear, angular, and position measurements without post-processing technology [8]–[9]. The integrated magneto-concentrator (IMC) solution can also convert an in-plane magnetic field locally into a vertical one, making conventional HHDs able to measure the same in-plane field component as VHDs, but the Hall sensors with IMC face several unavoidable drawbacks, such as higher manufacturing cost, a relatively narrower magnetic field detection range, and a relatively higher offset. Therefore, developing low-cost and high-performance VHDs in CMOS technology becomes very important.

However, CMOS VHDs suffer a lower magnetic sensitivity and a higher residual offset voltage [10]–[11] compared with the more widespread HHDs. Because the terminals of the VHDs are arranged at the device surface in parallel and the active region of the device is shallow in CMOS standard technology, the input bias current flows easily through the surface contact regions rather than go deep into the device interior, resulting in very low sensitivity. Thereby, a CMOS

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high-voltage (HV) manufacturing process with a special low-doped deep n-diffusion layer (NTUB) is suggested to be used [12], but it significantly increases the fabrication cost. For another thing, the high residual offset of the VHDs is mainly attributed to the lack of electrical symmetry concerning contact commutation when a spinning current technique for dynamic offset cancellation is applied. To improve the symmetry performance of the device, four-contact and six-contact structures instead of the conventional five-contact structure have been studied [13], but they still have problems with high initial offset voltage, especially for four-contact VHDs. One of the most popular methods to reduce the offset of a fully symmetric vertical Hall device (FSVHD) is a four-folded and three contacts structure [14]–[17], nevertheless, its sensitivity has not been greatly improved.

In recent years, various techniques have been proposed to enhance the magnetic sensitivity of VHDs. The influence of structure size and technology on the sensitivity of the five-contact VHD was studied by Finite Element Method (FEM) simulations [18], and the modification of the process conditions is suggested to improve sensitivity. A vertical Hall plate structure with a high negative differential sensitivity is also put forward [19], applying novel signal extraction techniques for sensitivity enhancement. An orthogonal coupling structure composed of two sets of double three-contact vertical Hall devices has been proposed, which achieves the purpose of further reducing the offset voltage while maintaining the device sensitivity [20].

In this work, aiming to solve the low sensitivity of VHDs in low-voltage (LV) CMOS standard technology, p^+/p-well implantation as a trench in the deep n-well (DNW) is proposed to improve the magnetic sensitivity for an FSVHD. The optimal device size is investigated for sensitivity improvement using TCAD simulation. After being fabricated in a 0.18 μm LV CMOS technology, the improved magnetic sensitivity of the proposed FSVHD was validated by the measured data.

This paper is organized as follows. Section II analyzes a p^+/p-well trench method to improve the sensitivity of VHDs. Section III shows the optimized device geometry parameters from the TCAD simulation results. The experimental results are given in Section IV. Conclusions are drawn in Section V.

II. DEVICE DESIGN AND TCAD SIMULATION

Fig. 1 (a) shows a fully symmetric VHD (FSVHD) structure with four identical three-contact vertical Hall elements (3CVHE) [16]–[17], realized in CMOS standard technology. The active region of each 3CVHE consists of an n-well (NW) diffused into a p-doped substrate and three n^+ diffusions as contacts are arranged on the surface of the n-wells. The two side contacts of each 3CVHE are used to interconnect the individual 3CVHE. The four central contacts of each 3CVHE (C1, C2, C3, and C4) serve as drive and sense terminals, enabling four bias operation modes to be applied, as shown in Fig. 1(b). If the interconnecting metal lines have the same resistances, the four bias modes are electrically equivalent. The symmetry of the FSVHD is similar to that of planar horizontal Hall devices, which is very suitable for the dynamic four-phase spinning-current technique. As a result, a low residual offset can be attainable. Unsatisfactorily, the sensitivity of the FSVHD is not improved relative to the conventional VHDs, such as a five-contact structure.

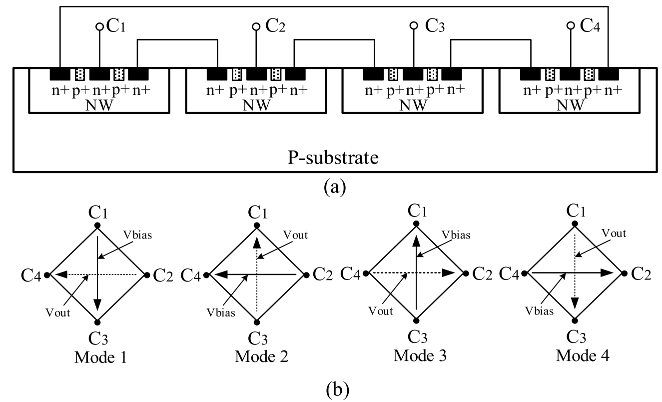


FIGURE 1. Schematic of (a) the conventional FSVHD in CMOS standard technology and (b) the four operating modes.

The Hall voltage for the VHDs in case of the voltage bias is given by [6]:

$$V_H = S_V \cdot V_{bias} \cdot B \tag{1}$$

where the voltage-related sensitivity S_V is determined by [21]:

$$S_V = G_V \cdot r_H \cdot \mu \tag{2}$$

We denote with G_V the geometrical factor ($0<G_V< 0.74$), with r_H the Hall scattering factor of the material, with μ the mobility of the carriers.

For planar HHDs with twofold symmetry, a high G_V can approach the theoretical limit of 0.74 [21]. However, For VHDs with lower symmetry and additional degrees of freedom, the G_V value is significantly reduced compared to that of the HHDs due to the value of the input resistance [22]. The Hall factor r_H is about 1.2 for an n-well silicon material at room temperature. The mobility depends on the material and doping concentration, which is reduced with the increase of doping concentration. Thus, the high sensitivity needs a high geometrical factor and low carrier concentration.

Notably for the VHDs, since the two sensing contacts are located between the two biasing contacts, respectively, the part of the bias current will flow through the sensing contacts. As a consequence, the VHDs suffer from short-circuit effects because of the sensing contacts [10], [23]–[24], which decreases the geometrical factor and results in low sensitivity. The short-circuit effect will become more marked for the LV standard CMOS technology with the limited n-well depth. Therefore, the VHDs are generally built in the deep N-well of an HV CMOS technology and the LV standard CMOS technology is not fit for implementation of the VHDs.

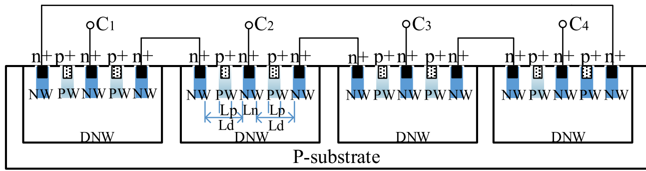
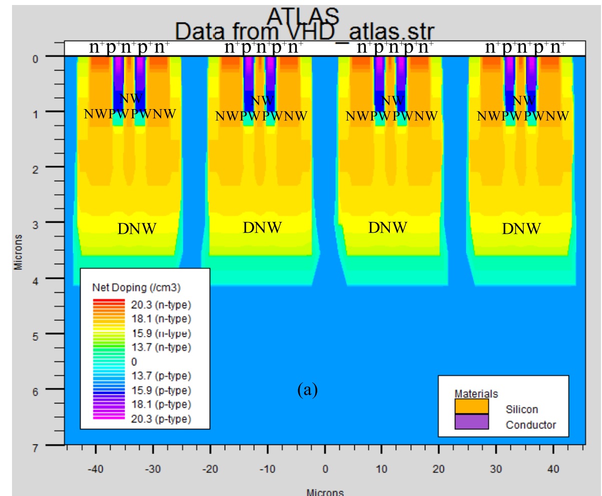


FIGURE 2. Schematic of the proposed FSVHD with the p^+/p-well trench based on CMOS standard technology.

To solve this critical problem, we propose a new solution to significantly enhance the sensitivity of the FSVHD based on low-cost low-voltage CMOS technology. Fig. 2 shows the FSVHD with the p^+/p-well trench structure. Unlike previous devices fabricated in the shallow n-well, the proposed FSVHD is realized in four identical deep n-wells (DNWs) on a p-type substrate. In each DNW, three n^+ active regions surrounded by three n-wells (NWs) are implanted as the input/output contacts. It is noteworthy that a p-well (PW) is inserted between two adjacent n-wells and a p^+ implantation in each p-well is performed to act as a trench, which can effectively drive the current to go into the interior of the DNW. Thereupon, the short circuit effect can be mitigated, enabling the improvement of magnetic sensitivity. On the other hand, since the DNW has a relatively larger depth than the n-well, the VHDs fabricated in the DNW can obtain higher sensitivity.

To verify the feasibility of the proposed method, TCAD simulation was carried out on the FSVHD with the p^+/p-well trench. According to an 0.18 μm low-voltage CMOS standard process, 2D device simulations were performed using the SILVACO Atlas tool to acquire the electrical properties of the FSVHD. Various physical models like carrier generation-recombination, mobility, magnetic, impact ionization were applied in the device simulation. Fig. 3 (a) shows the 2D device simulation structure. Here, the DNW has a retrograde doping profile with a junction depth of about 3.5 μm, and a peak concentration ($> 1.5\times10^{17}$ cm^{-3}) is situated at the depth of 2 μm. Besides, the depth of shallow n-well and p-well is about 1.5 μm and the peak doping level is about 5×10^{17} cm^{-3}. The simulated net doping profile as a function of depth provides information about the concentration of impurities in the diffusion layers, as illustrated in Fig. 3(b).

The geometry sizes, for example, the n^+ contacts and p^+/p-well trench and their locations will affect the current distribution and change the sensitivity of the FSVHD. To evaluate the effect, we choose three variables, namely, the width of n^+ contacts (Ln) and the width of a p^+/p-well trench (Lp), the distance between the two adjacent n^+/n-well terminals (Ld). To meet the design rule of the 0.18 μm CMOS standard technology, the n^+, and p^+ implantation regions are wrapped by n-well and p-well with an overlap of 0.3 μm, respectively. We can optimize the sensitivity of the proposed FSVHD by analyzing the effect of each variable.



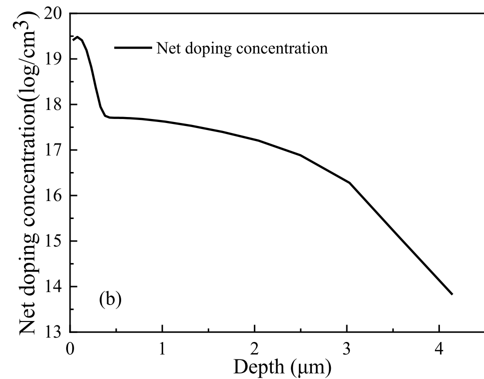


FIGURE 3. Schematic of (a) the 2D device simulation model of the FSVHD and (b) the 1D net doping profile of the active region obtained with the Silvaco Atlas tool.

III. TCAD SIMULATION RESULTS

A. INFLUENCE OF WIDTH OF N+ CONTACTS

Firstly, we studied the width of n^+ contacts on the sensitivity by TCAD simulation. The width (Ln) of central n^+ contacts of 3CVHE is increased from 0.42 μm to 2.42 μm by a 0.4 μm step when the distance (Ld) between the central and the two side n^+/n-well contacts and the width (Lp) of the p^+/p-well trench are fixed at 2.8 μm and 1.5 μm, respectively. Fig. 4 shows the simulated sensitivity versus the width of the central n^+ contacts. The voltage-related sensitivity (S_V) is significantly decreased from 9.2 mV/VT to 7.5 mV/VT with the increase of Ln at the 2 V bias. When fixing the Ln and changing the width of the n+ contacts on both sides, we further find that the sensitivity is almost unchanged. This is because for the central n^+ sense contact, the smaller width, the higher the geometry factor, leading to the larger sensitivity. For the two side n^+ contacts, they only play a role in Hall signal transmission and have no great effect on Hall current. The minimum width of the central n^+ implantation is thus suggested to be 0.42 μm for maximum sensitivity, which is determined by the design rule of the 0.18 μm CMOS process.

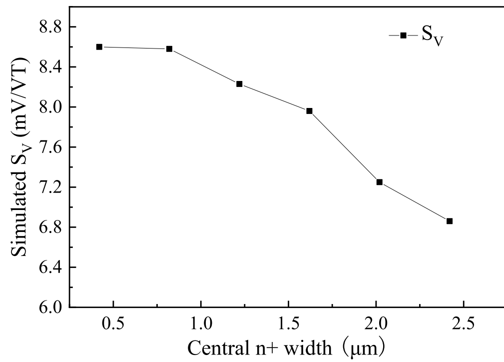


FIGURE 4. Simulated voltage-related sensitivity of the FSVHD versus the width of the central n+ contacts.

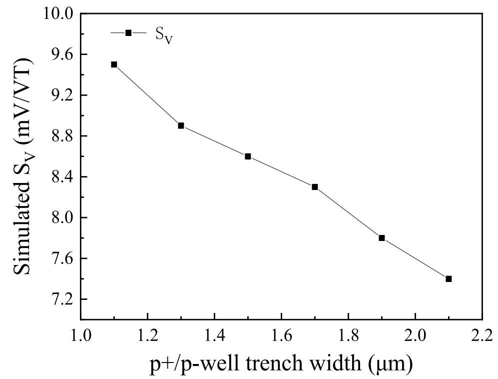


FIGURE 5. Simulated voltage-related sensitivity of the FSVHD versus the width of the p^+/p-well trench.

B. IMPACT OF P^+/P-WELL TRENCH WIDTH

The p^+/p-well trench width can also affect the sensitivity of a VHD because it changes the current density distribution. In the TCAD simulation, the p^+/p-well width (Lp) is varied from 1.1 μm to 2.1 μm by a 0.2 μm step while the distance Ld is fixed at 2.8 μm. Fig. 5 shows the simulated voltage-related sensitivity (S_v) versus the p^+/p-well width. It is seen that the S_v of the FSVHD decreases from 9.5 mV/VT to 7.4 mV/VT with the increasing p^+/p-well width. This inverse reduction in S_v comes from the resistance change of the FSVHD. As the p^+/p-well trench width increases, the resistance between the n^+ terminals becomes larger. The increased input resistance reduces the Hall current, therefore the sensitivity is inversely proportional to the trench width. It is also noted that the p^+/p-well implantation may lead to a larger offset. This is because the process of p^+/p-well implantation increases the mask-misalignment between the p^+/p-wells and n-wells, inducing a more asymmetrical PN junction depletion region. Therefore, there is a trade-off between magnetic sensitivity and offset for the choice of the p^+/p-well trench width.

C. INFLUENCE OF DISTANCE BETWEEN TWO ADJACENT N+ CONTACTS

We vary the distance (Ld) between two adjacent n^+ contacts from 1.6 μm to 3.2 μm by a 0.4 μm step to investigate the variation of the sensitivity when the p^+/p-well width and the central n^+ contact width are fixed at 1.5 μm and 0.42 μm, respectively. Fig. 6 shows the simulated voltage-related sensitivity versus distance Ld at the bias of 2 V. It is observed that the S_v is inversely proportional to the increase of the distance Ld. Due to the short circuit effect, the input bias current is easily flowing through the surface regions between the n^+ contacts. A longer distance causes a more severe short circuit effect, resulting in a weaker sensing Hall current. Consequently, the central n^+ contacts need to be as close to the two side n^+ contacts as possible.

From the simulated results above, an optimized FSVHD structure with a p^+/p-well trench for sensitivity improvement can be obtained. The central n^+ contact is designed to a minimum size of 0.42 μm for maximum sensitivity.

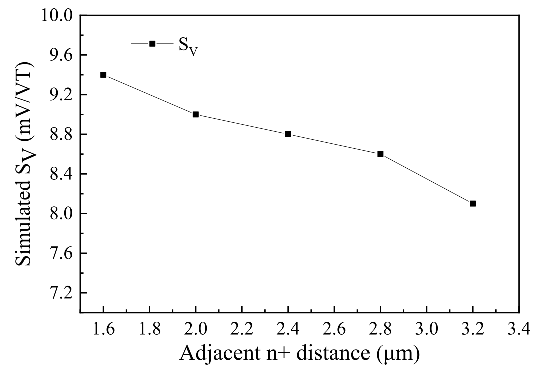


FIGURE 6. Simulated voltage-related sensitivity of the FSVHD versus the distance of the two adjacent n+ contacts.

Considering the offset, the width of the p^+/p-well trench is chosen to be 1.5 μm, not the minimum size of 1.1 μm. Reducing the distance between side and central n+ contacts is also beneficial for the enhancement of sensitivity. Similarly, the shorter distance may lead to the larger offset due to the mask misalignment, thus the distance Ld is suggested to be 2.4 μm − 3.2 μm.

IV. MEASURED RESULTS

A. EXPERIMENTAL SETUP

After the proposed FSVHD with a p^+/p-well trench was fabricated in SMIC 0.18 μm low-voltage CMOS standard technology, the magnetic sensitivity, offset, and noise characteristics were measured. Fig. 7 shows the experimental setup for the FSVHD sensor, which consists of a Gauss meter, a high-precision nanovolt meter, a semiconductor parameter analyzer, a magnetic field generator, and a power supply. After being packaged, the FSVHD was set in the center of the magnetic field generator driven by the power supply. The linear magnetic field ranged from 0 to 100 mT is generated by adjusting the output current of the power supply. The magnitude of the generated magnetic field was calibrated utilizing the Gauss meter. The Hall voltage including offset was tested by the high-precision nanovolt meter. The 1/f noise of the FSVHD was measured using the FS-PRO semiconductor parameter analyzer. The FSVHD was biased

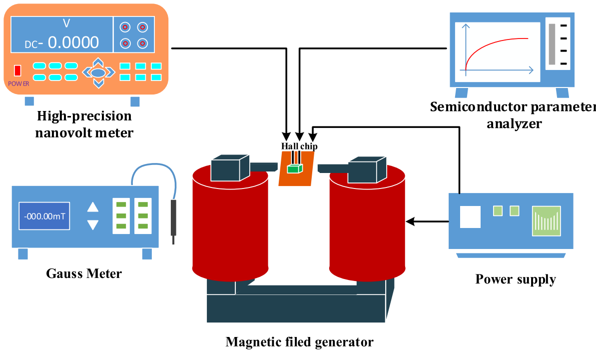


FIGURE 7. Experimental setup for the vertical Hall devices.

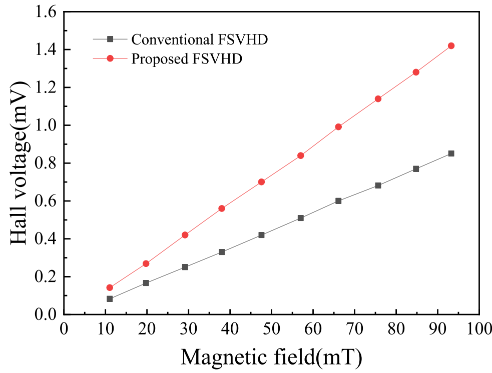


FIGURE 8. Hall voltage of the proposed FSVHD versus the magnetic field at 2 V bias. The magnetic sensitivity of the conventional FSVHD is also given for comparison.

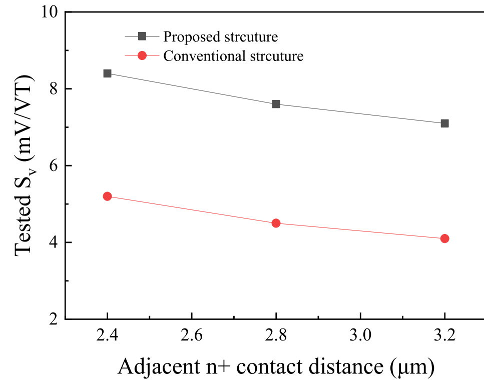


FIGURE 9. Tested voltage-related sensitivity as a function of the distance between two n+/n-well contacts.

under different voltages, setting the frequency sweep range to 1MHz, the noise power spectral density of the output terminal can be acquired by the FS-PRO.

B. MAGNETIC SENSITIVITY

Fig. 8 illustrates the output Hall voltage of the proposed FSVHD (Ln = 0.42 μm, Lp = 1.5 μm, and Ld = 2.8 μm) as a function of the magnetic field intensity at a bias of 2 V. It is found that the output Hall voltage is linearly increased with the magnetic field intensity in the 100 mT range. At the magnetic field of 93 mT, the measured Hall voltage is about 1.419 mV, thus the voltage-related sensitivity (S_v) is calculated as 7.6 mV/VT. By comparison, the conventional device without a trench shown in Fig. 1 has a lower sensitivity of 4.5 mV/VT. Fig. 9 further reveals the S_v values are changed with three distances (Ld = 2.4, 2.8, 3.2 μm). We can observe that the sensitivity is distinctly enhanced from 7.1 mV/VT to 8.4 mV/VT when the distance Ld is reduced from 3.2 μm to 2.4 μm, which is increased by about 70% over the conventional FSVHD without a trench fabricated in the same CMOS process. The test sensitivities are in good agreement with the simulation results, proving that the proposed p^+/p-well trench structure can significantly improve the magnetic sensitivity of the FSVHD.

The improvement in the sensitivity of the proposed FSVHD can be attributed to the reduction of the short-circuit effect. In our scheme, the p^+/p-well implantation trench in a deep N-well increases the effective depth of the current flowing, meanwhile, the distance between the two adjacent n+ contacts is reduced. As the proposed VHD structure is biased with a given voltage, the shunt effect due to the central contacts in each 3CVHE is certainly mitigated as compared to the conventional one without p^+/p-well implantation trench in the n-well design, which is very beneficial for the sensitivity improvement. But at the same time, the impedance between the contacts is increased when the p^+/p-well trench is used, which leads to a lower current, and thus to a lower Hall voltage. However, as seen in Fig. 9, for the same distances (Ld) between the central and the two side n+ contacts, the proposed structure can achieve higher magnetic sensitivity than the conventional one, indicating that the reduction of the short-circuit effect is dominant over the impedance increase effect on the voltage-related sensitivity in our design.

On the other hand, it should be noted that the doping concentration of the device's active area is also a major factor that affects magnetic sensitivity. Since a high n-well doping level of about 5×10^{17} cm^{-3} in our manufacturing technology degrades the mobility of electrons, the sensitivity of the presented device is relatively lower than that reported in [16]. However, our experimental results show that the voltage-related sensitivity of the proposed FSVHD is about 70% higher than that of the conventional FSVHD without a p^+/p-well trench using the same 0.18 μm CMOS process, proving that the p^+/p-well trench in the deep n-well is an efficient solution to improve the device sensitivity under the low-voltage standard CMOS technology. If the doping level of the active region is lowered, the sensitivity of the proposed device could be improved more significantly.

C. OFFSET

Although the p^+/p-well implantation between two adjacent n^+ contacts in the DNW is advantageous to the sensitivity of the VHDs, it may introduce the more severe DC offset due to mask alignment error. Fig. 10 displays the offset voltage as a function of bias voltage without applying a magnetic

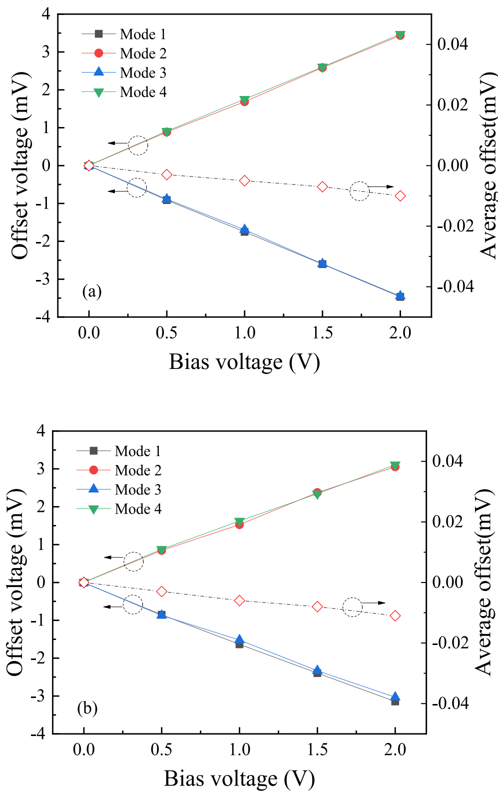


FIGURE 10. **Offset voltage as a function of voltage bias for (a) the proposed FSVHD with the p^+/p-well trench and (b) the conventional one without a trench.**

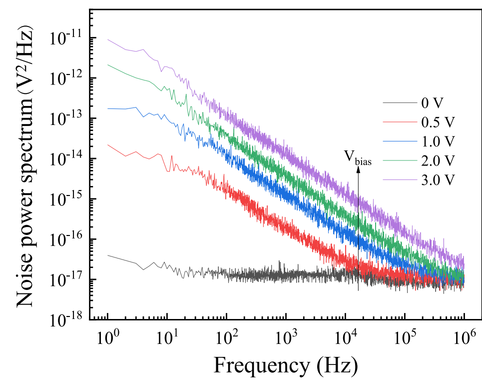


FIGURE 11. **The noise power spectrum of the proposed FSVHD with the p^+/p-well trench.**

field. To reduce measurement error, we use a high-precision nanovolt meter to measure the device offset and the offset voltage is obtained by averaging the multiple measurements. It is seen that the offset voltage is proportional to the bias voltage, and it is about 3.5 mV at the 2 V bias. It is also found that the offset voltages at the four operation modes show electrically equivalent characteristics, which is due to the fact of the fully symmetric device structure. As a result, a low average offset voltage of about 10 μV is obtained across 2 V bias. By contrast, the offset voltage of the conventional FSVHD is about 3.15 mV at the bias of 2 V and the maximum average offset voltage is about 11 μV at the four operating modes. Thanks to the optimized structure and considerable layout design, the measured offset of the proposed FSVHD is not degraded compared with that of the conventional FSVHD. Ultimately, the initial offset voltage of the FSVHD can be effectively eliminated by the four-phase spinning current technique and a low residual offset can be obtained due to the fully symmetric electrical characteristics.

D. NOISE

The noise of Hall sensors, including thermal noise and 1/f noise is also an important factor to decide the magnetic field resolution [25]. The 1/f noise is caused by electrically active carrier traps on the Si/SiO_2 borders. Vertical Hall devices usually show higher 1/f noise than horizontal Hall ones because the parallel placement of the contacts makes more Si/SiO_2 interface states exist in the device-sensitive region. In our presented VHD, the p^+/p-well implantation between n^+ contacts can push the current away from the silicon interface to reduce the parasitic trap effects, effectively lowering the 1/f noise of the VHDs.

The measurement results of the noise power spectrum are illustrated in Fig. 11. The presented FSVHD shows dominating 1/f noise at low frequencies. It is observed that the 1/f noise level is increased with the bias voltage and the corner frequency quickly shifts to higher values. At the bias of 0.5 V, the noise power spectral density at 100 Hz is about 1.38×10^{-15} V^2/Hz, and the corner frequency is about 200 kHz. As the bias is enhanced to 3 V, they are increased to about 8.63×10^{-14} V^2/Hz and 1 MHz, respectively. It is also seen that the 1/f noise decreases rapidly with increasing frequency. At the corner frequency, the 1/f noise can be almost ignored and the low thermal noise becomes the main source of the noise. The high 1/f noise of the device can also be effectively removed by the four-phase spinning-current technique [24].

V. CONCLUSION

A new p^+/p-well trench method is proposed to highly enhance the magnetic sensitivity of a fully symmetric vertical Hall device (FSVHD) with four identical three-contact vertical Hall elements (3CVHE) based on a 0.18 μm low-voltage standard CMOS technology. The p^+/p-well implantation trench is located between the two adjacent n^+ contacts inside a deep n-well, which can drive the input current flowing deeply and effectively reduce the short-circuit effect, enabling the Hall effect enhancement. The structure size parameters of the FSVHD affecting sensitivity were investigated by TCAD simulation to enhance the magnetic sensitivity using a 0.18 μm standard CMOS technology. The experimental results reveal that the FSVHD with a p^+/p-well trench has improved the voltage-related sensitivity up to 8.4 mV/VT at 2 V bias, which is improved by nearly 70% compared to that of the conventional one without a trench. Meanwhile, the offset and 1/f noise are as low

as the conventional ones. Therefore, the p^+/p-well implantation trench is a good solution to significantly enhance the sensitivity of a CMOS VHD without any additional process modification cost.

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HAIYUN HUANG received the Ph.D. degree in microelectronics and solid-state electronics from the Dalian University of Technology, China, in 2015.

He is currently a Lecturer with the Hangzhou Dianzi University, Hangzhou, China. His current research interests include CMOS analog integrated circuit design and hall sensor design.

YUE XU (Member, IEEE) received the Ph.D. degree in microelectronics and solid-state electronics from Nanjing University, Nanjing, China, in 2012.

He is currently a Professor with the Nanjing University of Posts and Telecommunications, Nanjing, China. His current research interests include CMOS hall integrated sensor and single-photon detector.