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On the Challenges of Reliable Threshold Voltage Measurement in Ohmic and Schottky Gate p-GaN HEMTs

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ABSTRACT For large scale testability of p-GaN HEMTs it is essential to investigate threshold voltage (V_{th}) instability from the perspective of the measurement induced instability. In this paper the impact of accumulated gate bias stress during standard transfer characteristic measurements (I_D-V_G) in a p-GaN AlGaN/GaN-on-Si normally off HEMT is quantitatively analysed and modeled. This illustrates the associated threshold voltage (V_{th}) instabilities and leads to a better understanding of the V_{th} measurement challenges of a p-GaN HEMT. Upon an application of a constant gate bias close to nominal V_{th} the drain current I_D shows an initial marginal rise, followed by a short stable period ($I_{Dstable}$-T_{zone}) and a steep decay period. The effective bias history built on the gate stack varies when pulse on-time (Ton) or step time (Tstep), corresponding to pulsed or DC step I_D-V_G measurements, are varied. We find that this can lead to a V_{th} variation of up to 20%. It is also observed that the choice of Ton and Tstep determines whether I_D is measured in $I_{Dstable}$-T_{zone} or the rise or decay periods. Measurement induced V_{th} instability is attributed to trapping of 2DEG electrons at the AlGaN barrier and we demonstrate that an ohmic gate contact, in comparison to the Schottky gate contact, may compensate for the trapped 2DEG electrons by hole injection across the AlGaN barrier. Experimental results of V_{th} stability under the same stress conditions for a Schottky and ohmic gate contact are supported by a detailed TCAD analysis.

INDEX TERMS V_{th} measurement induced V_{th} instability, HEMT V_{th} measurement technique, Schottky/ohmic gate, TCAD model.

I. INTRODUCTION

Gallium Nitride, normally-off High Electron Mobility Transistors (HEMTs) are expected to make a huge impact in power electronic applications [1], [2]. Among various normally off HEMT architectures p-GaN gate AlGaN/GaN-on-Si structures have gained considerable commercial traction and studies are underway to understand and engineer an optimum, reliable gate stack [3]–[5]. Threshold voltage (V_{th}) instabilities are consistently reported under on/off state operational stress [6] and are often attributed to the charge imbalance created in the p-GaN region [7], [8] or AlGaN region [9]–[11] of the gate stack. The charge imbalance is caused by trapping or de-trapping of electrons or holes in these layers.

While the stress induced V_{th} instability has been studied in the literature, the impact of the gate bias occurring during V_{th} measurement on V_{th} itself has not been investigated as extensively [12].

In this study, building on our previous findings [13], we disaggregate the key I_D-V_G measurement parameters that have an impact on V_{th} estimation and thereby promote better understanding of measurement induced V_{th} instabilities. This work provides an insight into the underlying dynamic effects occurring during the gate bias and is based on extensive measurements of commercially available p-GaN HEMTs and TCAD modeling. It is important to note that in mass manufacturing, during wafer acceptance test (WAT) procedures, it is a common practice to vary measurement time and measurement voltage ranges (e.g., $0.5V_{th}$ to $1.5V_{th}$) to adjust throughput. However, in this paper we show that variations in the measurement time and the gate bias history induce a significant change in the reading of the V_{th} value. We

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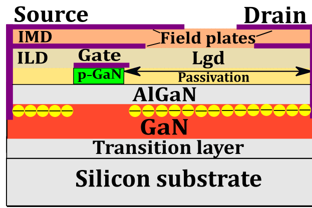


FIGURE 1. Standard normally off p GaN gate AlGaN/GaN HEMT structure.

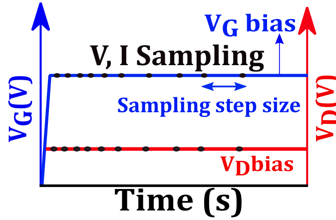


FIGURE 2. Illustration of drain current sampling at fixed gate bias (V_G bias).

illustrate further that the characteristics of this effect can vary significantly depending on the gate-stack technology used by different manufacturers.

II. EXPERIMENTAL METHODS

650V, 200mΩ, p-GaN gate AlGaN/GaN-on-Si normally off HEMTs (Fig. 1) with a Schottky gate contact (Type A) and nominal V_{th}=1.3V are primarily used in this study. Type A HEMT comprises 60-80nm thick Mg doped pGaN layer,15-25nm AlGaN layer and ∼ 5um GaN epi layer grown on a Silicon substrate with an intermediate transition layer. Type A HEMT is based on 650V TSMC technology [2]. A second set of p-GaN gate AlGaN/GaN-on-Si normally off HEMTs with an ohmic gate contact (Type B) are used in some experiments for comparison. Type B HEMTs are commercially available devices from Infineon [14]. The normalized gate leakage current (at V_G=3V, V_{DS}=50mV) of Type B HEMTs is 2 to 3 orders of magnitude higher, compared to Type A HEMTs. This is expected as the gate contact is ohmic rather than Schottky [15].

In one experiment, the Type A HEMT is subjected to a gate bias (V_G bias) of 1.5V and drain bias (V_D bias) of 50mV for 180 minutes and the corresponding drain current (I_D) is sampled at varied time intervals as illustrated in Fig. 2. The choice of V_G bias is such that it is ∼10% greater than the nominal V_{th}. At this bias level the channel starts to turn-on and the effects of low-level gate bias on I_D, and therefore the channel 2DEG concentration, can be observed. Based on these measurements we can begin to understand the effect of equivalent accumulated gate bias during transfer characteristic sweep (I_D-V_G) up to the V_{th} value. The sampled I_D over time as plotted in Figs. 3 & 4 shows a significant I_D decay trend exemplifying the possible impact of low voltage gate bias history on I_D measured during I_D-V_G.

For p-GaN HEMTs V_{th} is commonly estimated by a constant current technique (10uA/mm) using pulsed I_D-V_G

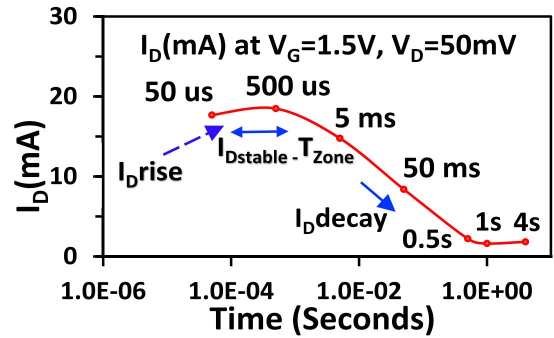


FIGURE 3. I_D sampling at $V_{G bias}$ 1.5V show $I_{Dstable}$-T_{zone} (100-500us), Type A HEMT.

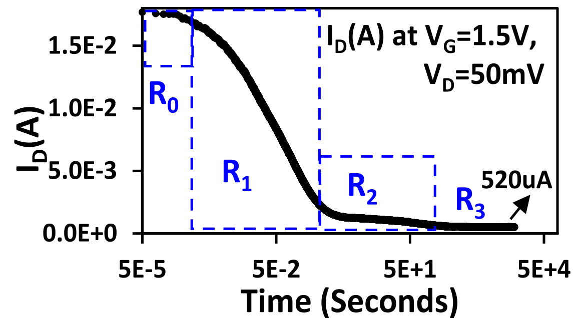


FIGURE 4. I_D sampling at $V_{G bias}$ showing varied slopes of I_D in Type A HEMT.

(Fig. 5) or DC step I_D-V_G (Fig. 6) measurement. Pulse on-time (Ton) and DC step size (Tstep) are the key parameters that affect the gate bias history developed during pulsed and DC step transfer characteristic measurements respectively. The impact of Ton, Tstep on I_D, and thereby V_{th} is illustrated by measuring V_{th} for various Ton Tstep values ranging from 100us to 50ms. The measurement delay time (Tmede) is fixed at Ton/2 for pulsed and Tstep/2 for DC step measurements respectively. In both pulsed and DC step measurements a sweep range of 0 to 3V with 3mV step is used. The effect of Ton, Tstep on V_{th} extracted using constant current technique from pulsed and DC step I_D-V_G measurements in Type A and Type B HEMTs are plotted in Fig. 7, 8 and 9, 10 respectively.

Finally, DC step I_D-V_G hysteresis and loop measurements (5x consecutive I_D-V_G sweep) are performed in both samples (Fig. 11, 12-(a)(b)). Sweep ranges are limited to 3V in the hysteresis and loop measurements to remove the effect of high gate voltage stress which is not the focus of this study.

III. RESULTS AND DISCUSSION

A. QUANTIFYING EFFECT OF TRANSFER CHARACTERISTIC MEASUREMENT ON THRESHOLD VOLTAGE

The drain current (I_D) sampling over time (Fig. 2 & 3) at V_G bias of 1.5V and V_D bias of 50mV for Type A HEMT reveals a) an initial rise period where I_D marginally rises b) a stabilization period (100-500us) ($I_{Dstable}$-T_{zone}) where

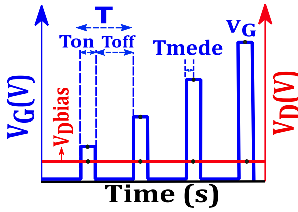


FIGURE 5. Illustration of pulsed I_D-V_G transfer characteristic measurement.

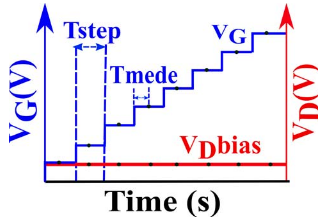


FIGURE 6. Illustration of DC step I_D-V_G transfer characteristic measurement.

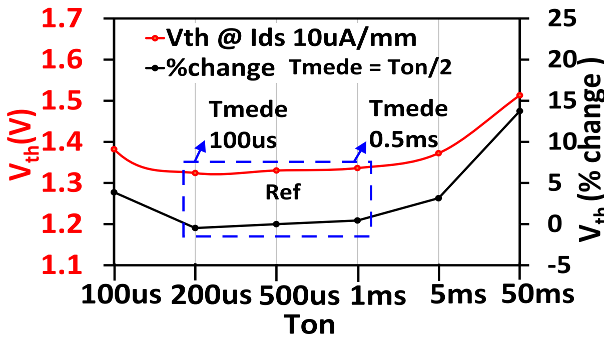


FIGURE 7. Impact of Ton on V_{th} measured from pulsed I_D-V_G in Type A HEMT.

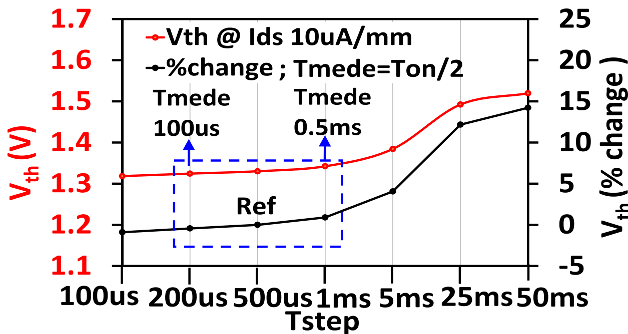


FIGURE 8. Impact of Tstep on V_{th} measured by DC step I_D-V_G in Type A HEMT.

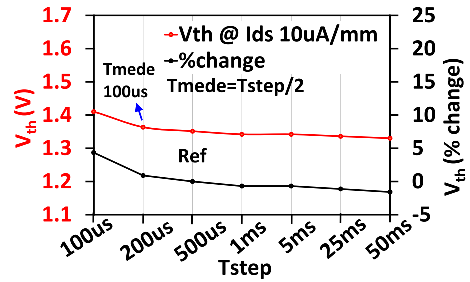


FIGURE 9. Impact of Ton on V_{th} measured by pulsed I_D-V_G, Type B HEMT.

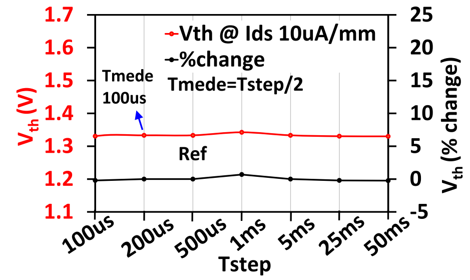
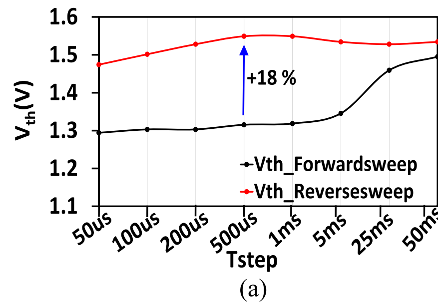


FIGURE 10. Impact of Tstep on V_{th} measured by DC step I_D-V_G, Type B HEMT.



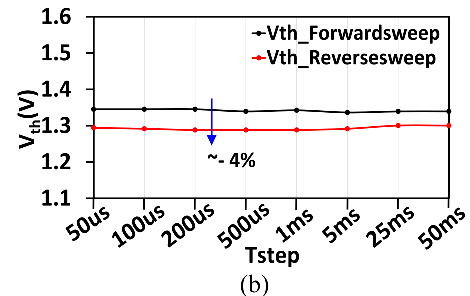


FIGURE 11. Effect of hysteresis alongside Tstep on V_{th} extracted by DC step I_D-V_G measurements on Type A HEMT (Fig. 11a) and Type B HEMT (Fig. 11b).

I_D stabilizes at 18mA and c) a fall period where I_D significantly decays to 520uA (-97%) at 180 minutes. The initial rise period observed is attributed to the gate voltage bias rise time limitations of the measurement equipment. The significant decay observed in I_D is analysed in more detail in Section III-D.

In the pulsed I_D-V_G measurements when Tmede < $I_{Dstable}$-T_{zone} (<100us) or Tmede> $I_{Dstable}$- T_{zone} (>500us) the I_D measured at each V_G bias point during I_D-V_G sweep, corresponds to the rise or fall period. During these periods I_D values are smaller leading to higher (5-20%) extracted V_{th} values as illustrated in Fig. 7. When Tmede is within $I_{Dstable}$-T_{zone}(= 100us, 250us & 500us) the I_D measured is within the stabilization period where I_D values are relatively larger leading to a lower measured Vth explaining the trend observed in Fig. 7. Similar behavior is observed for DC step

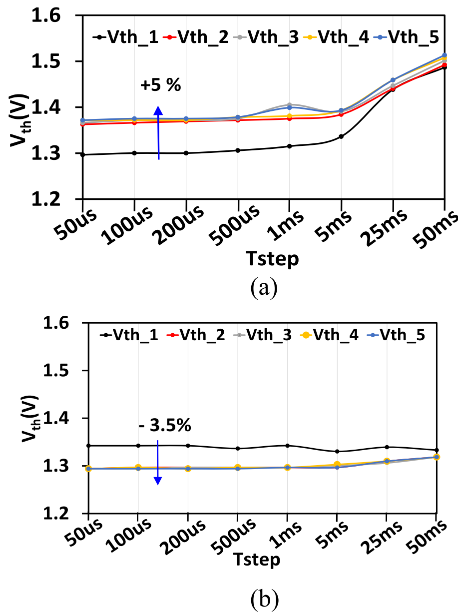


FIGURE 12. Effect of 5x looptests alongside Tstep on V_{th} extracted by DC step I_D-V_G measurements on Type A HEMT (Fig. 12a) and Type B HEMT (Fig. 12b).

I_D-V_G measurements. However, in DC step measurements there is no Toff period and hence the bias stress is more cumulative, making it harder to interpret especially when Tmede < $I_{Dstable}$-T_{zone}. In DC step I_D-V_G measurements when Tmede> $I_{Dstable}$- T_{zone} (>500us), V_{th} extracted is higher (5-15%) than values extracted when Tmede is within $I_{Dstable}$- T_{zone} as observed in Fig. 8.

As these results illustrate, V_{th} is a hard parameter to define in Schottky p-GaN HEMTs. As such, and similar to the Dynamic Ron effect [16], Dynamic V_{th} is becoming the subject of investigation in application conditions [17] where any adverse effects (e.g., false turn-on, increased reverse conduction losses) caused by the instability of the Schottky pGaN gate are of great interest.

In summary, to measure V_{th} of p-GaN gate HEMTs with a Schottky contact (Type A) reliably, the following procedure was followed in this study.

1) Identify $I_{Dstable}$-T_{zone} by biasing gate (V_G bias) at a voltage 10% greater than expected V_{th} and by sampling I_D over time (0-5s). The I_D transients and thus $I_{Dstable}$-T_{zone} can vary depending on the gate stack composition and processes.
2) Choose Ton (Tmede) in pulsed I_D-V_G measurements within $I_{Dstable}$-T_{zone} or Tstep (Tmede) in DC step I_D-V_G measurements less than or within $I_{Dstable}$-T_{zone}.

A recommended simplified methodology to measure the V_{th} of p-GaN Schottky gate HEMTs would be to use DC step I_D-V_G measurements and sweep the gate bias as fast as possible. That means Tstep selected should be as short as the measurement equipment permits. This simplified approach will extract the lowest possible nominal V_{th} which is a parameter of great interest when designing to avoid the possibility of false turn-on due to oscillations in the gate loop.

B. COMPARISON WITH TYPE B DEVICE OF DIFFERENT GATE STRUCTURE

Type B HEMTs when subjected to V_G stress bias of 1.5V and V_D bias of 50mV for 180 minutes have a constant I_D, unlike Type A HEMTs (Fig. 3 & 4). It is also observed that variations of Ton, Tstep in pulsed I_D-V_G measurements and DC step I_D-V_G measurements have negligible to no effect on V_{th} as illustrated in Fig. 9 & 10. This absence of threshold voltage instability in ohmic gate HEMTs is expected as there is no time dependent I_D variation with constant gate bias. This suggests that the ohmic gate contact is preferable from the perspective of I_D-V_G measurement induced V_{th} stability. Nonetheless, a considerable proportion of commercially available normally off p-GaN HEMTs have Schottky gate contacts to minimize gate leakage and minimize the current through the driver circuit.

C. HYSTERESIS AND LOOP TEST RESULTS

To better understand the underlying trapping/detrapping mechanisms occurring in the gate stack, hysteresis measurements having a consecutive forward and reverse I_D-V_G sweep (0 to 3V & 3 to 0V) and loop tests having 5 consecutive I_D-V_G sweeps (5x 0 to 3V) are used. From hysteresis measurements it is observed that V_{th} of Type A HEMTs in forward sweep is smaller than in the reverse sweep (Fig. 11(a)) implying a gate bias induced positive (+ve) V_{th} shift. In Type B HEMTs, the V_{th} in the forward sweep is larger than in the reverse sweep (Fig. 11(b)) implying a negative (−ve) V_{th} shift. 18% positive V_{th} shift is observed in Type A HEMT when Tstep is within $I_{Dstable}$-T_{zone} whereas the relative V_{th} +ve shift reduces when Tstep > $I_{Dstable}$-T_{zone} as reference V_{th} during forward sweep itself increases (Fig. 11(a)). When Tstep is within $I_{Dstable}$-T_{zone}, during forward sweep, I_D measured corresponds to unstressed phase resulting in a nominal lower V_{th}. However, in the following reverse sweep the gate stack is already stressed by the preceding forward sweep, a condition resulting in a higher V_{th}. In contrast, in Type B the HEMTs the small negative V_{th} shift stays constant at ∼-4 % irrespective of Tstep, agreeing with earlier observations.

Positive and negative V_{th} shifts, for Type A and B HEMTs respectively, are also observed in the loop tests. V_{th} stabilizes for the second sweep in both cases as illustrated in

Fig. 12(a), 12(b). However, when Tstep > $I_{Dstable}$- T_{zone} for Type A HEMT the +ve V_{th} shift observed is relatively smaller, similar to the observation in the hysteresis test.

D. PHYSICAL UNDERSTANDING

A schematic band diagram across the gate stack of Type A HEMTs is shown in Fig. 14(a). The band diagram

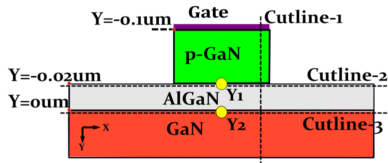


FIGURE 13. Cross sectional view of the gate stack showing cutlines-1,2,3, pGaN/AlGaN interface point Y1 and AlGaN/GaN-buffer interface pointY2.

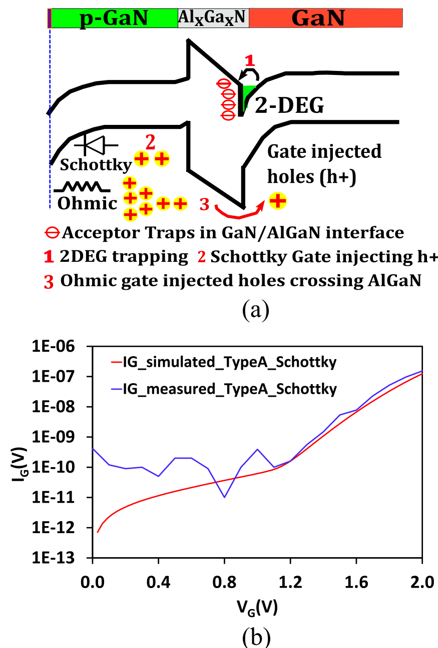


FIGURE 14. (a) Band diagram along cutline-1 p-GaN/AlGaN/GaN gate stack at V_G bias 1.5/2V showing trapping of 2DEG electrons in the AlGaN/GaN interface. (b) Simulated/experimental I_G-V_G curve of Type A HEMT.

illustrates the suspected mechanisms leading to the device behavior presented in this study. Fig. 14(a) depicts acceptor traps present at the AlGaN/GaN interface [18]. When a low forward voltage bias is applied 2DEG electrons are trapped in these interface traps causing the significant I_D decay observed during time periods R0, R1 in Fig. 4.

The I_D decay rate reduces in time (R2 in Fig. 4) due to

a) an increase in the interface trap occupancy reaching full occupancy levels.

b) an increase in the negative space charge at AlGaN/GaN interface screening the field pull from gate side.

c) a reduction in the overall 2DEG density with time.

In the case of the ohmic gate HEMTs (Type B), under similar gate bias conditions the significant I_D decay is not observed. This may be due to a reduced acceptor trap presence at the AlGaN/GaN interface in Type B devices by a different manufacturer. A second, potentially compounding, effect is that high hole injection from the gate during gate bias over time facilitates hole movement across the AlGaN barrier (Fig. 14a) and adds net positive charge in the

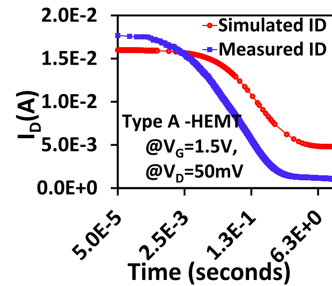


FIGURE 15. Simulated/Experimental I_D curve of Type A HEMT at V_G bias of 1.5V.

GaN buffer leading to 2DEG accumulation causing a negative V_{th} shift as observed in hysteresis tests and loop tests of type B HEMTs (Fig. 11b, 12b).

E. TCAD MODELING AND VALIDATION

To validate the physical understanding, a Technology Computer Aided Design (TCAD) model of Type A device has been developed. More details about the base TCAD model are given in [4]. In the model, a Schottky gate metal contact with a work function of 4.65eV and a hole tunneling mass 0.22 is used. The gate leakage current in the Schottky contact is modelled by creating a non-local mesh enabling electron and hole barrier tunnelling. By varying hole tunnelling mass, the ohmicity of the gate contact is controlled. A thermionic emission model is defined across the gate stack to model the leakage over both the Schottky barrier and the heterojunction barrier. The simulated gate current is matched with the measured gate current of Type A (Schottky) devices as shown in Fig. 14b. It is to be noted that at voltages below 1.1V the measured I_G is dominated by the noise from the measurement. Above 1.2V the simulated I_G (Tmh=0.22) starts to match the measurement well up to 2V, which is the area of focus in this study. Acceptor traps with a uniform density of $2x10^{19}$ cm^{-3} and activation energy 170 meV are introduced in the pGaN region to simulate the Magnesium (Mg) doping. A Guassian distribution of acceptor traps to simulate the Mg out-diffusion in the AlGaN layer is also introduced [6]. Acceptor traps at AlGaN/GaN interface are uniformly introduced between 0.15eV to 0.45eV below the conduction band with a density $3.5x10^{12}$ cm^{-2} and capture cross section $5x10^{-20}$ cm^2. A transient simulation for a V_G stress bias of 1.5V, 2V for 15 seconds at V_D=50mV is performed. It is observed that the simulated curve follows the experimental curve trend, as illustrated in Figs. 15 and 16. The marginal mismatch of the current levels in Fig. 15, 16, 17 are likely attributed to approximations in the interface trap energy, trap density used in the TCAD simulations.

To better understand the effect of the gate contact on the V_{th} shift, transient simulations are performed where the ohmicity of the gate is increased by:

a) changing the gate contact type to ohmic (to relate to the gate contact in Type B devices).

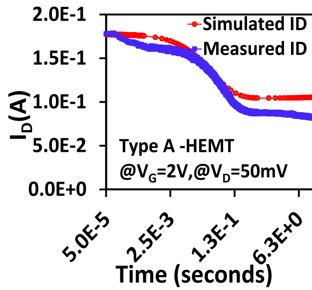


FIGURE 16. Simulated/Experimental I_D curve of Type A HEMT at V_G bias of 2V.

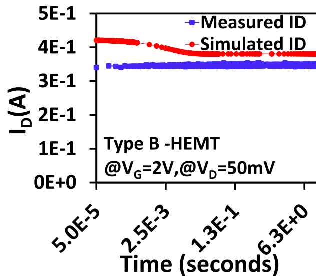


FIGURE 17. Simulated/Experimental I_D curve of Type B HEMT (Ohmic gate) at V_G bias of 2V.

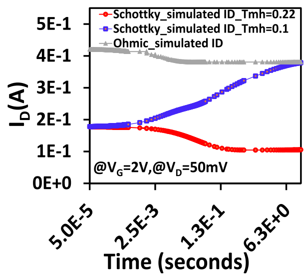


FIGURE 18. Simulated I_D curve at V_G bias of 2V of TCAD model with ohmic gate contact (Type B), Schottky gate contact (Type A, Tmh=0.1, 0.22).

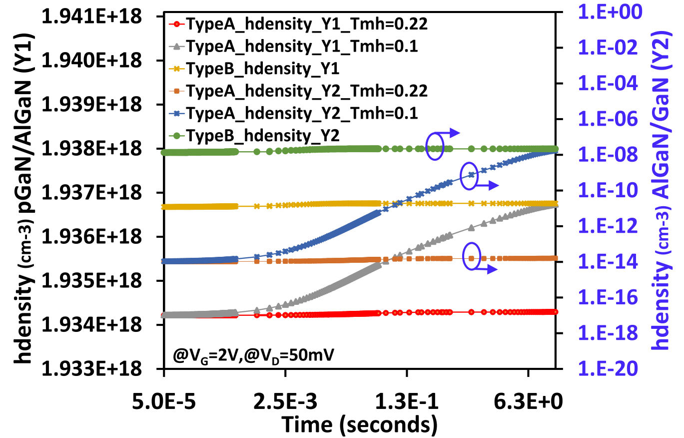


FIGURE 19. Hole density at pGaN/AlGaN interface (Y1), AlGaN/GaN interface (Y2) of Schottky gate model (Type A) and ohmic gate model (Type B).

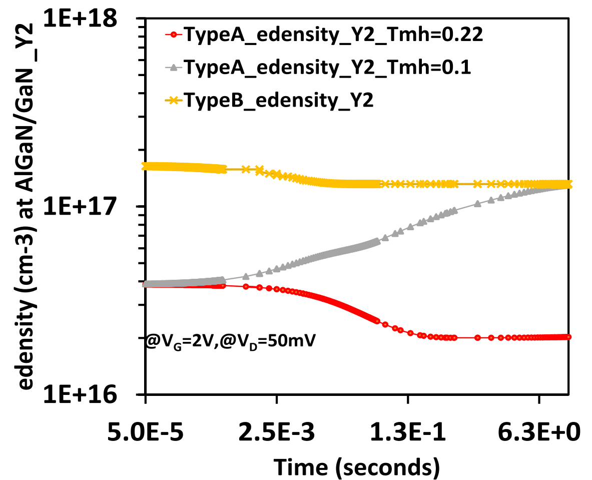


FIGURE 20. Electron density at AlGaN/GaN interface (Y2) of Schottky gate model (Type A) and ohmic gate model (Type B).

b) reducing the hole tunneling mass (Tmh) of the Schottky gate (from Tmh=0.22 to Tmh=0.1). This model represents an interesting case in-between the Schottky (Tmh=0.22) and ohmic gate and leads to better understanding of the different mechanisms at play. Other parameters are kept unchanged.

When the gate ohmicity is increased dramatically by changing the contact type to ohmic (similar to Type B device) it is observed that the initial simulated I_D (at V_G=2V) is higher compared to the Schottky gate TCAD models (Fig. 18).

The comparison between the simulated ohmic gate device and the measured result for Type B device is shown in Fig. 17. In the simulated ohmic case, after an initial mild decay, the I_D reaches a steady value at 2.5ms (Fig. 18). The decay observed in simulations is associated with the 2DEG electron trapping at the AlGaN/GaN interface. The hole gas at the pGaN/AlGaN interface directly correlates to the 2DEG density [19] and a portion of the gate injected holes add to this, which explains relative higher I_D levels for ohmic gate (Type B) at same voltage conditions (Fig. 18).

In the TCAD model where tunneling mass is reduced from Tmh=0.22 to Tmh=0.1, the initial I_D value is identical to the Tmh=0.22 value (and lower than the ohmic gate value). Nonetheless, the I_D transient simulations at fixed V_G bias for the Tmh=0.1 model no longer reveal an I_D decay as in Fig. 18. Rather, I_D starts to increase (after 2.5ms) signifying an increase in 2DEG density at the channel as seen in Fig. 20.

The quantity of holes supplied by the gate contact increases with the ohmicity of the gate, leads to accumulation at the pGaN/AlGaN interface, and eventually holes crossing the AlGaN barrier. The hole density increases with time, both close to the pGaN/AlGaN interface (Y1) and AlGaN/GaN interface (Y2), for the Type A device with Tmh=0.1 as illustrated in Fig. 19.

In the simulation, we can monitor the edges of the Schottky contact depletion region at different times during

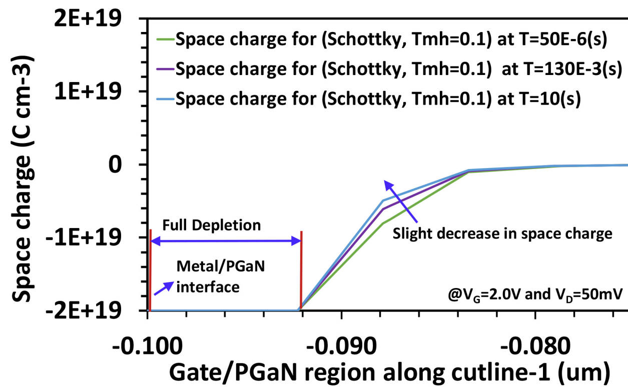


FIGURE 21. Simulated space charge across the gate/p-GaN region for type A devices (Tmh=0.1) along cutline −1 at V_G=2.0V, V_D=50mV at various time instances (50us, 130ms and 10s) showing the boundary of the depletion region.

the fixed V_G bias by monitoring the space charge in the region. We observe that the edge of the depletion remains almost constant or shows a marginal retraction over time in the case of the Schottky contact with tunnelling mass 0.1, as illustrated in Fig. 21. This suggests that the holes added to the 2DHG over time do not originate from any charge redistribution in this depletion region but rather come from the gate hole current, as the depletion region width marginally retracts, rather than expand, with time. Accumulation of holes can occur in the pGaN layer and at the pGaN/AlGaN interface over time, as the hole current from the Schottky gate terminal and the hole current over the heterojunction barrier are not necessarily matched. This may explain the marginal retraction in the Schottky contact depletion region. No change in the depletion region boundary was observed in the simulation with tunnelling mass Tmh=0.22.

In the case of Tmh=0.1 the I_D over time (>6s) settles at a higher constant value. This constant value matches the equivalent steady state value of the ohmic gate model I_D (Fig. 18). In the case of the ohmic gate, the supply of holes from the gate terminal is relatively high from the start, reaching a steady state value much earlier or instantaneously (Fig. 19).

These observations imply coordinated, time-matched changes in hole density (at Y1) and electron density at the AlGaN/GaN interface (at Y2) which are strongly controlled by the ohmicity, and therefore hole current supplied, of the gate contact. The TCAD simulations with reduced Tmh=0.1 and ohmic gate support the proposed theory that the ohmic gate contact facilitates higher hole current from the gate terminal, leading to additional holes at the pGaN/AlGaN interface as well as holes crossing the AlGaN barrier and compensating the 2DEG acceptor trapping. Furthermore, TCAD simulations also illustrate that the effect of hole current from the gate terminal on the transient I_D (and therefore perceived V_{th}) is faster for a relatively more ohmic contact.

To summarize, three time-dependent mechanisms are identified as crucial components of the V_{th} instability:

1) 2DEG electron trapping at the AlGaN/GaN interface traps due to field pull from gate side (Fig. 20).

2) hole current from the gate terminal and accumulation at the pGaN/AlGaN interface (Y1 axis of Fig. 19).

3) holes crossing the AlGaN barrier, thus changing the charge balance and attracting additional electrons to the 2DEG. Holes crossing the AlGaN barrier cause a six order of magnitude increase ($1x10^{-14}cm^{-3}$ to $1x10^{-8}cm^{-3}$) in hole density at the AlGaN/GaN interface (Y2 axis of Fig. 19) for the type A device with tunnelling mass Tmh=0.1. The hole density values observed at a gate bias voltage of 2V are not very significant compared to the other charges illustrated. However, as the gate bias increases this hole density will grow exponentially, due to the forward biasing of the heterojunction diode. This hole density may play a significant role in conductivity modulation at higher gate bias values as reported originally in [20].

With sufficient time at a fixed gate bias (t>6s), the three mechanisms lead to an equilibrium reaching a constant I_D value. The time-dependent effects listed are more prominent at gate voltage bias close to the threshold voltage where 2DEG density is lower and the interface acceptor traps are less likely to reach full occupancy.

Relating the TCAD findings to the experimental results we can understand the following:

1) In a Type A device, a significant I_D decrease in time is observed. This suggests that the effect of trapping at the AlGaN/GaN interface is dominating and the gate terminal hole current effect is negligible. This of course agrees with the more Schottky gate contact of the Type A device.
2) In a Type B device, a constant I_D is observed which is reflected in a fairly stable V_{th} extraction. A small reduction in extracted V_{th} is observed compared to a fresh device. The TCAD modelling suggests that the small reduction in extracted V_{th} may relate to accumulation of holes at the pGaN/GaN and AlGaN/GaN interface and is related to the magnitude of hole current from the gate terminal. The significant I_D decrease is not observed in Type B samples. This may be due to a reduced acceptor trap density at the AlGaN/GaN interface as they are devices from a different manufacturer with a different gate stack. Additionally, the I_D decrease may be suppressed by the counteracting effect of the increased hole current from the ohmic contact as demonstrated in the simulations.

IV. CONCLUSION

We have quantified threshold voltage measurement (I_D-V_G) induced V_{th} instability and proposed an approach to understand and mitigate it in normally off p-GaN Schottky gate HEMTs. Ton in pulsed I_D-V_G, Tstep in DC step I_D-V_G are critical parameters that control the gate bias history experienced and need to be chosen such that the measurement of the drain current, I_D, happens within a stable time zone

(identified via a demonstrated drain current sampling technique) for obtaining a nominal stable V_{th}. We suggest that the threshold voltage instability observed is attributed to electron trapping at the AlGaN/GaN interface. Furthermore, we show that the higher hole current from the gate terminal in ohmic gate HEMTs, compared to Schottky gates HEMTs, may counter compensate the electron trapping resulting in negligible or no threshold instability due to the stress of the threshold voltage measurement. These findings are based on extensive experimental results and are supported by TCAD modelling.

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