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Core-Shell Dual-Gate Nanowire Memory as a Synaptic Device for Neuromorphic Application

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ABSTRACT In this work, a synaptic device for neuromorphic system is proposed and designed to emulate the biological behaviors in the novel device structure of core-shell dual-gate (CSDG) nanowire flash memory. Floating-body effect in the device and charge trapping/de-trapping in the nitride layer are found to be effective for short-term potentiation (STP), long-term potentiation (LTP), and long-term depression (LTD), respectively. STP realizes a temporary potentiation in the artificial neural network, and it can transit to LTP through the process of rehearsal and meaningful association. The transition takes place at the 10th pulse in a permissibly optimized CSDG synaptic device. The proposed device shows a stronger capacitive coupling between the dual gates, which forms a deeper potential well for charge storing and achieves better memory performance metrics such as sensing margin and retention time. The series of results reveal that the synaptic memory device is applicable to neuromorphic system due to the stronger gate controllability, multi-level weight adjustability, and Si processing compatibility.

INDEX TERMS Synaptic device, neuromorphic system, core-shell dual-gate, nanowire, flash memory, short-term potentiation (STP), long-term potentiation (LTP), and long-term depression (LTD), Si processing compatibility.

I. INTRODUCTION

In order to overcome the issues of von Neumann architecture and increasing demand on the parallel computing capability, neuromorphic computing is increasingly gaining interest in recent days [1], [2]. In the neuromorphic system, memory components play the key role in storing the weights and communicating with the neuron circuits [1]–[13]. Synaptic plasticity is also one of the essential properties of human nervous system for the energy-efficient learning and memory [3]. Short-term plasticity is utilized for keeping the information for a short time with discrimination by duration of data (input frequency) while long-term plasticity provides the function of storing data for a long time. The synaptic behaviors can be realized by different types of memory devices [4]–[14].

Among these, two-terminal devices have the great resemblance with the biological synapse but lack of completeness in realizing the full functions, and in many cases, the Si-processing compatibility is not practically considered [4], [11]. In order to overcome these issues, Si-processing-based synaptic memory devices with combination of volatile and nonvolatile memories have been demonstrated as a promising candidate owing to their higher in functionality for synaptic operation reliabilities [5], [6], [7]–[10]. Floating-body effect can be utilized for the short-term potentiation (STP) function and charge trapping in the nitride layer realizes the long-term potentiation (LTP) and depression (LTD) functions. The unique feature of this type of device lies in that the generated charges in the body can be trapped in the charge-trap layer, which effectively realizes the transition from short-term to long-term memory. The previously reported multi-gate synaptic devices might face the short-channel effects (SCEs) in the nanoscale regime. For overcoming the nonideal effects,

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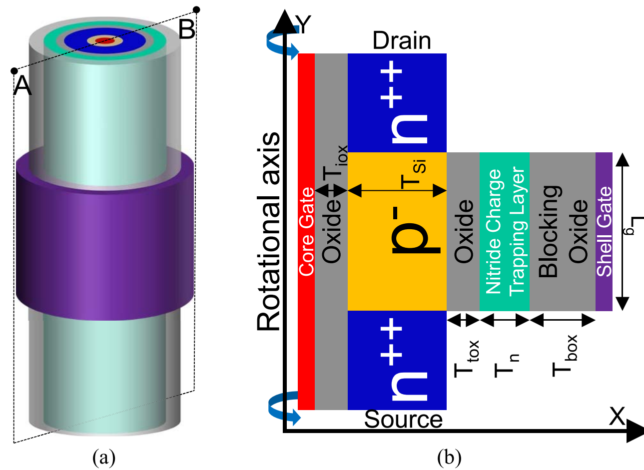

FIGURE 1. **Schematic of the CSDG synaptic flash memory. (a) 3-D aerial view of the device structure and (b) cross-sectional view along the A-B plain in (a).**

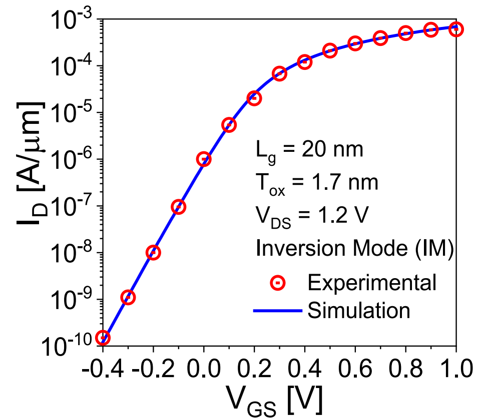

FIGURE 2. **Calibration of the simulated transfer curve with the experimental data of a MOSFET device operating in the inversion mode.**

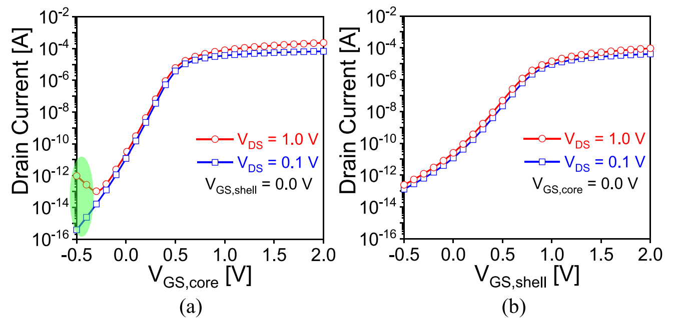

FIGURE 3. **Dual-gate operations of the synaptic memory device. Transfer characteristics at V_{DS} = 0.1 V and 1 V. (a) I_D-$V_{GS,core}$ curves at $V_{GS,shell}$ = 0 V. (b) I_D-$V_{GS,shell}$ curves at $V_{GS,core}$ = 0 V. L_g = 100 nm and T_{Si} = 20 nm.**

a novel core-shell gate-all-around (GAA) synaptic device and its synaptic performances were reported [15]–[18].

In this paper, we design and characterize core-shell dual-gate (CSDG) nanowire flash memory capable of the synaptic operations of STP, LTP, and LTD by series of technology computer-aided design (TCAD) simulations [19]. The effects of interval time between pulses on the transition from short-term to long-term memory are closely investigated. In addition, the impacts of change in workfunction of the core gate on the synaptic operations are examined. Operation schemes and the device parameters are adjusted for a optimum device performance.

II. DEVICE DESIGN AND SIMULATION RESULTS

A. DEVICE STRUCTURE AND SIMULATION APPROACHES

Fig. 1(a) shows the three-dimensional (3-D) schematic of the CSDG nanowire memory capable of synaptic operations. Fig. 1(b) shows the cross-sectional view of the device along the cut-plane adjoining points A and B in Fig. 1(a). The gate length (L_g) and the Si channel thickness (T_{Si}) are 100 nm and 20 nm, respectively. The inner gate oxide thickness (T_{iox}) is 2 nm. Also, thicknesses of tunneling oxide (T_{tox}), nitride charge-trap layer (T_N), and blocking oxide (T_{box}) were designed to be 2 nm, 4 nm, and 6 nm, respectively. The channel and source/drain doping concentrations are 10^{15} cm^{-3} and 10^{20} cm^{-3}, respectively. Core (inner) and shell (outer) gates are dually operated and their workfunctions can be adjusted to localize the band-to-band tunneling for potentiation, more specifically for generation of holes in the floating body. Workfunctions of core and shell gates are 4.6 eV and 4.8 eV, respectively. Also, the hole retention can be effectively increased by adopting the dual-gate structure [15], [16], [18]. Multiple models were simultaneously activated in the simulation works, including Shockley-Read-Hall generation and recombination model, bandgap narrowing model, Lombardi's mobility model, Auger recombination model, density-gradient quantum effect model, trapping and de-trapping models, non-local band-to-band calculation, impact ionization model, hot carrier injection model, Fowler-Nordheim tunneling model, and Poole-Frenkel emission model. The parameters in the simulation models were precisely adjusted by iterative calibration of the simulated current-voltage characteristics with the experimental results as shown in Fig. 2 [20].

B. PRELIMINARY VALIDATION OF THE MEMORY OPERATIONS

Figs. 3(a) and (b) show the transfer characteristics of the proposed synaptic memory device at drain voltage (V_{DS}) of 0.1 V and 1 V in order to verify the dual-gate operations. It is evident from the comparison between Figs. 3(a) and (b) that smaller subthreshold swing is obtained when core gate voltage ($V_{GS,core}$) is swept due to the thinner dielectric thickness. The transient accumulation and depletion of carriers out of the floating body across the potential walls provide the short-term memory function that can be usually found in the conventional one-transistor dynamic random-access memory (1T DRAM) [21]–[26].

Fig. 4(a) shows the variation in hole concentration (p) and potential (V) along the channel direction during a read (inference) operation. Δp and ΔV indicate the difference in hole

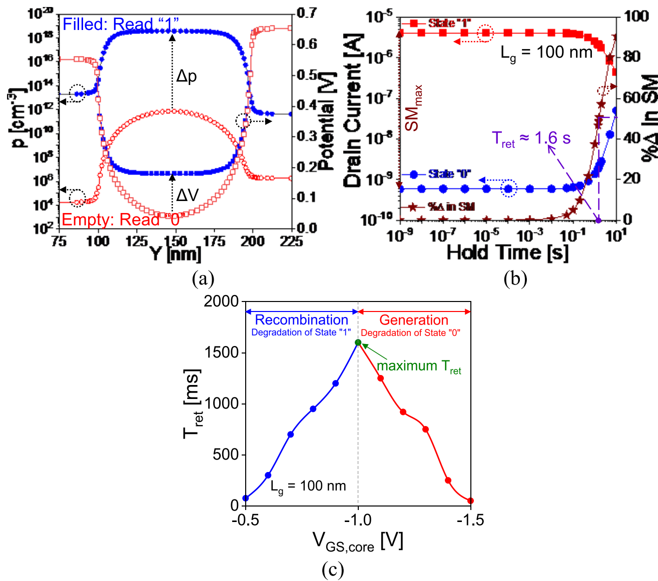

FIGURE 4. **Carrier distributions and memory device performances. (a) Distribution of hole concentration and potential along the channel direction during a read (inference) operation. Δp and ΔV indicate the changes in hole concentration and potential between state 1 and state 0. (b) Sensing margin (SM) and percentage change in SM as a function of hold time for estimating the retention time (T_{ret}). (c) Optimization of core gate voltage ($V_{GS,core}$) during hold operation to control the generation and recombination of carriers. Variation of T_{ret} with core gate voltage during hold operation.**

concentration and potential between state 1 and 0, respectively. The generation and confinement of holes in the potential well are based on band-to-band tunneling and drift by a forward bias, respectively [21]–[28]. Fig. 4(a) confirms that the accumulation (depletion) of holes in the potential well increases (lowers) the potential for read 1 (0) operation, which eventually increases (decreases) the state 1 (0) read current as depicted in Fig. 4(b). The difference between state currents can be termed as sensing margin (SM) and the retention time can be defined as the time when 50% of the maximum SM (initial SM value) is reached [21]–[33]. Fig. 4(b) shows the change in state currents and the percentage change in SM. The results show that the synaptic memory device in the CSGD structure achieves a long retention time (T_{ret}) of ~1.6 s with current ratio (CR (I_1/I_0)) of 10^4 at a hold voltage of $V_{\text{GS,core}} = -1.0$ V. The retention time of 1T DRAM cell is based on charge generation and recombination of the carriers in the device and it can be controlled through device design, bias and time during operations (write, erase, hold, and read) [21]–[33]. Hold voltage is a crucial parameter, which controls the diffusion and recombination of the carriers during the hold operation, and thus, need to be optimized to get longer retention time. Fig. 4(c) shows the variation of retention time with core gate voltage during hold operation. Fig. 4(c) confirms that state "1" is degraded due to the recombination of carriers (SRH recombination due to shallower potential depth) when the gate bias is increased in the positive direction, while the

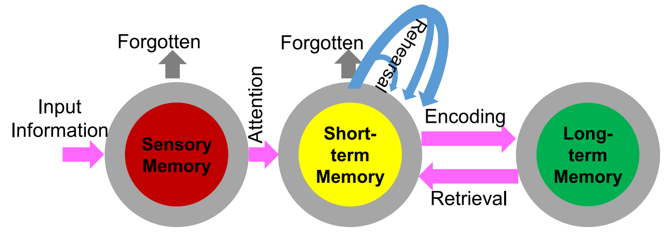

FIGURE 5. **Mechanism of short-term to long-term memory transition [34].**

generation of carriers (due to thermal generation and BTBT) is dominant and degrades the state "0" retention when the gate bias is moved in the negative direction.

C. CORE-SHELL DUAL-GATE SYNAPTIC MEMORY OPERATIONS

In order to verify the synaptic characteristics of the proposed device, pulse operations have been performed for the synaptic learning – potentiation and depression. These functions are realized by storing holes in the floating body and trapping/detrapping them in the nitride layer [5], [7]–[10], [12]. The short-term to long-term memory transition is achieved by repeated stimuli, which is analogous to rehearsal for human nervous system. Increase in the number of pulses is associated with hole generation in the floating body near the core gate. Accumulation of holes generated by pulses of which the interval is shorter than time for diffusion out of the body to either source or drain junction increases the probability for holes occupying the higher energy states into the nitride layer. The charges trapped in the nitride are retained for a long time even when the synaptic pulses are no more present. In this manner, short-term-to-long-term memory transition which can be schematically shown by the model proposed by Atkinson and Shiffrin in Fig. 5 [34], is artificially realized in a hardware. Figs. 6(a) and (b) show the set of voltage waveforms for potentiation and depression operations, respectively. Repeated pulses with both signal width and interval time of 2 μs are applied to demonstrate the learning procedures of the memory device. This pulsed voltage scheme can be derived from the operation of 1T DRAM devices.

The band-to-band tunneling mechanism for accumulating the holes allows one to expect low power consumption and high device reliability. Fig. 6(c) depicts the drain current (I_D) and the amount of trapped charge over the repeated potentiation pulses, as a function of time. At the 10th pulse, drain current shows a sharp increase and the amount of charge trapped in the nitride starts to show a step-like increase. This is the location, minimum number of pulses, where the short-term to long-term memory transition takes place. Fig. 6(d) shows the drain current and the amount of trapped charge over the repeated depression pulses, as a function of time. The envelope of the drain current shows a monotonic decrease, which reveals that the synaptic weight, or equivalently, the electrical conductivity, gradually decreases

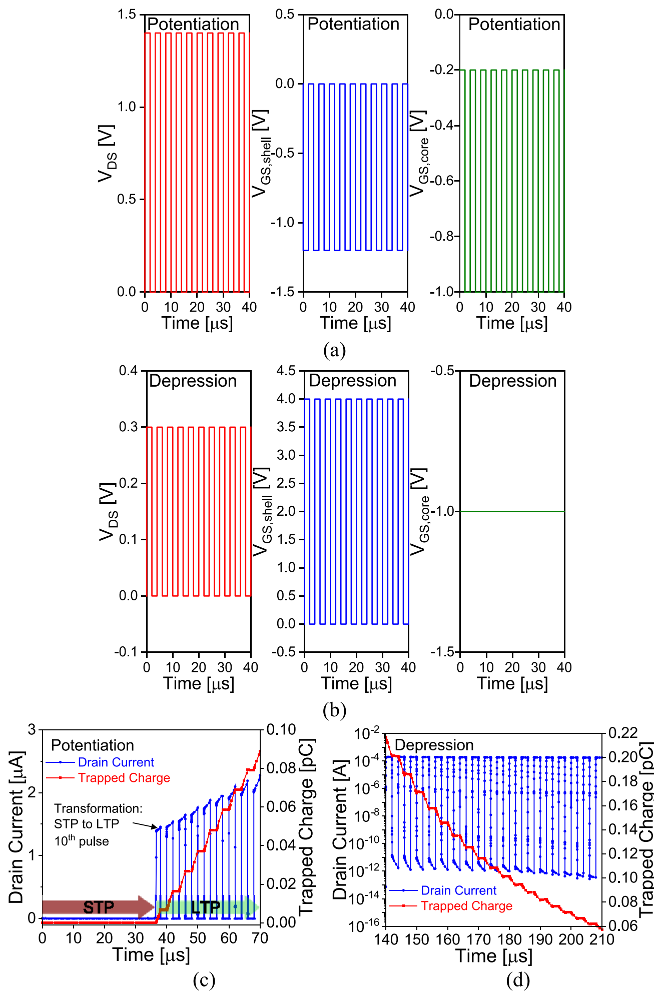

FIGURE 6. Pulse operations of the synaptic memory device. Set of voltage waveforms for (a) potentiation and (b) depression operations. Transient current analysis and the amount of trapped charge in the nitride over (a) potentiation and (b) depression pulses.

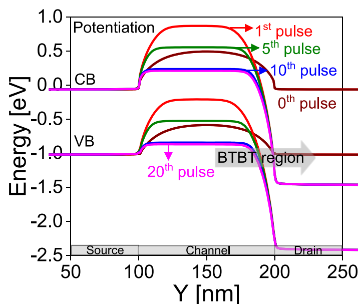

FIGURE 7. Change in the energy-band diagram during the pulsed potentiation operation. Lowering of the conduction band minimum (CB) and valence band maximum (VB) at different number of pulses: no pulse, 1st, 5th, 10th, and 20th pulses.

along with decrease in the amount of charge trapped in nitride. The energy-band diagrams during potentiation operation have been extracted along a cutline 1 nm below the core gate oxide at different number of potentiation pulses: no pulse, 1st, 5th, 10th, and 20th pulses. Fig. 7 shows that the combination of negative $V_{GS,core}$ and positive V_{DS} sets up a condition in which the band-to-band tunneling can easily occur and the that the electron potential energy in the channel is lowered by the accumulated holes (smaller number of pulses) and trapped ones (larger number of pulses). At the 10th pulse and above, the conduction band minimum (CB) and valence band maximum (VB) do not show a significant lowering since most of the band lowering has been predominantly determined by the amount of trapped charge, which is larger than that of the accumulated charges in the floating body. The LTD operation is based on hot electron injection into the nitride layer through FN tunneling. Here, hot electron does not specifically mean an accelerated electron with a high velocity but more formally means a high-temperature electron that occupies a higher energy state in the Fermi-Dirac distribution, not necessarily accompanied by lateral field-induced acceleration. The increase in number of depression pulses reduces the amount of hole trapped in nitride (weight) gradually without a rather complicated scheme [35]–[37].

Fig. 8 shows the variation of charges in the nitride layer during potentiation and depression operation with different interval times (Fig. 8(a) for 2 μs, Fig. 8(b) for 10 μs, Fig. 8 (c) for 100 μs, and Fig. 8 (d) for 10 ms). It is evident from the figure that charges in the floating body generated by longer interval pulses cannot be injected into the nitride layer since it is hard for the generated charges to be accumulated to occupy the higher energy states before they vanish by diffusion or recombination in a short time. Figs. 9(a)–(d) show the transfer characteristics and transient analysis during inference (read) operation. Fig. 9 demonstrates the short-term to long-term memory transition and weight tunability under different learning conditions with different pulse interval times of 2 μs, 10 μs, 100 μs, and 10 ms. When the device is in the STP state (up to 9th pulses), I_D is unchanged from the initial value (no pulse) for all the interval times as shown in Fig. 9(a). From the 10th potentiation pulse, for all the interval times, increase in number of pulses increases I_D, which explicitly proves that the holes are trapped in the nitride. However, for interval time of 100 μs, the change in I_D is significantly reduced and eventually becomes indistinguishable for interval time of 10 ms since the interval times are too long for the holes in the floating body to tunnel into the nitride layer before they vanish by fast diffusion. Thanks to core-shell structure that helps construction of a deeper potential well, the synaptic memory device can achieve LTP for longer interval time. In the similar manner, the interval time-dependent depression operation characteristics are shown in Fig. 9(b). It becomes less probable for the electrons to tunnel into the nitride layer if a sufficiently short interval time is not warranted, which eventually leads to negligibly small changes in threshold voltage in the transfer curves as shown in Fig. 9(b). The results in Figs. 9(a) and (b) can be mapped into the time domain analysis as demonstrated in Figs. 9(c) and (d). As previously shown, LTP is achieve at the 10th potentiation pulse for all the simulated interval times. From the time-domain

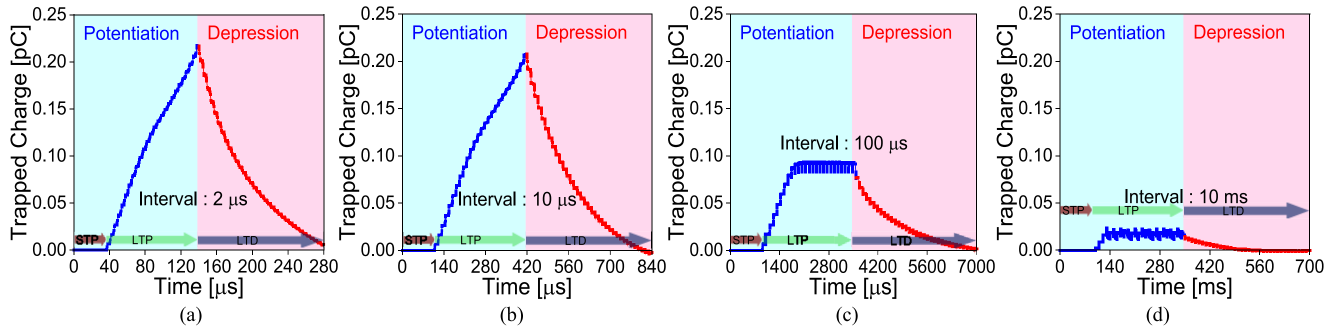

FIGURE 8. Trapped charges in the nitride layer during potentiation and depression for interval of (a) 2 μs, (b) 10 μs, (c) 100 μs, and (d) 10 ms.

analysis, if the synaptic memory device remains in the STP, I_D can increase for a short time after a potentiation pulse is applied but it decays to the value in case that no pulse is applied (initial). As can be traced by the pink curves in Fig. 9(c), by the loss of holes accumulated in the floating body by an expedited diffusion process. On the other hand, if the device is brought into the LTP (10th or more pulses), the initial I_D's at $t = 0^+$ asymptotically approach steady-state values which are distinguishably higher than the value in case that no pulse is applied. The electrical conductivities, or synaptic weights, are retained for longer than 10^4 s since they are determined by the holes semi-permanently trapped in the nitride layer. For longer interval time, due to the fast carrier diffusion, the amount of weight change decreases and the transition from STP to LTP becomes hard to take place. LTD is realized by de-trapping the holes from the nitride layer by a proper set of depression biasing scheme, the synaptic device loses memory gradually and continuously, no matter how long the interval time might be as depicted in Fig. 9(d).

It has been also found that the STP-to-LTP transition depends on workfunctions of the dual gates. Energy-band diagrams of the device with variation in the workfunction of core gate ($\varphi_{m,core}$) are drawn in Fig. 10(a) while that of shell gate ($\varphi_{m,shell}$) is fixed to 4.8 eV. Larger $\varphi_{m,core}$ deepens the quantum well for hole, and thus, can induce the accumulation of more holes as shown in Fig. 9(a). Higher concentration of accumulated holes has an effect of increasing the electric field across the channel as shown in Fig. 10(b). The energy-band diagrams and the electric fields were extracted 1 nm below the core gate. Fig. 10(c) shows the variation of trapped charges in the nitride layer with increase in repetitive pulse for core gate workfunction of 4.5 eV and 4.6 eV. This confirms that due to increase in gate workfunction increases the electric field (Fig. 10(b)), which increases the tunnelling in the device and thus, the LTP is achieved at lower pulse. Fig. 10(d) shows the smallest number of potentiation pulses by which STP-to-LTP transition occurs as a function of $\varphi_{m,core}$. Due to the increase in electric field between channel and drain junction induced by larger $\varphi_{m,core}$, the band-to-band tunneling probability increases and the minimum number of pulses required for the transition decreases monotonically as depicted in Fig. 10(d).

TABLE 1. Comparison among metrics for volatile memory functions of the reported 1T DRAM devices and the proposed CSDG synaptic device.

Ref.	L_T* [nm]	T [°C]	SM [μA/μm]	T_{ret} [ms]	CR [I_1/I_0]	WT [ns]
[21]	200	27	4.54	0.01	2.5	500
[23]	100	27	9	1000	266	1,000
[29]	200	27	1	5	1	500
[30]	250	85	0.2	500	10^2	50
[30]	250	85	0.03	0.001	2×10^5	50
[31]	300	27	60	30	2×10^4	200
[32]	100	85	60	20	1.5	10
[33]	90	27	7	---	4.5	200
This work	100	27	5	1,600	10^4	2,000

L_T* indicates the total length: length between source and drain.

Table 1 shows the comparison of our results with with the performances of the published 1T DRAM cells. It is evident from the table that the proposed CSDG nanowire transistor achieves the best retention time. The speed of the memory is estimated through write time (WT) and it is defined as the requirement of maximum time to perform the operation while current ratio (CR) is estimated through (I_1/I_0) [22], [27]. Core-gate helps to construct deeper potential well compared with conventional double-gate transistor, which enhances the retention of state "1", and thus, retention time of the memory [23], [29]. In comparison with tunnel field-effect transistor [30], CSDG nanowire transistor achieves better sensing margin and retention time due to lower diffusion and recombination probabilities in the device. In comparison with Z^2-FET [31], our results demonstrate better retention time and comparable current ratio with shorter gate length. Junctionless device has shallower potential depth and shorter carrier lifetime due to higher doping [27], [32], and they are not capable of achieving longer retention time compared with the proposed CSDG device. In comparison with [21], [33], CSDG device achieves higher current ratio and longer retention time. Thus, the results confirm that CSDG nanowire transistor is suitable for next-generation 1T DRAM and neuromorphic synaptic transistor applications. Table 2 represents the comparison of performance metrics between the synaptic devices in reports and the proposed one [5], [38]–[45]. The capability of short-term potentiation (STP) is mostly found in

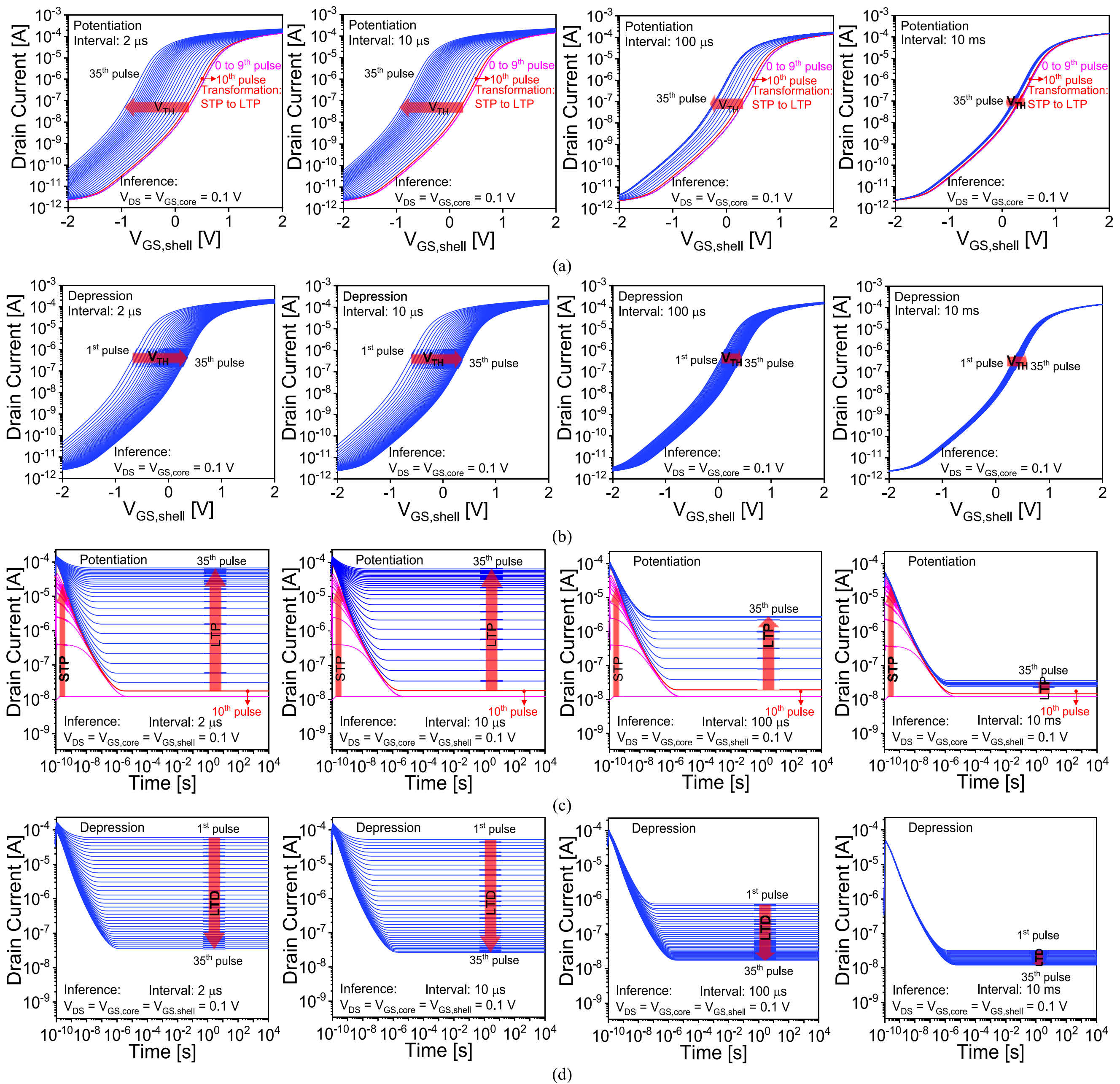

FIGURE 9. **Transfer characteristics and transient analysis results of the CSDG nanowire synaptic memory device during inference (read) operation for identifying the short-term and long-term memories. Transfer curves over (a) potentiation and (b) depression pulses with different pulse interval times of 2 μs, 10 μs, 100 μs, and 10 ms. Transient analyses for validating weight changes of the synaptic memory over (c) potentiation and (d) depression pulses with different pulse interval times of 2 μs, 10 μs, 100 μs, and 10 ms.**

the charge-trap devices in case that the charge reservoir is either physically or electrically floating [5], [38]–[40]. On the other hand, the synaptic devices based on emerging nonvolatile memories are focused on realization of multiple-weight long-term potentiation in many cases [41]–[45]. The minimum number of pulses by which STP-to-LTP transit takes place might not be critical in the sense that it can be controlled by the pulse profile and time interval. The proposed synaptic device is capable of STP, LTP, and LTD, and shows relatively small magnitude of maximum potentiation voltage. The prominent advantage of the CSDG nanowire synaptic transistor lies in the extremely low inference energy. While the synaptic devices based on emerging nonvolatile memories still have room for further reduction in inference energy consumption, Si devices with floating channel and charge-trap storage node demonstrate relatively low power consumption. The proposed synaptic device shows even lower power consumption for inference compared with one of the most recently reported devices by one order magnitude [5].

TABLE 2. Comparison of performance metrics among CSDG nanowire synaptic transistor and those reported in recent publications.

Ref.	STP capability / Min. number of pulses for STP-to-LTP transit	Max. potentiation voltage [V]	Inference Energy [J]	Mechanism for synaptic weight modulation
[5]	STP applicable / 3 pulses required	7	7.66×10^{-16}	Charge trap / de-trap
[38]	STP applicable	4	1×10^{-11}	Charge trap / de-trap
[39]	STP applicable / 7 pulses required	2	1×10^{-6}	Charge trap / de-trap
[40]	STP applicable	8	9×10^{-8}	Charge trap / de-trap
[41]	STP not applicable	1	1×10^{-8}	Stochastic switching
[42]	STP not applicable	-4.4	5.5×10^{-16}	Ferroelectric switching
[43]	STP not applicable	15	7.92×10^{-5}	Ferroelectric switching
[44]	STP not applicable	5	3×10^{-8}	Resistive switching
[45]	STP not applicable	7	1.21×10^{-14}	Phase changing
This work	STP applicable / 10 pulses required	4	2.48×10^{-17}	Charge trap / de-trap

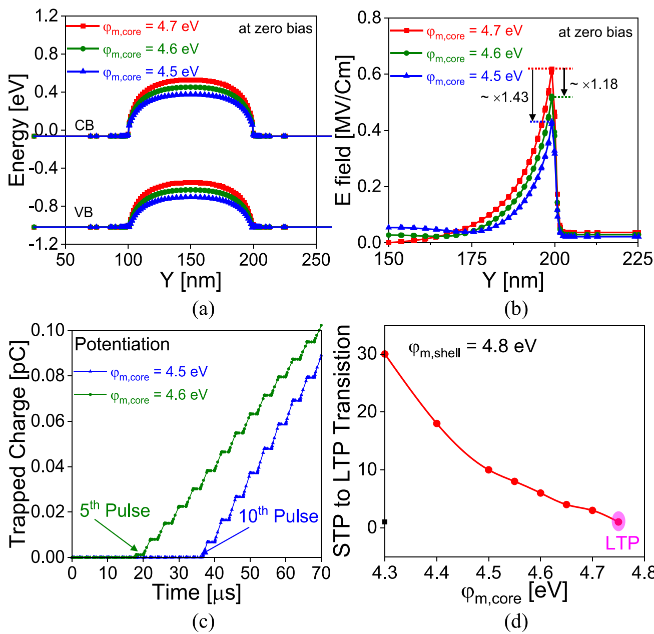

FIGURE 10. Workfunction dependency. Variation of (a) Energy-band diagram and (b) Electric field (E field) along the channel direction for different core gate workfunctions ($\phi_{m,core}$) at zero bias condition with fixed shell gate workfunction ($\phi_{m,shell}$). (c) Variation in trapped charges in the nitride layer to observe the transition pulse with different core gate workfunctions. (d) Number of pulses required for the transit from STP to LTP. CB and VB indicate conduction band minimum and valence band maximum, respectively.

III. CONCLUSION

In this work, core-shell dual-gate (CSDG) nanowire memory has been proposed, designed, and characterized by series of simulation works to highlight its applicability as a synaptic device in the neuromorphic system. It has been confirmed that the CSDG synaptic device is highly suitable for the realization of biological synaptic functions including STP, LTP, and LTD. The effective hole confinement by introducing dual gates with different workfunctions helps managing the number of potentiation pulses for the short-term-to-long-term memory transition. Both short-term memory for filtering the low duration information and long-term one with accurate weight tunability for long duration information make the proposed synaptic device a promising component toward highly energy-efficient neuromorphic system.

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