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On the Critical Role of Ferroelectric Thickness for Negative Capacitance Device-Circuit Interaction

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ABSTRACT This paper demonstrates the critical role that Ferroelectric (FE) layer thickness (t_{FE}) plays in Negative Capacitance (NC) transistors connecting device and circuit levels together. The study is done through fully-calibrated TCAD simulations for a 14*nm* FDSOI technology node, exploring the impact of t_{FE} on the figures of merit of n-type and p-type devices, voltage transfer characteristic (VTC) and noise margin of *inverter* as well as the speed of *buffer* circuits. First, we analyze the device electrical parameters (e.g., I_{ON}, SS, I_{ON}/I_{OFF} and C_{gg}) by varying t_{FE} up to the maximum level at which hysteresis in the I-V characteristic starts. Then, we analyze the deleterious impact of Negative Differential Resistance (NDR), due to the drain to gate coupling, demonstrating how it imposes an additional constraint limiting the maximum t_{FE}. We show the consequences of NDR effects on the VTC and noise margin of inverter, which are essential components for constructing robust clock trees in any chip. We demonstrate how the considerable increase in the gate's capacitance due to FE seriously degrades the circuit's performance imposing further constraints limiting the maximum t_{FE}. Further, we analyze the impact of t_{FE} on the SRAM cell static performance metrics such hold noise margin (HNM), read noise margin (RNM) and write noise margin (WNM) at supply voltages of 0.7V and 0.4V. We demonstrate that the HNM and RNM in a NC-FDSOI FET based SRAM cell are higher then those of the baseline FDSOI FET based SRAM cell noise margin and further increase with t_{FE}. However, the WNM in general follows a non monotonic trend w.r.t t_{FE}, and the trend also depends on the supply voltage. Finally, we optimize the design of the SRAM cell considering overall performance metrics. All in all, our analysis provides guidance for device and circuit designers to select the optimal FE thickness for NCFETs in which hysteresis-free operations, reliability, and performance are optimized.

INDEX TERMS SRAM, reliability, FDSOI, NDR.

I. INTRODUCTION

Negative Capacitance FET (NC-FET) is one of the most promising devices for future low-power applications [1], [2]. Recently, NC-FET has been experimentally demonstrated to achieve a steep sub-threshold swing that goes below 60mV/dec with high (I_{ON}/I_{OFF}) ratio [3]. The properties of NC-FETs such as improved SS, Drain-Induce Barrier Rise (DIBR), and Negative Differential Resistance (NDR) with device scaling, are often opposite to conventional FETs. This has recently attracted a large attention in several research areas [4]. When it comes to low-power applications, the Fully Depleted Silicon on Insulator (FDSOI) technology is one of the main choices for circuits' designers due to its inherent higher electrostatic controllability [5]. FDSOI

technology can be even more efficient and further scaled down if it is augmented with the negative capacitance technology. This can be realized by replacing the conventional high-κ material inside the gate's stack (HfO_2) with an FE layer (e.g., $Hf_{0.5}Zr_{0.5}O_2$) [6]. In existing literature, limited study has been done on NC-FDSOI. Based on TCAD study, [6] has showed that the ultra-thin body NC-FDSOI can achieve a sub 60mV/decade *SS* at the room temperature. Reference [7] has experimentally demonstrated the impact of NC-induced voltage amplification on lowering *SS* and improving I_{ON} in NC-FDSOI in comparison to conventional FDSOI devices. Importantly, existing state of the art is mostly limited to the device level when exploring the impact of FE thickness. In this work, we demonstrate the different aspects at both device and circuit levels that inevitably limit the maximum possible thickness of FE layer. The 6T SRAM cell memory cover a large portion of the chip area in the state-of-the-art system on chip. Therefore, it is valuable to scrutinize the performance of NC-FDSOI FET based SRAM cell for nano technology nodes. Here, we extend our previous work presented in [8], where we have extensively studied the impact of ferroelectric layer thickness on the device performance, voltage transfer characteristic (VTC) of the inverter (defines the noise margin), and the delay of buffer circuits. The impact of t_{FE} on the hold noise margin (HNM), read noise margin (RNM), and write noise margin (WNM) of a 6T SRAM cell at different supply voltages such as 0.7V and 0.4V is additionally included. Further, we incorporated the design guideline for high read and write noise margin of NC-FDSOI FET-based SRAM cell.

Our Key Contributions: we demonstrate how NC-FDSOI provides much better *SS* and I_{ON} than the baseline FDSOI showing that up to t_{FE} of 7nm, hysteresis-free in the electrical characteristics can be ensured. However, above t_{FE} of 3nm, the inverter VTC starts to exhibit hysteresis due to NDR effects – stemming from the $I_D - V_D$ characteristics of devices. Finally, to study the impact of NC on circuit's performance, the delay of a buffer is analyzed using TCAD simulations. We show that when t_{FE} is larger than 1.7nm, there is very little gain in performance due to the large increase in the gate's capacitance of transistors (caused by NC effect), which considerably compensates any gain from NC-induced current improvements. In other words, although a maximum t_{FE} of 7nm appeared possible when solely looking at the device level, it turns out that the actual FE thickness is limited to merely 1.7nm when it comes to the circuit speed. Further, we examine the impact of t_{FE} on the SRAM cell hold, read and write noise margins at supply voltage of 0.7V and 0.4V. The hold and read noise margin increase with increase in the t_{FE} of all the 6T SRAM cell. However the write noise margin is limited to $t_{FE} =\sim 3nm$. In addition, we analyze five different NC-FDSOI SRAM cell designs and compare their performance with the FDSOI SRAM cell. Our analysis illustrates the trade-off between different performance metrics (i.e., HNM, RNM and WNM) and provides useful guidelines for an optimum NCFET based SRAM design.

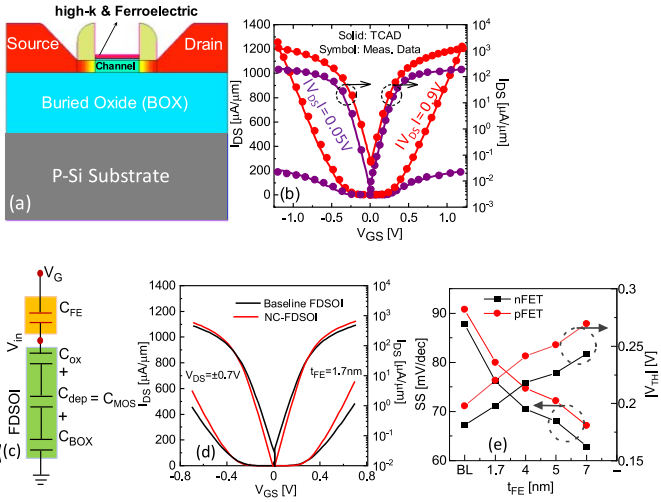

FIGURE 1. **(a) The 2D cross section view of the 14nm FDSOI. (b) The calibration of 14nm FDSOI showing the matching between TCAD results and experimental data. (c) The simple capacitance schematic of NC-FDSOI. (d) $I_D - V_G$ comparison between FDSOI and NC-FDSOI at high V_{DS}. (e) *SS* for baseline (BL) FDSOI and NC-FDSOI as a function of t_{FE}.**

TABLE 1. **Device geometrical parameters.**

L_{gate}	20 nm
L_{ext}	8 nm
t_{ox}	0.6 nm
t_{Hfo_2}	1.7 nm
t_{FE}	1.7-7nm
t_{soi}	5 nm
t_{BOX}	25 nm
EOT	1 nm

II. TCAD SETUP AND DEVICE ANALYSIS

The Synopsys TCAD tool is used to create and simulate the 14nm FDSOI device structure, as shown in Fig. 1(a). The device parameters are obtained from the experimental data [5], and the values are summarized in the Table 1. TCAD simulations have been performed to analyze the electrical properties of n/p-FDSOI devices. For proper calibration, the mobility parameters, doping profile, metal work function, and saturation velocity are carefully tuned to reproduce the measurement data in both linear and saturation regions, as shown in Fig. 1(b). NC-FDSOI is realized by depositing a FE layer ($Hf_{0.5}Zr_{0.5}O_2$) on the transistor's interfacial oxide layer, as shown in Fig. 1(a). Fig. 1(c) shows the schematic of capacitance network in NC-FDSOI. The TCAD self-consistently solves the Landau–Khalatnikov equation with the Poisson equation at every grid point in the transistor. The Landau coefficients (α, β, and γ) are extracted by fitting L-K model to an experimentally-measured *S*-shape polarization-electric field curve from [9]. The coupling coefficient for the polarization gradient ($g = 10^{-4} cm^3/F$) is used in simulations, which lies in the range of conventional ferroelectric material [10]. For fair comparisons, NC-FDSOI

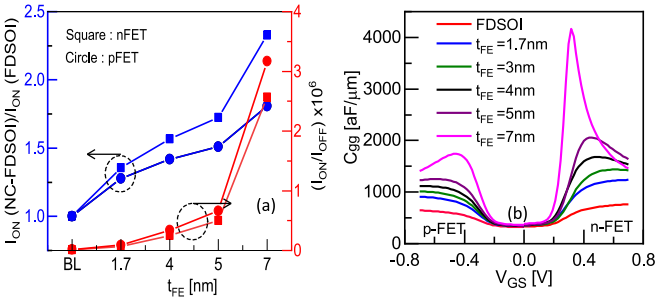

FIGURE 2. **(a) Improvements in I_{ON} and I_{ON}/I_{OFF} ratio in the NC-FDSOI with different FE thickness. Note that BL refers to the baseline FDSOI transistor. (b) Transistor gate capacitance (C_{gg}) at different t_{FE} showing the increase due to NC effects.**

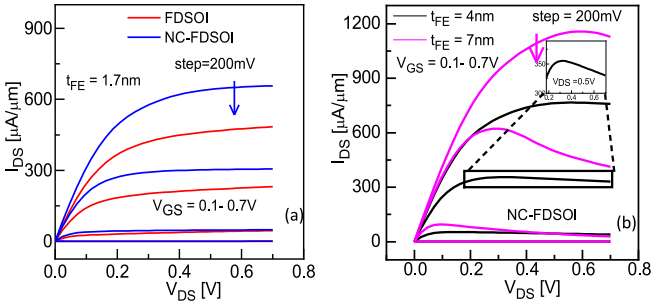

FIGURE 3. **(a) $I_D - V_D$ for both baseline FDSOI and NC-FDSOI (n-type) at the same HfO_2 thickness and FE thickness (i.e., 1.7nm) showing no NDR effects. (b) $I_D - V_D$ for NC-FDSOI at higher thickness 4nm and 7nm, demonstrating the NDR behavior, which becomes dominant across the voltage range at 7nm.**

is simulated with the same parameters used in the baseline FDSOI, except the FE parameters.

Fig. 1(d) shows the comparison of $I_D - V_G$ between the FDSOI and NC-FDSOI. NC-FDSOI shows steeper sub-threshold slope and higher I_{ON} than the baseline transistor due to NC effect [11]. Further, the improvement in *SS* and threshold voltage with increasing t_{FE} is apparent in Fig. 1(e). The *SS* for nNC-FDSOI noticeably decreases to 63mV/dec compared to the baseline transistor of 90mV/dec. Fig. 2(a) shows the boost in the NC-FDSOI current at different t_{FE} compared to the baseline FDSOI. As t_{FE} increases from the baseline 1.7nm to 7nm, the I_{ON} increases by around 2.3x and 1.8x for nNC-FDSOI and pNC-FDSOI, respectively. This leads to around 200x increase in the I_{ON}/I_{OFF} ratio between the NC-FDSOI and baseline FDSOI. Fig. 2(b) shows how NC capacitance increases with t_{FE}. Since I_{ON} and C_{gg} both increase with t_{FE} but they have a contradicting impact on the circuit's delay, designers need to carefully select the optimal FE thickness to maximize the circuit's performance. The device output characteristics $I_D - V_D$ of FDSOI and NC-FDSOI for different t_{FE} are shown in Figs. 3(a, b) in which V_{GS} ranges from 0.1V to 0.7V with a step of 200mV. Fig. 3(a) shows the case of $t_{FE} = 1.7$nm demonstrating the absence of any NDR effects. However, when t_{FE} is above 3nm, the $I_D - V_D$ starts to show the NDR behavior due to increased NC effect and drain to gate coupling [10]. This can be observed in Fig. 3(b) that presents $t_{FE} = 4$nm and 7nm cases. At 7nm, NDR effects even dominate almost the entire V_{GS} range for 0.1V to 0.7V.

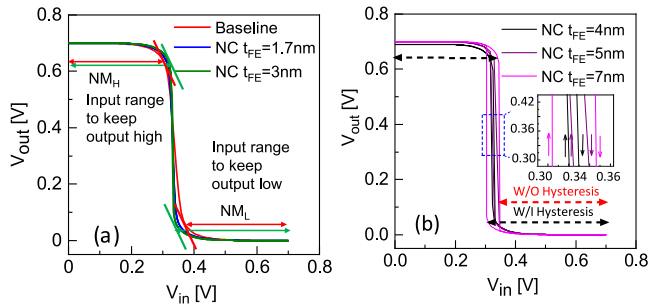

FIGURE 4. **(a) Inverter VTC curve comparison between FDSOI and NC-FDSOI inverter at t_{FE} = 1.7nm and 3nm. (b) NC-FDSOI inverter VTC for higher thickness t_{FE} = 4nm, 5nm and 7nm.**

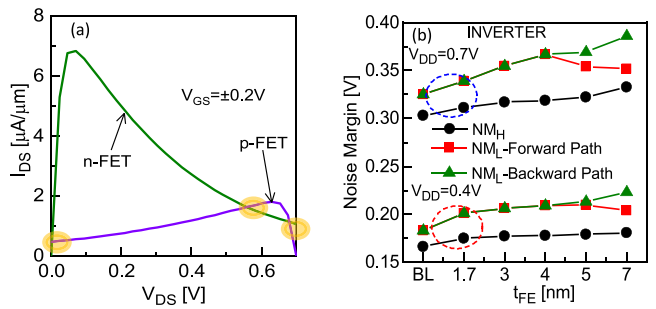

FIGURE 5. **(a) $I_D - V_D$ of n-p NC-FDSOI crossing more than one point for same input due to NDR effects. (b) FDSOI and NC-FDSOI based inverter high and low noise margins at two different supply voltages 0.4V and 0.7V.**

III. INVERTER NOISE MARGIN AND BUFFER DELAY

Fig. 4(a) shows the inverter voltage transfer characteristic (VTC) of the FDSOI and NC-FDSOI for the baseline t_{FE} of 1.7nm and, additionally, 3nm. NC-FDSOI inverter shows a sharper transition from logic '1' to '0' compared to FDSOI. This becomes more apparent at $t_{FE} >$ 3nm. Fig. 4(b) demonstrates the VTC for t_{FE}: 4nm, 5nm, and 7nm. Due to the dominating NDR at the device level, NC-FDSOI inverter exhibits a hysteresis loop [12] from t_{FE} of 4nm and above. Hence, the maximum t_{FE} should be limited to 3nm. Otherwise, a hysteresis-free operation in inverter cannot be anymore ensured. To understand better the reason of hysteresis, Fig. 5(a) shows the $I_D - V_D$ characteristic at $V_{GS} = \pm 0.2V$ of n and p NC-FDSOI superimposed on the same V_{DS} axis. The inverter VTC is extracted from the cross point of the n and p NC-FDSOI load line curves. In the conventional FET, there is a single cross point for one input voltage, but in the case of NC-FDSOI with the stronger NDR at high t_{FE}, two to three cross points are observed as shown in Fig. 5(a). Such multiple cross points induce the hysteresis behavior in the VTC of NC-FDSOI FET inverter at higher t_{FE} (i.e., > 3nm). To analyze the consequence hysteresis, we calculate the noise margin high (NM_H) and noise

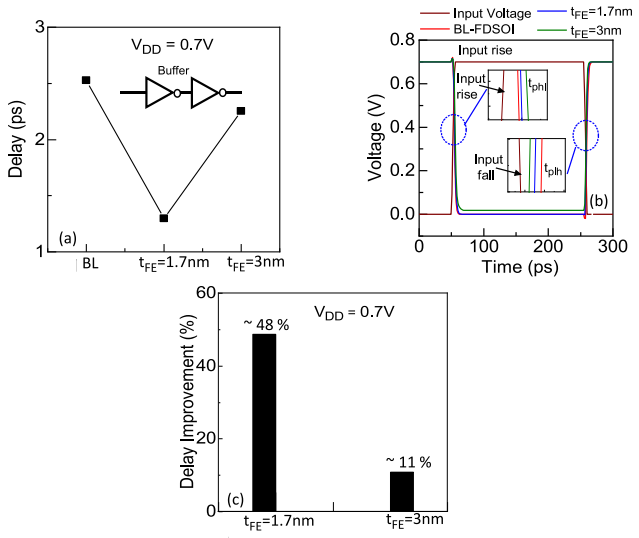

FIGURE 6. **(a) Buffer delay comparison between baseline and NC-FDSOI at t_{FE} = 1.7nm and 3nm for supply voltage of 0.7V. (b) shows the comparison of output fall and rise of the buffer. The Table II shows the absolute value of delay with oxide thickness. (c) showing how increasing the FE thickness leads to diminishing the gain in performance.**

TABLE 2. **Buffer delay comparison.**

	Buffer Delay (s)
BL=1.7nm	2.53E-12
t_{FE}=1.7nm	1.29E-12
t_{FE}=3nm	2.25E-12

margin low (NM_L) [13] for the inverter. NM_H is the range of input voltage for which the output is high as indicated in Fig. 4(a). NM_L is the range of input voltage for which the output is low as shown in Fig. 4(a). Fig. 5(b) shows the noise margin is higher in NC-FDSOI FET based inverter and it increases with an increase in the t_{FE} compared to the FDSOI inverter. The NM_H increases with an increase in t_{FE} and is higher than the FDSOI based inverter irrespective of supply voltages as shown in Fig. 5(b). The NM_L also increases at higher t_{FE}, due to hysteresis in the VTC, which makes backward path more wider. The NM_L during backward path of the NC-FDSOI inverter VTC shows higher noise margin compared to the conventional FDSOI based inverter VTC (without hysteresis).

Finally, because t_{FE} considerably impacts the transistor's gate capacitance, its impact on the circuit's performance cannot be neglected. To investigate that, we compare the delay of a buffer for both baseline FDSOI and NC-FDSOI (at t_{FE} of 1.7nm and 3nm) for 0.7V. Fig. 6(a) demonstrates that NC-FDSOI buffer has an optimal delay at t_{FE} of 1.7nm, which is the same baseline oxide thickness. Fig. 6(b) shows the delay waveform (output high to low (t_{phl}) and output low to high (t_{plh})) comparison between BL-FDSOI and NC-FDSOI based buffer. The waveform clearly indicates the impact of t_{FE} on the delay. The absolute value of the delay is indicated in the Table 2. An increase in t_{FE} from

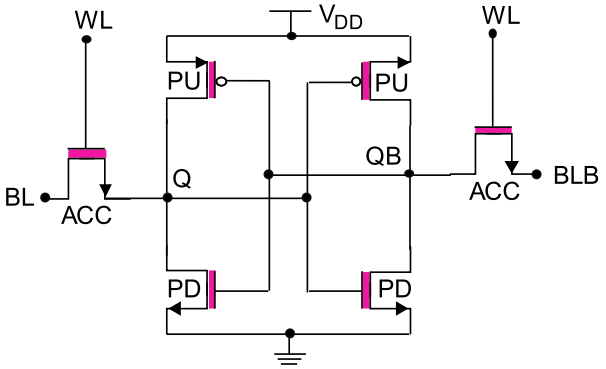

FIGURE 7. **Schematic circuit diagram of 6T SRAM cell.**

1.7nm to 3nm makes the buffer's delay noticeably increase despite the improvement in current due to the larger C_{gg} [see Fig. 2(b)]. Fig. 6(c) shows the NC-FDSOI FET buffer delay improvement compared to the FDSOI based buffer. At the same oxide thickness (1.7nm) the NC-FDSOI FET based buffer has $\sim$ 48% improvement in the delay compared to the FDSOI FET based buffer. However, at higher $t_{FE} = 3nm$, the improvement in the NC-FDSOI is merely $\sim$ 11% due to dominating capacitance.

IV. IMPACT OF T_{FE} ON THE SRAM CELL PERFORMANCE

In this section, the impact of t_{FE} (varies from 1.7nm to 7nm) on the static noise margin of NC-FDSOI FET based 6T SRAM cell is analyzed using TCAD simulations. Further, we show the design guideline for a higher read and write noise margin of NC-FDSOI FET SRAM cell compare to the FDSOI FET SRAM cell. The schematic of the 6T SRAM cell including pull-up (PU), access (ACC), and pull-down (PD) transistors is presented in Fig. 7.

A. HOLD NOISE MARGIN

The hold state of the SRAM cell is characterized by a hold noise margin (HNM). In this state, the word line (WL) is off and access transistors (ACC) are cutoff, the SRAM cell stores the complementary data at the internal storage node (Q, QB). The HNM is calculated from the side of the maximum square embedded into the butterfly curve formed by DC sweep of the input of bistable circuit composed of two cross-coupled inverters as shown in Fig. 8 [14], [15], [16]. The internal storage node Q and QB are swept to form a butterfly curve. Fig. 8(a) shows the comparison of the butterfly curve between FDSOI and NC-FDSOI (t_{FE} varies from 1.7nm to 6nm) of SRAM cells during hold state. It shows the NC-FDSOI accommodates the larger square in the butterfly curve that increases with the increase in t_{FE}. The increment in the t_{FE} leads to a sharper transition in the voltage transfer characteristic (VTC) due to reduced sub-threshold swing (SS). The internal voltage is swept in both forward and reverse directions for all the thicknesses to check the hysteresis in VTC curve. It can see from the Fig. 8(a) at higher t_{FE} (i.e., 6nm), the HNM shows hysteresis, which decreases the

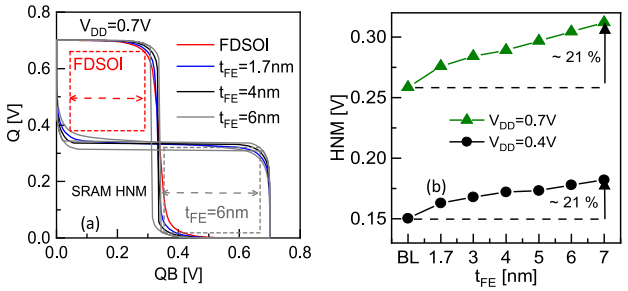

FIGURE 8. **(a) Comparison of butterfly curve between FDSOI and NC-FDSOI FET based SRAM cell during hold state. (b) shows the HNM comparison between baseline FDSOI and NC-FDSOI FET based SRAM cell at the supply voltages of 0.7V and 0.4V.**

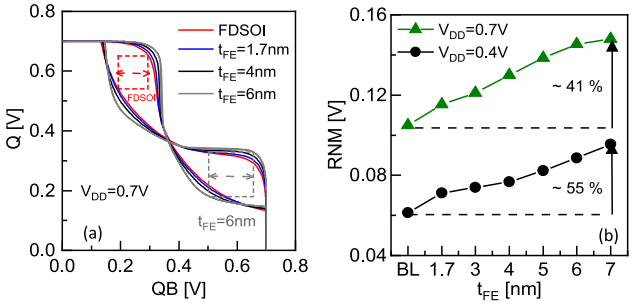

FIGURE 9. **(a) Comparison of butterfly curve between FDSOI and NC-FDSOI FET based SRAM cell during read state. (b) shows the RNM comparison between baseline FDSOI and NC-FDSOI FET based SRAM cell at the supply voltages of 0.7V and 0.4V.**

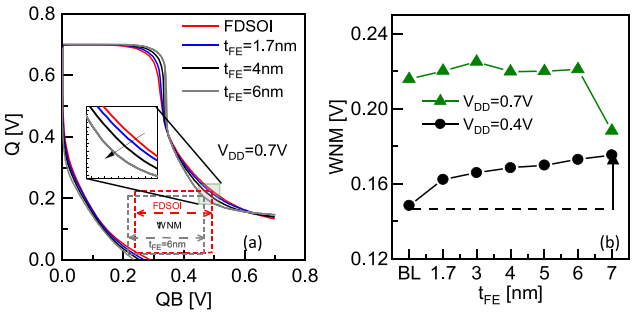

FIGURE 10. **(a) Comparison of butterfly curve between FDSOI and NC-FDSOI FET based SRAM cell during write state. (b) shows the WNM comparison between baseline FDSOI and NC-FDSOI FET based SRAM cell at the supply voltages of 0.7V and 0.4V.**

HNM value. Further, we show the HNM at two different voltages for a wide range of ferroelectric thicknesses. The HNM of NCFET based SRAM cell can be increased up to $\sim 21\%$ compared to baseline SRAM cell at a supply voltage of 0.4V and 0.7V and $t_{FE} = 7$ nm. The NC-FDSOI FET SRAM cell shows a better hold of SNM than its standard counterpart FDSOI FET based SRAM cell for all t_{FE} values.

B. READ NOISE MARGIN

The SRAM cell read stability is characterized using read noise margin (RNM). During a read operation, the internal storage nodes (Q, QB) stores the complementary data and keeping BL, BLB, and WL to V_{DD}. The RNM is calculated from the side of the larger square fitted into the eyes of butterfly curve formed using the DC sweep of the internal storing node as shown in Fig. 9. The NC-FDSOI FET-based SRAM cell accommodates a larger square compared to the FDSOI FET SRAM cell which further increases with an increase in t_{FE}. The increment in the t_{FE} leads to a higher V_{th} shift and sharper transition due to reduced subthreshold swing (SS) in the voltage transfer characteristic (VTC). Further, we present the RNM at two different supply voltages for a wide range of t_{FE} values. The RNM of NCFET based SRAM cell is increases by $\sim 41\%$ and $\sim 55\%$ compared to baseline SRAM cell at a supply voltage of 0.4V and 0.7V, respectively. The higher increment in the RNM at lower supply voltage is due to the operation of the transistor near the sub-threshold region with the sharper transition over the voltage range.

C. WRITE NOISE MARGIN

The WNM of 6T SRAM cells is evaluated by the side of the smallest square inscribed in the butterfly curve formed by the combination of read and write VTC [17]. We assume that during the write operation the internal storage node (Q (0), QB (1)) stores the complementary data, keeping BL and WL to V_{DD} and BLB biased at "0." The butterfly curve is formed by sweeping the internal storage node as shown in Fig. 10(a). Fig. 10(a) compares the butterfly curve for WNM between baseline FDSOI and NC-FDSOI FET (t_{FE} varied from 1.7 nm to 6 nm) based SRAM cells. The single cross-over point in the butterfly curves shows the successful write '1' operation. The square embedded in the butterfly curve indicated the FDSOI and NC-FDSOI FET have nearly the same WNM for larger t_{FE}. The WNM depends on the ratio of the strength of the pull-up (PU) transistor to that of the access transistor (ACC). For the acceptable write operation PU/ACC ≤ 1. As we increase the t_{FE} [from $1.7nm$ to $7nm$ in Fig. 10(b)], the PU to ACC strength ratio decreases up to $\sim 3nm$, hence the WNM increases compared to the baseline FDSOI-FET based SRAM's WNM for both the 0.7V and 0.4V supply voltage cases. At larger t_{FE} ($\geq 3nm$), the WNM starts to decrease at the higher supply voltage due to threshold voltage increment and dominating NDR [8], [18]. This increase of threshold voltage and NDR with t_{FE} increases the PU/ACC ratio, hence, decreases the WNM. It is also clearly visible from the zoomed part in the Fig. 10(a)), that for higher t_{FE} (6nm) the node voltage changes slowly (grey line). However, at larger t_{FE}, the WNM is increase with a lower supply voltage due to a smaller NDR effect.

D. SRAM CELL DESIGN GUIDELINE

In the last section, we discuss the impact of t_{FE} on the SRAM cell static noise margins and compared it with counterpart FDSOI FET-based SRAM cell performance. In this subsection, we design five different NC-FDSOI based SRAM cells

TABLE 3. NC-FDSOI FET SRAM cell design.

	Ferro Thickness (nm)		
Design	PU	ACC	PD
D1	1.7	1.7	6
D2	1.7	3	6
D3	1.7	4	6
D4	1.7	5	6
D5	1.7	6	6

as given in Table 3. The high-performance SRAM cell is designed by a certain ratio such that PD ≥ ACC ≥ PU [19]. Therefore, in these designs, the t_{FE} is varied to maintain the current drive strength of these among PU, ACC, and PD ratios. By keeping this in mind, the PU is fixed to minimum t_{FE} value, PD fixed to maximum t_{FE} value and for the access transistor t_{FE} is varied from 1.7nm to maximum 6nm value, to design high noise margins of SRAM cell design. Fig. 11(a) shows the RNM comparison between the baseline-FDSOI and different NC-FDSOI FET-based SRAM cell designs at supply voltages of 0.7V and 0.4V. For the baseline SRAM cell design, the PU, ACC, and PD transistors have the same oxide thickness (t_{HfO2} = 1.7nm). The RNM depend upon the strength ratio of PD to ACC (cell ratio CR) [20], therefore the D1 has the highest RNM with the highest CR, and RNM decreases for other designs due to increase in the ACC strength, thus decrease the CR. Fig. 11(b) shows the WNM comparison between the baseline FDSOI and different NC-FDSOI FET based SRAM cell design at supply voltages of 0.7V and 0.4V. The WNM depends upon the strength of the PU to ACC ratio (pull up ratio PR), it is as low as possible [20]. Fig. 11(b) shows the WNM is increases with an increase in the strength of the access transistor compared to the PU transistor. The designs D1 and D2 have a lower write noise margin compared to the FDSOI FET-based SRAM cell at the supply voltage of 0.7V. However, in the case of lower supply voltage, the WNM is increases from design D1 to D5 and it is higher than the BL-WNM. The hold noise margin is the same in all the design cases (0.292V) because it depends upon the strength of PU and PD. Finally, it is concluded from the above analysis that the D1 design is better for higher RNM and D5 is better for the higher WNM of NC-FDSOI FET-based SRAM cell. Overall D3 is a optimum design considering overall performance metrics, i.e., HNM, RNM, and WNM.

V. CONCLUSION

In this work, we have investigated the critical role of FE layer thickness at the device and circuit levels in NC-FDSOI. We investigated how the characteristics of individual devices as well as full inverter and buffer circuits are impacted when FE thickness increases. We showed how analysis at the device level standalone is insufficient to explore the impact of FE thickness. Our investigation demonstrated how the optimal

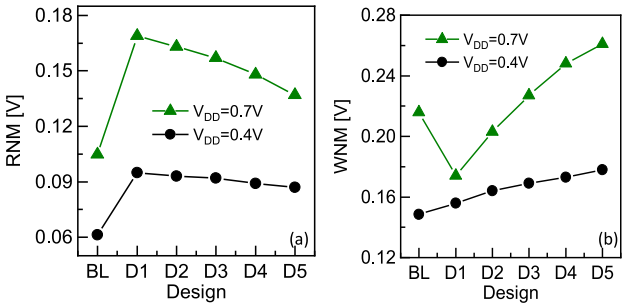

FIGURE 11. (a-b) Show the RNM and WNM at different design point using NC-FDSOI based SRAM cell compared with FDSOI based SRAM cell at supply voltage of 0.4V and 0.7V.

FE thickness drops from 7nm (which is the maximum thickness that ensures hysteresis-free operation at the device level) to 3nm at the inverter level (due to the hysteresis in the VTC) down to merely 1.7nm at the buffer level (due to performance loss induced by capacitance increase). Finally, we have investigated the impact of t_{FE} on the SRAM cell hold, read and write noise margins at supply voltage of 0.4V and 0.7V. We found that the hold and read noise margin increase with increases in the t_{FE}. The WNM increases upto t_{FE} =∼ 3nm and thereafter it decreases for higher t_{FE} values. We also demonstrated that in the NCFET technology, SRAM cells for different performance requirements (i.e., HNM, RNM and WNM) can be designed by using different ferroelectric thickness combinations for the pull up, access and pull down transistors. Overall, our analysis provides many useful guidelines to optimize device-circuit co-design in the NCFET in comparisons to convectional FinFET technology.

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