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An Inclusive Structural Analysis on the Design of 1.2kV 4H-SiC Planar MOSFETs

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ABSTRACT A detailed structural analysis of 1.2 kV 4H-SiC MOSFETs with accumulation mode channel is reported in this paper. 1.2 kV SiC MOSFETs with a variety of cell designs were fabricated and compared with respect to the output and transfer characteristics, and blocking behaviors. All the design rules, such as channel length, JFET width, contact openings, gate-to-source overlap, and cell pitch were investigated to clearly provide the quantitative impact on the static performances. 2D-simulation was also conducted to support experimental results. As a result, it turned out that the channel length is the most determining factor for the specific on-resistance, resulting in 0.364 mΩ-cm^2 increase per 0.1 μm increase in the channel length. However, the channel potential is also largely dependent on the channel length such that the leakage current tends to increase with short channel design. The enhanced doping in the JFET region with a current spreading layer (CSL) is essential for achieving a narrower JFET width, which satisfies all static performances, as well as device reliability and ruggedness. Methods to further improve the trade-off characteristics using other design aspects are discussed in this paper.

INDEX TERMS Silicon Carbide, 4H-SiC, MOSFET, current spreading layer (CSL), 2D-simulation, design consideration, specific on-resistance, breakdown voltage, V_{th}, yield, FOM.

I. INTRODUCTION

Silicon Carbide (SiC) MOSFETs provide various advantages for high voltage and high frequency applications, such as power inverter and fast charter for electric vehicles, medium voltage motor drives, and commercial aviation. In most applications, the driving force for the commercialization of SiC MOSFETs is low on-resistance with superior switching performance when compared to the Silicon IGBT. Numerous research efforts have been conducted aiming to minimize the specific on-resistance ($R_{on,sp}$) for a specified breakdown voltage (BV). The process technologies that enabled the demonstration of high-performance 1.2 kV SiC MOSFETs include the post oxidation anneal in nitric oxide (NO) [1], high quality epi-growth technique [2], ion implantations at elevated temperatures [3], etc. In regards to the device architecture, many groups have been developing the trench-type MOSFET [4], [5], but the planar-type MOSFET has remained mainstream since its commercialization in the early 2010s. Many novel design approaches, as well as edge termination techniques, for SiC planar MOSFETs have been attempted to improve $R_{on,sp}$, BV, switching performance, reliability, and the trade-offs between them. Accumulation mode channel has been reported to improve $R_{on,sp}$ due to the increase of channel mobility [6]–[8]. K. Han has reported the effect of channel length for the inversion mode channel MOSFETs [9]. The optimization of JFET region [10] and current spreading layer (CSL) [11] have been suggested for the improvement of forward conduction mode. Saha and Cooper [11] and Liu *et al.* [12] have briefly reported the effect of cell pitch for $R_{on,sp}$. Although accumulation mode channel MOSFETs with CSL are known to exhibit a trade-off relationship between $R_{on,sp}$ and BV

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with respect to the channel and JFET region, detailed information and discussion on the impact of the channel and JFET design for accumulation mode channel MOSFETs with CSL is lacking in previous literatures. Moreover, the completed and specific unit cell design rules are deficient, resulting in the lack of detailed research and comprehensive understanding regarding trade-off relationship between $R_{on,sp}$ and BV within the cell structure. In particular, when reviewing the presently available literature it is difficult to fairly compare the effect of each component of the MOSFETs due to different structures and processes reported by different groups. This study is particularly important for low voltage (600 ~ 1200 V) SiC MOSFETs because the on-resistance is largely dependent on the cell design.

This paper presents a comprehensive analysis on trade-off relationship between $R_{on,sp}$ and BV (along with yield) for the 1.2 kV accumulation mode channel SiC MOSFETs with CSL and different dimensions in the cell structure. Such dimensions explored include, the channel, JFET, contact opening, ILD (inter-layer dielectric) width, and gate-to-source overlap. In order to conduct a completed experiment that produces comprehensive results for a deep understanding, while fairly comparing the effect of each component of the MOSFET, the 1.2 kV accumulation mode channel SiC MOSFET devices investigated in this paper were fabricated on the same, 6-inch wafer using the same mask set. In Section II – Device Design, design approaches for the fabricated 1.2 kV SiC MOSFETs are discussed; In Section III – Fabrication Technology, device fabrication process is explained; In Section IV – Results, electrical characteristics measured from fabricated SiC MOSFETs with the above mentioned design variations are presented; In Section V – Discussion, inclusive analyses are provided.

II. DEVICE DESIGN AND MODELING

Fig. 1 (a) and (b) show top views of layout designs for 1.2 kV SiC MOSFET cells with P+ sources located in a stripe pattern and intermittently located in the orthogonal direction, respectively. A-A' cross-sectional view for the stripe pattern P+ is shown in Fig. 1 (c). In order to reduce dead space (i.e., the area underneath the P-well that is not fully utilized for the current conduction), and thus enable a reduction in the cell pitch, the P+ source contacts are intermittently placed in the orthogonal direction, as shown in Fig. 1 (b) [7]. Fig. 1 (d) and (e) pertain to the MOSFET with orthogonal P+ sources and show the cross-sectional views of portions that include N+ source contact and P+ source contact, respectively. As shown in Fig. 2, ion implantation schedules for the JFET region and P-well are designed to create the accumulation mode channel to attain high channel mobility [7]. A current spreading layer (CSL) underneath the P-well is adopted to further reduce the resistance near the bottom of the P-well. The half-cell pitch (A-A' or B-B') consists of contact opening (W_C), ILD width (W_{ILD}), gate-source overlap (W_{G-S}), channel length (L_{ch}), and JFET width (W_{JFET}), as shown in Fig. 1 (c). Analyses of device designs (described

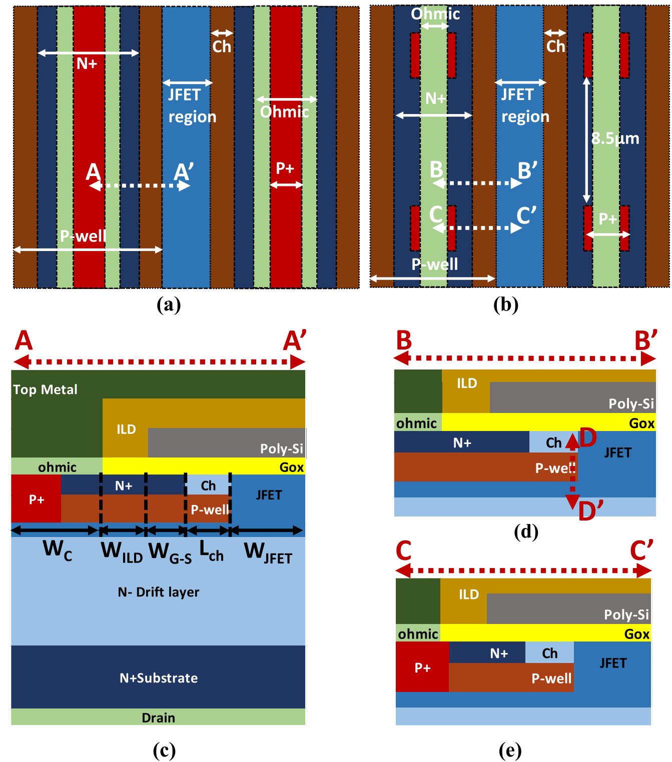


FIGURE 1. (a) A layout approach of MOSFETs with linear striped P+, (b) a layout approach of MOSFETs were placed intermittently in the orthogonal direction. (c) A-A' cross-sectional view of MOSFETs with linear striped P+, (d) B-B' cross-sectional view of N+ source contact of MOSFETs were placed intermittently in the orthogonal direction, and (e) C-C' cross-sectional view of P+ body contact of MOSFETs were placed intermittently in the orthogonal direction.

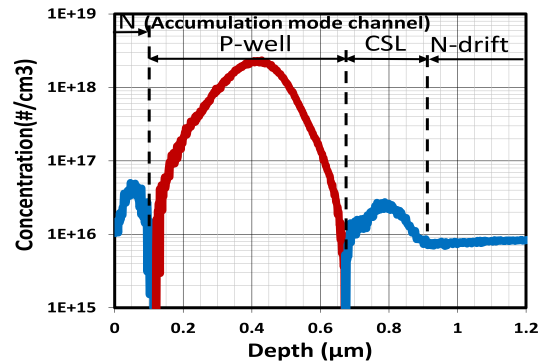


FIGURE 2. Designed implant profiles for channel region and P-well (D-D') using sPROCESS.

in Sections IV and V, with Table 1 containing detailed design parameters) were divided into 4 parts: contact opening, JFET width, channel length, and others (i.e., contact opening, ILD width, and gate-source overlap that determine the cell pitch altogether).

For fair evaluation in the blocking mode, an efficient edge termination structure is necessary to compare all the design variations mentioned above. A hybrid-junction termination extension (Hybrid-JTE) was employed to achieve a near ideal breakdown voltage [13].

Sentaurus 2D TCAD was used to support and clarify the experimental results. For the simulation of forward conduction, Lombardi model for interface trap and channel mobility degradation was applied to match experimental channel mobility and V_{th} [14]–[16]. Okuto-Crowell model was used for the avalanche model [14], [17]. The BV value was extracted when the integral of impact ionization coefficient of holes reaches unity, which implies avalanche breakdown. Simulation models for Silicon Carbide have been developed and optimized [14], [18].

III. DEVICE FABRICATION TECHNOLOGY

The devices were fabricated by Analog Devices, Inc. (ADI) fabrication facility in Hillview, San Jose, CA, using the same base process line [19], [20]. A 10 μm thick drift layer with N- type doping concentration of 8×10^{15} cm^{-3} on 6-inch, N+ 4H-SiC substrate was used for the fabrication of proposed 1.2 kV MOSFETs. Aluminum and Nitrogen ion implants were used to form P-well/P+ source/JTE, and JFET/N+ source, respectively. All implants were conducted at 500 °C. After all implantation steps, a 1650 °C, 10-min activation anneal with a carbon cap was conducted. A 50 nm thick gate oxide was formed by ultrathin (2 nm) thermal oxide and 48 nm of deposited oxide, followed by a post oxidation anneal (POA) in N_2O ambient. The N-type polysilicon was deposited and patterned for the formation of the gate. After, undoped silicon glass (USG) was deposited as interlayer dielectric (ILD), then patterned and etched to make ohmic contact regions. Nickel (Ni) was deposited on the frontside, followed by an RTA for the silicidation process. Next, unsilicided Ni metals were removed and annealed by RTA at 965 °C for 2 mins. Backside was then deposited by Ni, followed by the same RTA process. A 4 μm thick Ti/TiN/Al stack was deposited for the source and gate metal. Silicon nitride and polyimide were used for the passivation. Finally, a solderable metal stack was deposited on the backside. Fig. 3 shows the cross-sectional SEM image of the fabricated MOSFET.

IV. RESULTS

A. CONTACT OPENING (W_C)

To examine the impact of contact dimensions on the on-resistance, half contact openings (W_C) of 1.0, 0.5, 0.4, and 0.3 μm were included keeping other parameters identical (W_{ILD} = 0.6 μm, W_{G-S} = 0.5 μm, L_{ch} = 0.5 μm, W_{JFET} = 0.8 μm). Except for the structure with W_C of 1.0 μm, all other MOSFETs used the design approach shown in Fig. 1 (b) to reduce the cell pitch. Resultant cell pitches are 6.8, 5.8, 5.6, and 5.4 μm, respectively.

Fig. 4 (a) shows output characteristics of the fabricated 1.2 kV rated SiC MOSFETs with different W_C. All electrical data presented in this paper were measured from on-wafer. In our experience, after packaging, there is a 15% reduction in $R_{on,sp}$. Structures with orthogonal P+ provide larger currents than the ones with stripe pattern P+ and W_C of 1.0 μm. This difference in the on-resistances originates from the cell pitch. The role of P+ source contact is to provide a stable zero potential to the P-well under the forward conduction mode. Both structures with striped and orthogonal P+ sources successfully serve this purpose. However, the larger cell pitch in the stripe pattern MOSFET causes the increase in $R_{on,sp}$. In contrast, MOSFETs with W_C of 0.5, 0.4 and 0.3 μm show identical output characteristics regardless of the cell pitch. The smaller W_C would increase N+ contact resistance in MOSFETs. This increase of N+ contact resistance is compensated by the decrease of resistance stemming from reducing the cell pitch. Measured specific contact resistance, extracted by N+ circular type transmission line measurements (cTLMs), was $6.18\times10^{-5}\Omega$-cm^2. Depending on the contact resistance, the optimum W_C will differ; When the specific contact resistance is much lower than $6.18\times10^{-5}\Omega$-cm^2, tight W_C could reduce the on-resistance, although the degree of improvement would not be significant; The narrow W_C using ideal contact resistance which is zero provides the reduced $R_{on,sp}$ in simulation, as shown in Fig. 4 (b).

The measured transfer characteristics of the fabricated MOSFETs with varied W_C are shown in Fig. 5 (a). The threshold voltage (V_{th}) extracted at drain-source current (I_{ds})

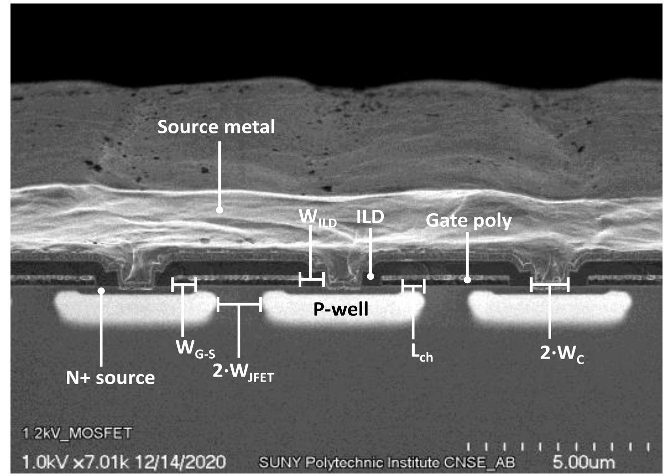


FIGURE 3. The cross-sectional SEM image of the fabricated 1.2kV 4H-SiC MOSFETs with nominal design rules (W_C = 0.5 μm, W_{ILD} = 0.6 μm, W_{G-S} = 0.5 μm, L_{ch} = 0.5 μm, W_{JFET} = 0.8 μm, Cell pitch = 5.8 μm).

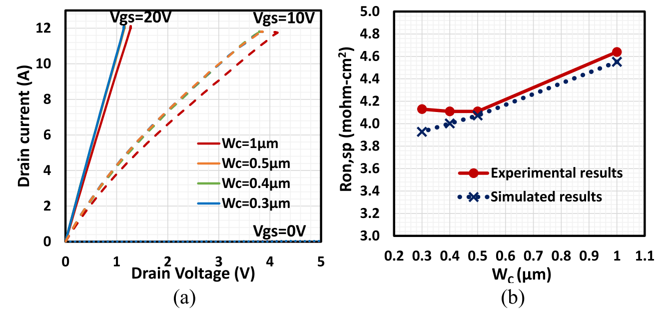


FIGURE 4. (a) Output characteristics of fabricated 1.2kV MOSFET with different W_C and (b) Summary of experimental and simulated $R_{on,sp}$. MOSFETs were measured at gate-source biases of 0 to 20 V with 10 V steps. The $R_{on,sp}$ were extracted at V_{gs} of 20 V and V_{ds} of 0.1 V.

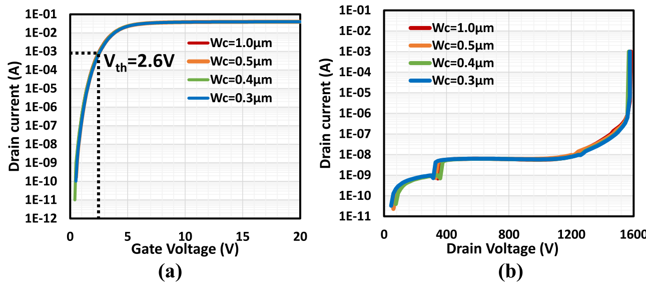


FIGURE 5. **(a) Measured transfer characteristics and (b) measured forward blocking behaviors of the fabricated MOSFETs with different W_C.**

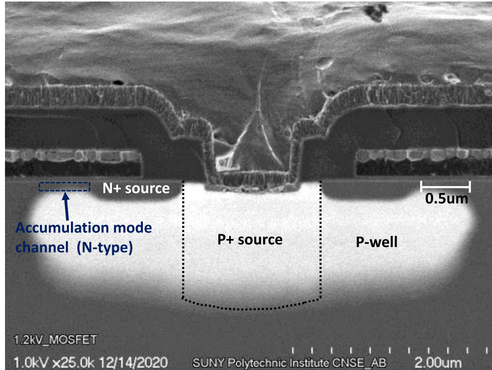


FIGURE 6. **The cross-sectional SEM image of the fabricated 1.2kV 4H-SiC MOSFETs for the device of L_{ch} of 0.5 μm.**

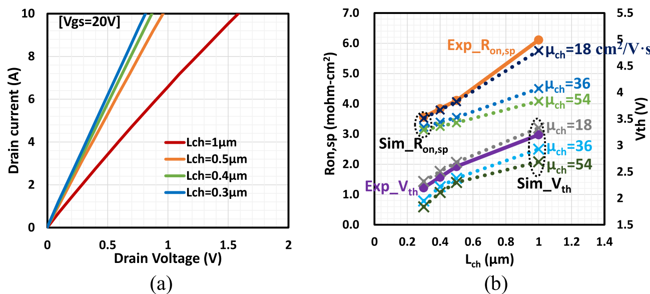


FIGURE 7. **(a) Measured output characteristics of the fabricated MOSFETs with different L_{ch} and (b) summary of experimental and simulated $R_{on,sp}$ with different channel mobilities (18, 36, 54 cm^2/V·s) and experimental V_{th}.**

of 1 mA is about 2.6 V for all structures, which also highlights that orthogonal direction P+ provides appropriate zero potential to P-well. Fig. 5 (b) shows measured forward blocking behaviors of the fabricated MOSFETs with different W_C. Regardless of the split, high breakdown voltages with low leakage currents were accomplished thanks to the efficient edge termination technique (Hybrid-JTE). As expected, W_C for N+ is unrelated to blocking behaviors. It is important to note that orthogonal P+ design also provides a high breakdown voltage with no negative outcomes, such as snapback.

B. CHANNEL LENGTH (L_{CH})

The channel length (L_{ch}) was varied to investigate the trade-offs between $R_{on,sp}$ and BV, and $R_{on,sp}$ and V_{th}. L_{ch} of 1.0,

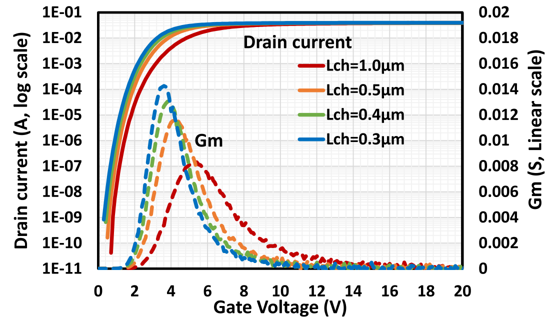


FIGURE 8. **Measured transfer characteristics at V_{ds} = 0.1V and transconductances of the fabricated MOSFETs with different L_{ch}. Vth were extracted from transfer characteristics at drain current of 1 mA. Vth, for L_{ch} of 0.3, 0.4, 0.5, and 1.0 μm, are 2.2, 2.4, 2.6, and 3.2 V, respectively.**

0.5, 0.4, and 0.3 μm were designed keeping other design rules identical (W_C = 0.5 μm, W_{ILD} = 0.6 μm, W_{G-S} = 0.5 μm, W_{JFET} = 0.8 μm and orthogonal direction P+ were used). Fig. 6 shows the cross-sectional SEM image of the accumulation mode channel MOSFET with L_{ch} = 0.5 μm (showing C-C' in Fig. 1(e)). Accumulation mode channel was formed using the controlled JFET and P-well implants, as shown in Fig. 2.

Fig. 7 (a) shows measured output characteristics of the fabricated accumulation mode channel MOSFETs with different L_{ch}. Due to a lower channel resistance, shorter channels offer higher current at the same drain-source voltage. Another important variable along with the L_{ch} is the channel mobility. In this case, the field effect channel mobility extracted from a lateral test MOSFET (FATFET) with a L_{ch} of 200 μm at V_{ds} of 0.1 V was approximately 18 cm^2/V·s, which is considered as reasonable in the current SiC technology. Summary of experimental and simulated $R_{on,sp}$ with different Simulated results with different channel mobilities show the importance of high channel mobility. As the channel mobility increases, the rate of change of $R_{on,sp}$ per increase of L_{ch} gets smaller. The measured transfer characteristics and transconductance of the fabricated MOSFETs with different L_{ch} channel mobilities and experimental V_{th} is shown in Fig. 7 (b) are shown in Fig. 8. Transfer characteristics and transconductances were measured at V_{ds} of 0.1 V. When compared with a longer L_{ch}, the transconductance of a shorter L_{ch} decreases to a value of 0 much more dramatically after reaching the maximum transconductance value. As a result, a shorter L_{ch} is preferred to minimize the channel resistance and overall device on-resistance. However, the reduction in the on-resistance brings in a detrimental issue during the forward blocking mode.

Fig. 9 shows measured forward blocking behaviors of the fabricated 1.2 kV MOSFETs with various L_{ch}; clearly showing that a shorter channel results in poor blocking behavior with large leakage current. Breakdown of MOSFETs with shorter channels (L_{ch} of 0.3 and 0.4 μm) occur due to the increase of leakage current from the channel, not as a result of the avalanche breakdown. In contrast, longer channel (L_{ch}

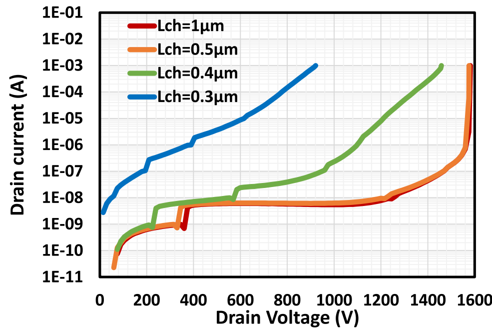


FIGURE 9. Measured forward blocking behaviors of the fabricated MOSFETs with different L_{ch}.

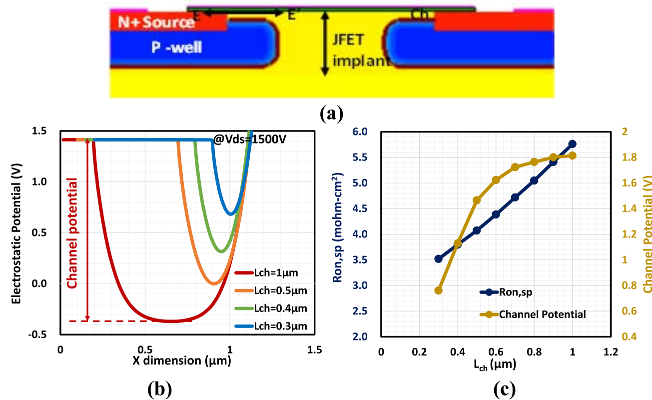
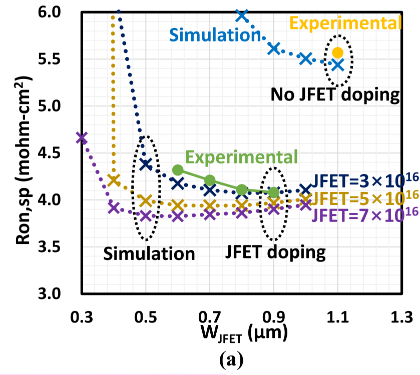


FIGURE 10. (a) Cross-sectional view of simulated 1.2kV accumulation channel mode MOSFETs (b) simulated electrostatic potential at channel region of MOSFETs with different L_{ch} at V_{ds} of 1500V, and (c) summary of simulated $R_{on,sp}$ and channel potential (V_{ds} = 1500V).

of 0.5 and 1.0 μm) shows avalanche breakdown behaviors, identified by a sudden increase in the drain-source current. In order to further explore the effect of L_{ch} on the blocking behavior, simulated electrostatic potential near the surface, starting at the N+ source, proceeding through the channel, and ending in the JFET region (E-E' shown in Fig. 10 (a)) was extracted at V_{ds} of 1500 V, as shown in Fig. 10 (b). It is demonstrated that longer L_{ch} has a larger and thicker potential barrier, thus providing lower leakage current under the high drain voltage. The large leakage current at low drain bias from the short channel structure is originated from the reduced potential barrier formed across the channel. When the L_{ch} is sufficiently long ($L_{ch} \geq 0.5$ μm), the channel potential is maintained and blocks the leakage current between source and drain until the avalanche breakdown occurs. Fig. 10 (c) summarizes the $R_{on,sp}$ and channel potential at V_{ds} of 1500 V for simulated MOSFETs with varied L_{ch}. From the comparison between this simulation and experimental results (Fig. 9), it is concluded that a channel potential larger than at least 1.4 V is essential to suppress the leakage current up to the avalanche condition, which is informative when exploring new device design concepts using 2D device simulations.



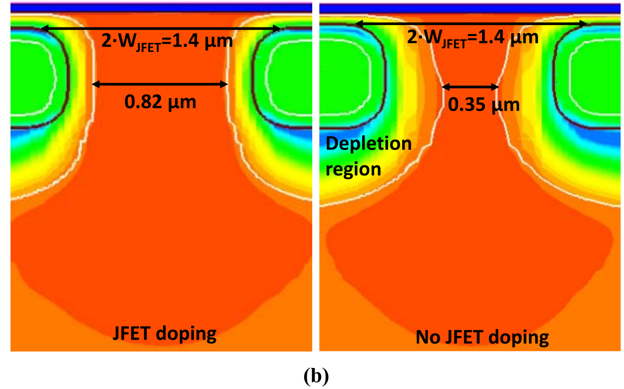


FIGURE 11. (a) Summary of measured and simulated $R_{on,sp}$ and (b) current density distribution of simulated MOSFETs with W_{JFET} of 0.7 μm (*Simulated JFET doping of 5×10^{16} and 7×10^{16} cm^{-3} has channel doping of 3×10^{16} cm^{-3} to keep same channel region).

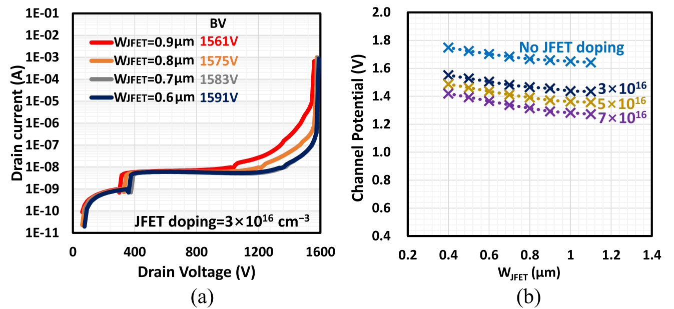


FIGURE 12. (a) Measured forward blocking behaviors and (b) simulated channel potential of MOSFETs with varied W_{JFET} (*Simulated JFET doping of 5×10^{16} and 7×10^{16} cm^{-3} has channel doping of 3×10^{16} cm^{-3} to keep same channel region).

It is particularly important to minimize the misalignment between P-well and N+ source since these two layers define the L_{ch}. With a certain misalignment, one side of the L_{ch} in the unit cell structure, as shown in Fig. 10 (a), becomes smaller than the other resulting in large leakage current. To prevent both side of the unit-cell from having a L_{ch} shorter than the designed L_{ch}, alignment tolerance should be considered, and more preferably, a well-established process scheme to implement a self-align channel is required.

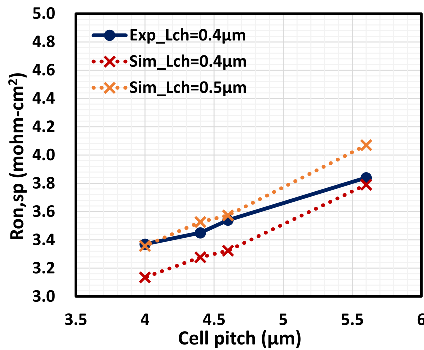


FIGURE 13. Summary of measured and simulated $R_{on,sp}$ with different cell pitch.

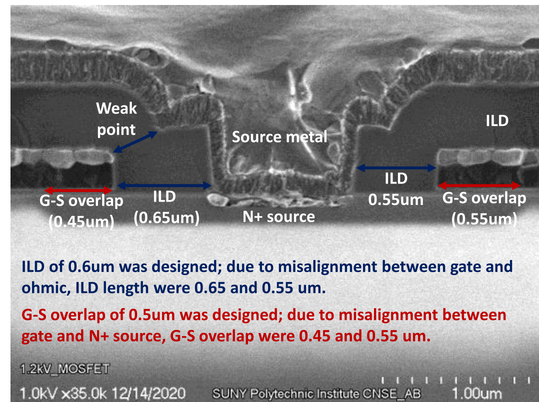


FIGURE 14. The cross-sectional SEM image of the fabricated 1.2kV 4H-SiC MOSFETs for the device of W_C of 0.5 µm.

C. JFET WIDTH (W_{JFET})

To optimize the JFET region, different W_{JFET} of 0.6, 0.7, 0.8, and 0.9 µm were included. The designed doping concentration in the JFET region is approximately 3×10^{16} cm^{-3}. The depth of the JFET junction is 0.9 µm and is 0.1 µm deeper than the P-well, which implements the current spreading layer (CSL). Enhanced doping in the JFET region with CSL allows a narrow W_{JFET}, which provides improved conduction and switching behaviors with reduced leakage current during the forward blocking mode. Fig. 11 (a) compares measurements and simulations of $R_{on,sp}$ for varied W_{JFET}. Simulation results agree well with the experimental data, regardless of the doping concentration in the JFET region. It was discovered that the enhanced doping in the JFET region allows significantly improved conduction behaviors. Fig. 11 (b) compares current density distributions of simulated MOSFETs with and without enhanced doping (3×10^{16} cm^{-3}) in the JFET regions ($W_{JFET} = 0.7$ µm). An enhanced doping offers larger effective W_{JFET} for current to flow due to smaller depletion region, enabling the use of narrower W_{JFET} in design.

Fig. 12 (a) shows measured forward blocking behaviors of MOSFETs with varied W_{JFET}. Narrower W_{JFET} provides higher breakdown voltage with lower leakage current because the channel is better shielded from the drain bias, as shown in Fig. 12 (b). Depending on the implementation of the JFET implant and doping concentration, the optimum W_{JFET} will differ to achieve the best combination of low $R_{on,sp}$ with high breakdown voltage; the trade-off relationship between $R_{on,sp}$ and BV was improved using JFET implant with CSL. Higher JFET doping is required to achieve narrower W_{JFET} and therefore obtain the desired breakdown voltage, lower electric field in the gate oxide, and improved short-circuit capability [21].

D. CELL PITCH

Different combinations of dimensions for the contact opening (W_C), ILD width (W_{ILD}), and G-S overlap (W_{G-S}) of 0.5/0.6/0.5, 0.4/0.4/0.3, 0.4/0.4/0.2, and 0.3/0.3/0.2 µm (L_{ch} = 0.4 µm and W_{JFET} = 0.8 µm) were included to examine the impact of the cell pitch on the $R_{on,sp}$. It is important to investigate the manufacturability of these structures since there are concerns regarding the gate to source leakage and misalignments between different mask layers. Fig. 13 shows the measured $R_{on,sp}$ from MOSFETs with different cell pitches. As expected, a smaller cell pitch is beneficial in reducing the $R_{on,sp}$. To suppress the leakage current and attain higher BV, simulated $R_{on,sp}$ in case of L_{ch} = 0.5 µm are also added in Fig 13. The difference between experimental and simulated results stems from the contact resistance, as mentioned in Section IV-A.

While pursuing a smaller cell pitch to reduce the $R_{on,sp}$, it is important to evaluate the yield loss due to the aggressive design rules for W_{ILD} and W_{G-S}. Too small W_{ILD} provokes shorting between gate and source, resulting in high gate leakage and low gate-source breakdown. In other words, a tight W_{ILD} has trouble with gate control. During the fabrication of SiC MOSFETs, misalignments between N+ source implant and gate poly are inevitable, as shown in Fig. 14. When the N+ source and gate poly become significantly separated due to misalignment, MOSFETs ultimately lose one side of the channel within the unit cell, resulting in high $R_{on,sp}$. Fig. 15 (a) shows half-wafer maps measured from devices with different cell pitches demonstrating yield losses due to narrow W_{ILD} and small W_{G-S}. Fig. 15 (b) summarizes the % yield losses based on the measurement shown in Fig. 15 (a). Cell pitch of 5.6 µm (W_{ILD} = 0.6 µm, W_{G-S} = 0.5 µm) have 100% operational yield. However, when reducing W_{ILD} from 0.6 µm to 0.4 µm, several operational failures occurred (i.e., 1 or 2 out of 15 have problem with gate control). When W_{ILD} becomes 0.3 µm, the gate failure rapidly increases (4 out of 15). Yet, a decreased W_{G-S} of 0.5 to 0.3 µm resulted in 100% operational yield. However, it was observed that a W_{G-S} of 0.2 µm began to cause the loss of channel due to misalignment, resulting in the increase of $R_{on,sp}$ in spite of reduced cell pitch. It was discovered that tight cell pitch caused by tight W_{ILD} and W_{G-S} increases the likelihood of operational failure. W_{ILD} of larger than 0.4 µm and W_{G-S} of larger than 0.3 µm are required to operate MOSFETs without failure and achieve low yield losses.

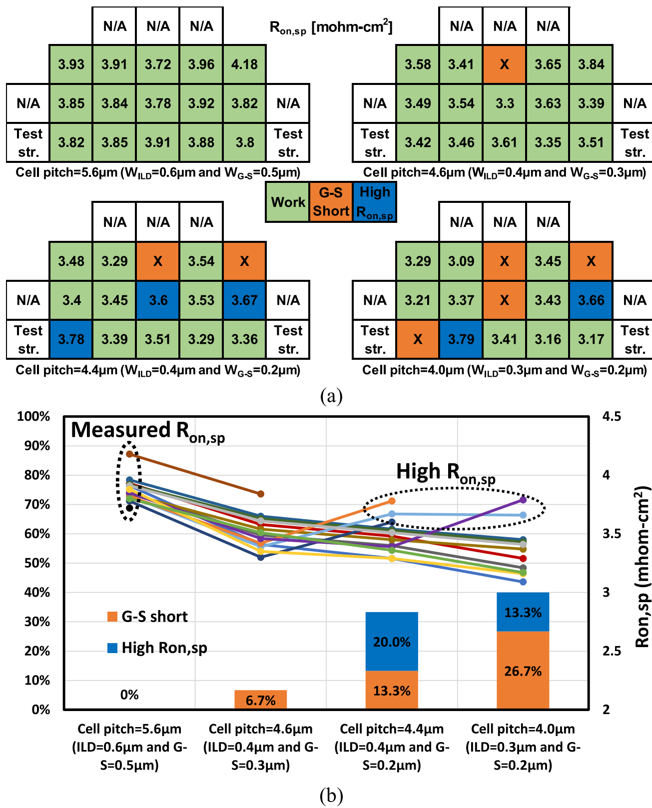


FIGURE 15. (a) Wafer-map of extracted $R_{on,sp}$ from the MOSFETs with different cell pitch and (b) the percentage of yield issue for MOSFETs and $R_{on,sp}$ with varied cell pitch (G-S short: Gate voltage was not applied, High $R_{on,sp}$: when compared with cell pitch of 4.6 μm in the same die, $R_{on,sp}$ was higher).

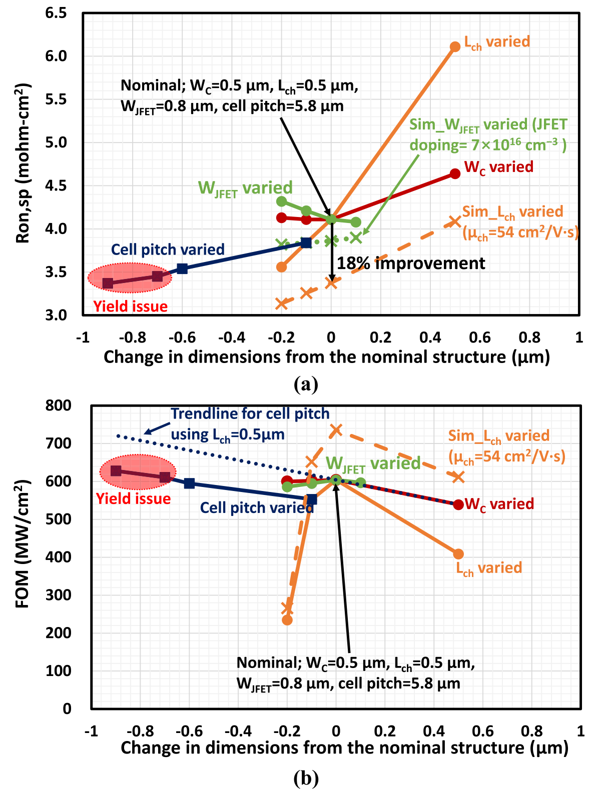


FIGURE 16. (a) Summary of $R_{on,sp}$ and (b) FOM depending on delta dimension for each parameter (*Nominal device has W_C = 0.5 μm, L_{ch} = 0.5 μm, W_{JFET} = 0.8 μm, cell pitch=5.8 μm).

V. DISCUSSION

Fig. 16 (a) summarizes $R_{on,sp}$ as a function of different dimensions in the MOSFET cell structure. Although improving the channel resistance has been the main focus of the SiC industry, the channel mobility for a planar-type MOSFET remains in the range of 15 – 30 cm^2/Vs. As a result, the channel resistance still contributes to the largest portion of $R_{on,sp}$ of 1.2 kV SiC planar MOSFET. With the aid of higher channel mobility, a three times higher channel mobility as an example, 18 % improvement in the $R_{on,sp}$ can be additionally achieved, as shown by the dashed line in Fig. 16 (a). In contrast, a small change of $R_{on,sp}$ between W_{JFET} was achieved, even for a W_{JFET} of 0.6 μm. However, W_{JFET} smaller than 0.6 μm with the same doping concentration would dramatically increase the $R_{on,sp}$. Therefore, a further enhanced doping concentration in the JFET region can be considered to accomplish a narrower W_{JFET} and further reduce $R_{on,sp}$ (see the dotted line). It is also important to note that reduced cell pitch associated with orthogonal P+ and tight W_{ILD} and W_{G-S} is proven to be effective in reducing $R_{on,sp}$ without negatively impacting the blocking behavior, at the price of serious device yield issues.

Figure-of-Merits (FOM, $BV^2/R_{on,sp}$) [22] are shown in Fig. 16 (b) to compare static characteristics for each component. FOM exhibits strong sensitivity to L_{ch} due to low channel mobility; shorter channel has lower BV and longer channel provides higher $R_{on,sp}$. The improved channel mobility is an effective way to further increase FOM as shown in the dashed line. For W_{JFET} variations, FOM is relatively similar due to enhanced JFET implant with CSL. Depending on W_C for N+, FOM is almost identical. In contrast, the change of W_c of 1 μm to 0.5 μm increases FOM because of the use of orthogonal P+ causing reduced cell pitch (W_C for N+ is the same). The decreased cell pitch caused by reduced W_{ILD} and W_{G-S} also increases FOM. However, when considering yield issue, cell pitch of 4.6 μm is seen as the optimum value. Trendline for cell pitch for an L_{ch} of 0.5 μm exhibits the improvement of static characteristics when compared with an L_{ch} of 0.4 μm due to the high BV. In general, it was demonstrated that device performance is significantly affected by cell design when considering all aspects. Table 1 summarizes all experimental results and design information. It was discovered that L_{ch} is the most critical factor for the $R_{on,sp}$, resulting in 0.364 mΩ-cm^2 increase per 0.1 μm increase in L_{ch} ($\Delta R_{on,sp}/\Delta$dimension). Reducing the cell pitch by putting the p+ source in the orthogonal direction results in a greater influence on the $R_{on,sp}$ change than by controlling W_{ILD} and/or W_{G-S}. The optimization of the JFET region parameters is also very important but would produce an opposite trend when doping is further enhanced. Combined effort to improve the

TABLE 1. Summary of experimental results and design information.

Device Structure	Experimental results					Design information							
	Ron,sp [mΩ-cm²]	Vth [V]	BV [V]	FOM [MW/cm²]	ΔRon,sp / Δdimension [mΩ-cm²]	W_C for P+	W_C for N+	W_{ILD}	$W_{G\text{-}S}$	L_{ch}	W_{JFET}	Cell pitch
W_C=1.0 µm	4.64	2.6	1581	539	0.106	0.5	0.5	0.6	0.5	0.5	0.8	6.8
W_C=0.5 µm	4.11	2.6	1575	604		0.0	0.5	0.6	0.5	0.5	0.8	5.8
W_C=0.4 µm	4.11	2.6	1573	602	~0	0.0	0.4	0.6	0.5	0.5	0.8	5.6
W_C=0.3 µm	4.13	2.6	1574	600		0.0	0.3	0.6	0.5	0.5	0.8	5.4
L_{ch}=1.0 µm	6.11	3.2	1581	409	0.364	0.0	0.5	0.6	0.5	1.0	0.8	6.8
L_{ch}=0.5 µm	4.11	2.6	1575	604		0.0	0.5	0.6	0.5	0.5	0.8	5.8
L_{ch}=0.4 µm	3.84	2.4	1457	553		0.0	0.5	0.6	0.5	0.4	0.8	5.6
L_{ch}=0.3 µm	3.56	2.2	914	235		0.0	0.5	0.6	0.5	0.3	0.8	5.4
W_{JFET}=0.9 µm	4.08	2.6	1561	597	0.080	0.0	0.5	0.6	0.5	0.5	0.9	6.0
W_{JFET}=0.8 µm	4.11	2.6	1575	604		0.0	0.5	0.6	0.5	0.5	0.8	5.8
W_{JFET}=0.7 µm	4.21	2.6	1583	595		0.0	0.5	0.6	0.5	0.5	0.7	5.6
W_{JFET}=0.6 µm	4.32	2.6	1591	586		0.0	0.5	0.6	0.5	0.5	0.6	5.4
Cell pitch=5.6 µm	3.84	2.4	1457	553	0.078	0.0	0.5	0.6	0.5	0.4	0.8	5.6
Cell pitch=4.6 µm	3.54	2.4	1451	595		0.0	0.4	0.4	0.3	0.4	0.8	4.6
Cell pitch=4.4 µm	3.45	2.4	1452	611		0.0	0.4	0.4	0.2	0.4	0.8	4.4
Cell pitch=4.0 µm	3.37	2.4	1455	628		0.0	0.3	0.3	0.2	0.4	0.8	4.0

channel mobility and enhanced doping in the JFET region will benefit all aspects of SiC MOSFETs.

VI. CONCLUSION

The fabricated 1.2 kV 4H-SiC MOSFETs with accumulation mode channel are closely investigated in terms of all aspects of design (W_C, W_{ILD}, W_{G-S}, L_{ch}, and W_{JFET},) on static characteristics, such as output and transfer characteristics, and blocking behaviors. Moreover, 2D-simulation was implemented to elucidate the effect of cell design from experimental results and suggest a direction to be further improved. It is demonstrated that L_{ch} is the most critical factor in 1.2 kV 4H-SiC MOSFETs due to low channel mobility; 3 times channel mobility can improve $R_{on,sp}$ of 18% with no negative effect on BV. The enhanced JFET doping with CSL allows lower $R_{on,sp}$, and narrow W_{JFET}, providing better blocking and reliability; to further improve the device performance and reliability, the increased JFET doping with narrower W_{JFET} is preferable. Different W_c exhibits identical static characteristics in low contact resistance; when contact resistance is near ideal, narrower W_c provides better conduction behaviors due to tight cell pitch. Lastly, the reduced cell pitch from tight W_C, W_{ILD}, and W_{G-S} reduces $R_{on,sp}$ without negatively affecting blocking behaviors, but too tight W_{ILD} and W_{G-S} trigger operational failures. Overall, a detailed structural analysis of 1.2 kV 4H-SiC MOSFETs with accumulation mode channel enables further device performance improvements to be proposed.

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