Received 14 July 2021; revised 12 August 2021; accepted 17 August 2021. Date of publication 1 September 2021;
date of current version 13 December 2021. The review of this article was arranged by Editor Q. Shao.

Digital Object Identifier 10.1109/JEDS.2021.3108523

Analog Resistive Switching in BEOL, Ferroelectric Synaptic Weights

L. BÉGON-LOURS [1] (Member, IEEE), M. HALTER [1,2], Y. POPOFF [1,2], Z. YU [1,2], D. F. FALCONE [1,3], D. DÁVILA [1], V. BRAGAGLIA [1], A. LA PORTA [1], D. JUBIN [1], J. FOMPEYRINE [1,4], AND B. J. OFFREIN [1] (Senior Member, IEEE)

1 Science & Technology, IBM Research, 8803 Rüschlikon, Switzerland
2 Information Technology and Electrical Engineering, ETH Zürich, 8092 Zürich, Switzerland
3 Department of Applied Science and Technology, Politecnico di Torino, 10129 Torino, Italy
4 Lumiphase AG, 8802 Zürich, Switzerland

CORRESPONDING AUTHOR: L. BÉGON-LOURS (e-mail: lbe@zurich.ibm.com)

This work was supported in part by H2020 "FREEMIND" under Grant 840903; in part by "ULPEC" under Grant 732642; and in part by "BeFerroSynaptic" under Grant 871737. Part of this work was presented at IEEE EDTM (2021), see [34], as well as IEEE IMW (2021), see [35].

ABSTRACT A Ferroelectric, two-terminals, analog memristive device is fabricated with a Back-End-Of-Line, CMOS compatible process. A bilayer composed of a ferroelectric material, $HfZrO_4$ (HZO) and a semiconducting oxide, WO_x layer is comprised between two TiN electrodes. The devices demonstrate reversible and remanent resistive switching, with a record endurance ($>10^{10}$ switching cycles) and ON/OFF ratio up to 10. The analog resistive switching is obtained, with a cycle-to-cycle reproducibility of 90%. The synaptic behavior is explored with pulses of varying sign, length, or amplitude. For the scheme with constant pulse width the linearity coefficients for the potentiation and depression are -1.4 and 4. The dynamics of the resistive switching is shown to be governed by the ferroelectric domains switching. Finally, temperature dependent transport measurements indicate Ohmic conduction at low bias and Modified Schottky Emission at larger bias. They provide insights on the role of defects and oxygen vacancies in the transport and resistive switching mechanisms.

INDEX TERMS Ferroelectric devices, memristors, synapse, analog resistor.

I. INTRODUCTION

Analog memristive devices receive increasing interest for analog [1], in-memory [2], [3] as well as neuromorphic [4], [5] computing. In particular deep-neural network accelerators rely on the hardware implementation of the Vector-Matrix-Multiplication [6], for which device requirements are: analog resistive switching and good retention (memory) under operating voltage, time and temperature stress. Supervised [7] (e.g., back-propagation [8]) or unsupervised [9], [10] (e.g., spike-timing dependent plasticity) learning rules for bio-inspired computing further requires synaptic behavior: the ability to gradually increase (potentiation) or decrease (depression) the conductance upon positive or negative voltage pulses. In field-driven devices such as ferroelectric memristors, the positive and negative voltage pulses of varying amplitude emulate pre-synaptic and post-synaptic spikes in unsupervised learning experiments [11], [12]. Ferroelectric, analog memristors can be fabricated with CMOS compatible materials in a three-terminals, ferroelectric field-effect geometry, where the resistance of a channel is tuned by electrostatic modulation of the carrier density [13], [14]. Two-terminals memristive devices consist of a ferroelectric thin-film separating two asymmetric electrodes. Upon (partial) switching of the ferroelectric domains, the screening of the ferroelectric polarization, the energy profile and thus the transport properties across the stack is modified. Several mechanisms leading to the resistive switching effect were observed first using epitaxial, perovskite thin films: for example, polarization reversal can lead to a change in the effective barrier thickness of direct tunnel junctions [15]. In Schottky barriers, it can lead to a change in the height [16], or the thickness [17] of the later. In defect-rich ferroelectric layers, it can modify the electrode to trap distance [18], [19]. These effects can coexist. The resistive switching effect was also obtained using CMOS-compatible

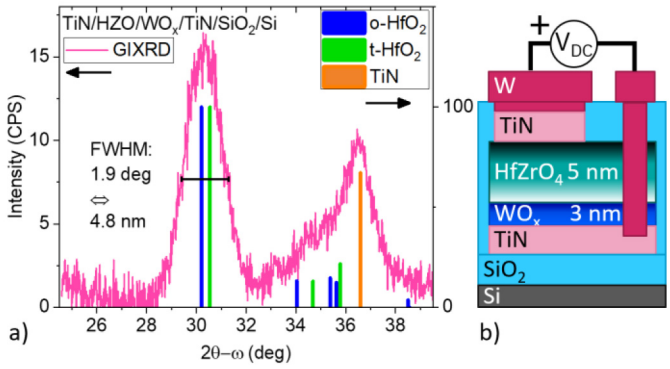

FIGURE 1. a) GIXRD scan showing HZO crystallization in a non-monoclinic phase. b) Scheme of the cross-section of the device.

materials: the metastable, ferroelectric phase of hafnia [20]. In the work of Max *et al.* [12] or Berdan *et al.* [3], a 10 nm thick HfO_2 layer is combined with an oxide interlayer acting as the tunnel barrier. The device operates under a read voltage as high as 2 V to allow transport across the HfO_2 layer, and large "On/Off" ratios (ratio between the conductance in the low and high resistive states) are obtained. However, the current voltage characteristics in this transport regime is strongly non-linear, which requires logarithmic amplifiers [3] for Vector-Matrix-Multiplication, where the analog implementation of this operation corresponds to a parallel voltage drop of varying voltages pulses through a crossbar array of linear memristors. Moreover, charge trapping in the dielectric interlayer typically leads to a moderate endurance and retention [21]. To overcome this limitation, the use of a 5 nm thick $HfZrO_4$ (HZO) layer in combination with a TiO_x semiconducting oxide interlayer was proposed [22], resulting in write voltage below 5 V and read voltage of only 0.1 V, around which the current-voltage characteristics are quasi linear. In this work, a WO_x semiconducting oxide layer is used: the On/Off is increased by a factor 5, and remarkably the devices do not show any wake-up effect. Analog resistive switching as well as synaptic potentiation/depression is demonstrated. The process is compatible with the Back-End-Of-Line, with a thermal budget not exceeding 400°C, showing high potential for co-integration with CMOS neurons.

II. BACK-END-OF-LINE FABRICATION

An asymmetric Metal Metal (M) / Ferroelectric (FE) / Semiconductor (SC) / Metal (M) (Fig. 1) layer stack was deposited on a Silicon wafer coated by a 200 nm thick thermal oxide, by Atomic Layer Deposition. The semiconducting layer is WO_{3-x}, a metal oxide with n-type semi-conducting properties due to the presence of oxygen vacancies [23]. The ferroelectric layer is $HfZrO_4$ (HZO), the bottom and top metallic electrodes are TiN, to favor the crystallization of HZO in the ferroelectric phase [20] by a ms-flash lamp annealing (ms-FLA) technique [24]: the sample is heated to a moderate temperature of 375°C, then a 20 ms long flash of 70 J/cm^2 in energy is applied to the surface. The I_d-V_g characteristics of P- and N-MOS (130 nm) test transistors were not affected by such treatment. W is then sputtered on-top. Capacitors are subsequently defined by optical lithography and reactive ion etching of the top electrode (W/TiN). The passivation layer (100 nm of SiO_2 deposited by Plasma-Enhanced Chemical Vapor Deposition at 300°C) is opened by reactive ion etching, then the HZO layer by ion beam etching. A 100 nm W layer is then sputtered and patterned to define the contacts, as sketched in Fig. 1 b). Here, we demonstrate the fabrication of HZO, ferroelectric, analog non-volatile memories at a thermal budget of ∼375°C.

X-Ray Diffraction (Fig. 1 a)) confirms the crystallization in the orthorhombic (o-) or tetragonal (t-) phase of HZO, the absence of monoclinic phase and the polycrystalline nature of the films. The Full-Width at Half-Maximum of HZO's main diffraction peak, using a Scherrer fit with k=0.9, indicates a crystallite size of 4.8 nm. X-Ray Reflectivity (see [35]) indicates sharp interfaces and a thickness of 4.8 nm for the HZO layer. Junctions do not require wake-up and Dynamic Hysteresis Measurement (DHM, see [35]) on a 120 μm diameter junction shows that no breakdown is observed after 10^{10} switching cycles with triangular pulses of +/−2V.

III. A FERROELECTRIC MEMRISTOR

In this section the resistive memory characteristics of the junction are described. First, a pulse of amplitude V_{write} and duration t_{width} is applied across the junction to align the ferroelectric domains with the applied field. The polarization screening in the M and SC layers, but also within the HZO layer itself, is asymmetric, thus the energy profile as well as the conductance of the junction is modified. Subsequently, an I(V) sweep in the range +/−300 mV measures the resistance. In this section, we address both the programmability of the device for inference and its response under pulses of varying sign, amplitude and width, emulating the combination of pre-synaptic pulses (negative bias) and post-synaptic pulses (positive bias), described for example in [25] or [12].

A. DC CHARACTERIZATION

At low bias (<300 mV) the device characteristics are moderately nonlinear with voltage, as seen in Fig. 2. The non-linearity I(V=100 mV) / I(V=50 mV) is 2.3, which is slightly improved compared to the TiO_x based junctions [22], for which the same figure was 2.4. The ON/OFF, defined as the ratio of the currents measured in the Low Resistive State, LRS (after applying −1.6 V) and the High Resistive State, HRS (after applying +2.4 V) is >10 for V_{read} = 100 mV. The ON/OFF is maximal at low bias, which is discussed in the light of the conduction mechanisms in Section IV-C.

The LRS, HRS and intermediate states can be reversibly reached and in a remanent way, as shown in Fig. 3. In this work, the metal oxide electrode plays a role in the stabilization of the HRS and allows a large memory window of 1.4 V, as discussed in Section IV-B.

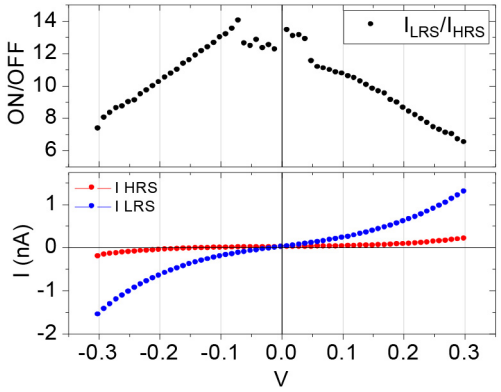

FIGURE 2. Non-switching I-V sweeps (bottom), measuring the resistance at low bias in the high (red) and low (blue) resistive state. The curves are slightly non-linear, resulting in an On/Off ratio (top) varying between 7 and 14.

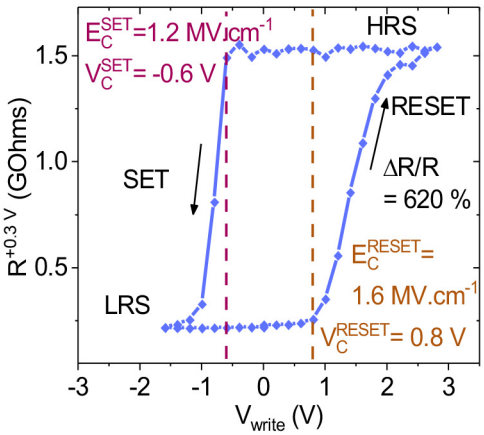

FIGURE 3. Read resistance measured at 0.3 V after DC bias V_{write}. The SC electrode is grounded. The arrows indicate the chronological occurrence. V_C and E_C are the coercive voltages and fields.

B. PULSE CHARACTERIZATION

B.1. POTENTIATION/DEPRESSION WITH CONSTANT PULSE WIDTH

Weight update potentiation (depression) is then demonstrated by sending sequences of negative (positive) pulses of 50 µs and increasing amplitude (Fig. 4), showing good repeatability: during the RESET, the resistance measured after a given V_{ampl} falls within 90% of the maximal value observed during the various cycles.

B.2. POTENTIATION/DEPRESSION WITH CONSTANT FIELD

The memristors also demonstrate constant field weight update, by increasing the pulse duration (Fig. 5). Similarly to previous work with a three-terminals structure [13] the ON/OFF is only slightly reduced compared to the scheme with constant pulse width and increasing amplitude.

In Fig. 6 the normalized conductance is fitted by a soft-bound synaptic behavior $\sigma_0(1–e^{-Count/A})$ function where A is the fit parameter [26]. The function does not provide an accurate model for the potentiation and depression, however it provides a figure of merit for quantifying its linearity. Interestingly, linearity is opposite for both schemes (sharp depression at constant V_{ampl} vs sharp potentiation at constant t_{width}) showing that symmetry can be tuned using a hybrid scheme by increasing both pulse width and amplitude.

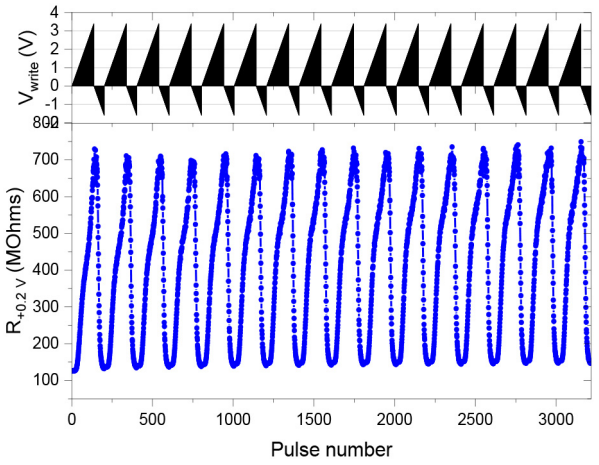

FIGURE 4. Read resistance $R^{+0.2V}$ after potentiation/depression pulses of constant duration (50 us) and increasing amplitude. n-SC is grounded.

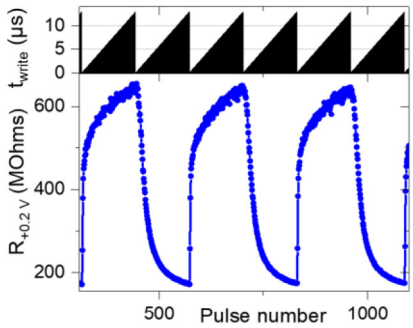

FIGURE 5. Read resistance $R^{+0.2V}$ after potentiation/depression pulses of constant field V_{write} = 3.2 V (−1.4V) and increasing duration t_{write}.

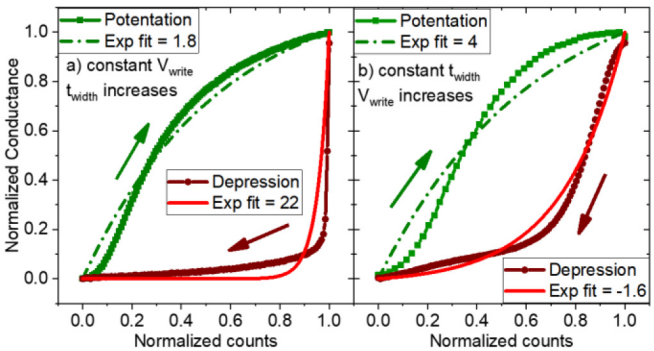

FIGURE 6. Normalized conductance vs counts (pulse number). Exp. fit parameters is measured as in [26]. a) for constant field, b) for constant pulse duration.

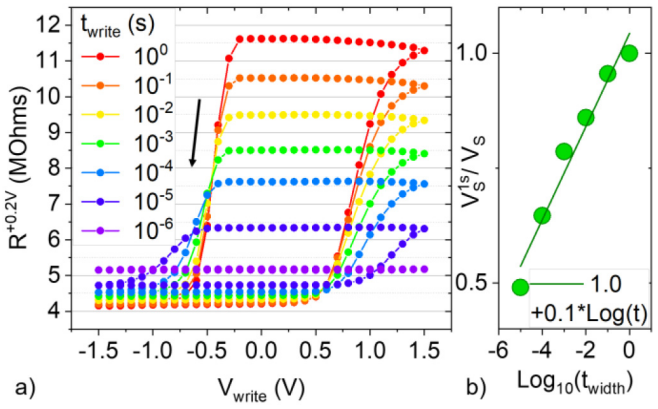

FIGURE 7. a) Resistance of a device, measured at 0.2 V, after pulses of constant duration t_{write} (see legend, 1 μs to 1 s) and increasing amplitude V_{write}. The arrow indicates the chronological occurrence. b) Normalized coercive voltage for the positive bias (green circles) and a linear regression.

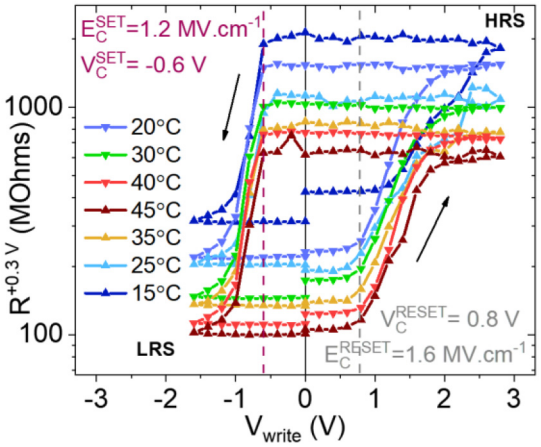

FIGURE 8. Read resistance $R^{+0.3V}$ after DC writing V_{write}. Very stable HRS ($V_C^{SET} = -0.6V$) despite screening with depleted SC. R(V_{write}) loops at increasing and decreasing temperatures, the chronological order being indicated by the order of the legend. n-SC layer is grounded.

C. POTENTIAL INTEGRATION IN A CROSS-BAR ARRAY FOR INFERENCE

On top of the low-thermal budget fabrication, the devices show a room-temperature retention larger than 10 days and are stable against heating at 45°C (Fig. 8). They show a small device to device variation ($\sigma = 0.1$ in the HRS) and scalability: current density (J) characteristics overlap for capacitors of various sizes (see [35]). Thanks to the high resistance, the energy of the pulse during writing is < 1 pJ. For V>0.5, the non-linearity of the current-voltage characteristics is high: I(V)/I(V/2)>40. This allows built-in self-selection (limited sneak paths in absence of selectors) in a writing scheme where $V_{write}/2$ is applied to unselected rows [27]. The resistivity of the devices is relatively high and extrapolation to sub-micrometric, individual devices leads to read currents <pA for read voltages of 0.2 V. Consequently, in cross-bar arrays, parallel read-out of a large number of bitlines is required to reach measurable current at the wordline.

IV. DISCUSSION

In order to provide guidelines for the optimization of the ferroelectric memristors for crossbar array fabrication, the physical mechanisms controlling the memory (in particular the stability of the HRS), the conductance and the non-linearity (conduction mechanisms) are explored.

A. SWITCHING DYNAMICS

As observed in Fig. 4 and Fig. 5, the analog resistive switching is obtained by changing the pulse amplitude or the pulse duration. To describe this dual dependance, work cycles at a given amplitude of $+/-1.5$ V are performed with various pulse widths in the range 10^{-6} – 10^{0} s, as shown in Fig. 7. The resistance in the low (resp. high) resistive state decreases moderately (resp. increases strongly) with pulse width, indicating that the saturation of the polarization in the high resistive state requires larger bias as the pulses are shorter in time. In the low resistive state, the saturation is reached below -1.5 V for pulse duration higher than 10^{-4} s. The coercive field (field at which domains start to switch) for both polarities decreases linearly with the exponent of the pulse width. This phenomenological behavior is described by Merz's law [28], and shows that the device dynamics are governed by ferroelectric switching and not by capacitive phenomena.

B. ROLE OF THE METAL OXIDE ELECTRODE

The stability of the polarization in the HRS and the dependence of the resistive switching on the pulse duration are discussed in terms of oxygen exchange between the ferroelectric and the metal oxide layer. Changing the metal oxide thickness while keeping HZO thickness constant has minor effect on the HRS and LRS (the change is less than 5%), showing that the resistance is dominated by the HZO layer and indicating that the resistive switching is mainly due to ferroelectric switching (not shown). However, the dependence of the resistive switching on the pulse duration (Fig. 5) indicates that other than purely ferroelectric effects play a role in the switching mechanism. We anticipate a resistance change through field driven migration of oxygen from the SC to the FE layer, allowing defects and oxygen vacancies in the HZO layer to self-screen the polarization. This is supported by the observation of a strongly reduced ON/OFF when using TiO_2 as SC [22] (allowing little oxygen exchange).

C. CONDUCTION MECHANISMS

The devices are tested under temperature cycling, by increasing steps first (20, 30, 40 and 45 °C) followed by decreasing steps (35, 25 and 15 °C) as shown in Fig. 8. The ON/OFF is not affected by the temperature, but the resistance in both states decreases upon heating and reversibly increases upon cooling. Such dependence and simulations discard direct tunneling as being the dominant mechanism in these junctions.

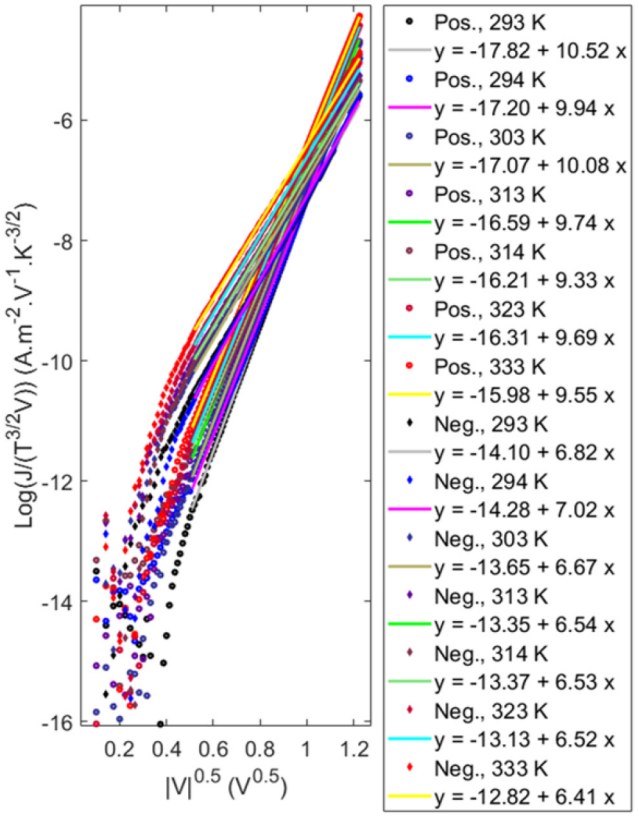

FIGURE 9. Non-switching, positive (High Resistive State, HRS, circles) and negative (Low Resistive State, LRS, diamonds) characteristics in the Modified Schottky Emission (MSE) representation after subtracting the Ohmic contribution. The bottom electrode (WO_x interlayer) is grounded. At each temperature a linear regression is perform (solid line).

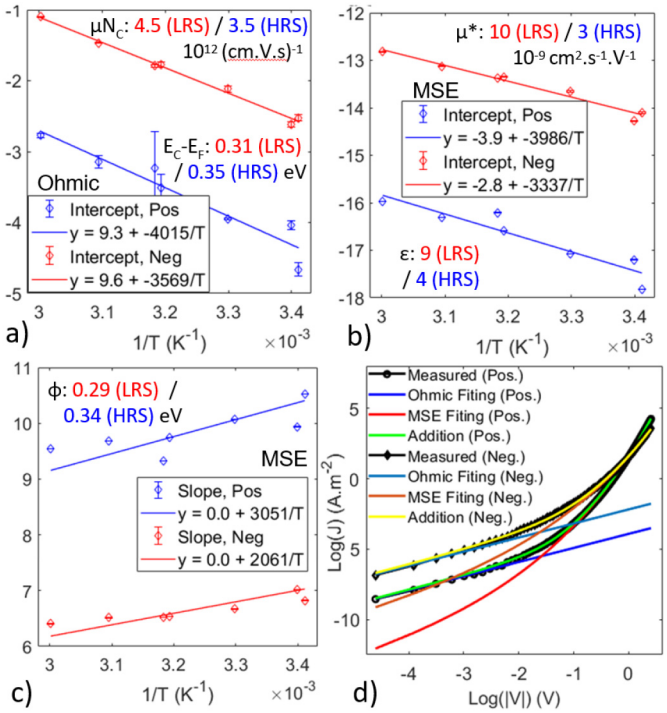

FIGURE 10. a) From the Arrhenius plot of the intercepts for the Ohmic regime the product of the mobility and the carrier density μN_C and the difference in energy between the conduction band and the Fermi level (E_C-E_F) are obtained for the LRS and the HRS. From the Arrhenius plot of the intercepts for the MSE regime (b) the effective mobility $\mu^* = \mu^*(m^*/m_0)^{3/2}$ (m^* is the effective mass) and the dielectric constant ε are obtained for the LRS and the HRS. From the Arrhenius plot of the slopes for the MSE regime (c) the barrier height φ is obtained for the LRS and the HRS. d) the experimental data is well described by a multi-branch fitting consisting of the Ohmic and MSE mechanisms.

A multibranch fitting of the J-V characteristics at various temperature is performed. At low bias (0–100 mV), the characteristics are linear. This regime is well described by the Ohmic conduction [29]:

$$J = \sigma E = \mu q N_C exp\left[\frac{-(E_C - E_F}{kT}\right]E \qquad (1)$$

with J the current density, σ the electrical conductivity, μ the electron mobility, q is the electronic charge, N_C the carrier concentration at equilibrium, E_C - E_F the energy difference between the conduction band and the Fermi level, k the Boltzmann constant, T the absolute temperature and E the electric field across the ferroelectric layer.

At each temperature, a linear regression in the log(J)=log(V) representation is performed. The intercept is plotted as a function of 1/T in Fig. 10 a), in the low and high resistive state. From this graph, a second linear regression is performed. According to equation (1) and assuming that the product μN_C is constant with the temperature [30], the latter can be estimated to $4.5 \cdot 10^{12}$ $(\text{cm.V.s})^{-1}$ in the LRS. Consistently with a higher resistance, it reduces to $3.5 \cdot 10^{12}$ $(\text{cm.V.s})^{-1}$ in the HRS. In addition, the energy E_C - E_F increases from 0.31 eV in the LRS to 0.35 eV in the HRS.

Above ∼200 mV, additional transport takes place, also thermally activated. In Fig. 9 Log(J/($T^{3/2}$V)) is represented as a function of $|V|^{0.5}$, after subtracting the current density carried by Ohmic transport (multi-branch fitting): in this representation the characteristics are linear. They correspond to the Modified Schottky Emission regime (MSE) [31], governed by the equation:

$$J = \alpha T^{\frac{3}{2}} E \mu \left(\frac{m^*}{m_0}\right)^{\frac{3}{2}} exp\left[\frac{-q\left(\phi_B - \sqrt{qE/4\pi\varepsilon_r\varepsilon_0}\right)}{kT}\right] \qquad (2)$$

where $\alpha = 3 \times 10^{-4}$ A·s/cm^3 · K$^{3/2}$ is a constant, m_0 is the free electron mass, m^* is the effective electron mass in HZO, $q\phi_B$ is the Schottky barrier height, ε_0 is the permittivity in vacuum, and ε_r is the dynamic dielectric constant.

Again, linear regressions are performed in the MSE plot at each temperature. From equation (2), we see that the product $\mu^* = \mu(m^*/m_0)^{3/2}$ and the dynamic dielectric constant ε_r can be measured from the Arrhenius plot of the intercepts (Fig. 10 b)), and the barrier height $q\phi_B$ can be measured from the Arrhenius plot of the slopes (Fig. 10 c)). The dynamic dielectric constant varies from 9 in the LRS to 4 in the HRS, which can be linked to the change in electrostatic screening of the polarization charges withing the HZO itself (space

TABLE 1. Benchmark.

Device type	MO-ECRAM [31]	TaOx/HfOx [32]	PCMO [33]	AlOx/HfO2 [34]	c-FSJ [35]	This work
Non-linearity	<1	0.04/-0.63	3.7/-6.8	1.94/-0.61	4.2/-4.2	1.9/-4.3
RON	67KΩ	100KΩ	23MΩ	16.9KΩ	100KΩ	100MΩ
ON/OFF	20	10	6.84	4.43	21	7
Depression	4V/ 10ns	1.6V/ 50ns	2V/ 1ms	0.9V/ 100µs	2V/ 80ns	2.4V/ 50 us
Potentiation	-4V/ 10ns	-1.6V/ 50ns	-2V/ 1ms	-1V/ 100µs	-2V/ 80ns	-1.6V/ 50us
Cycle-to-cycle var.	<10%	3.70%	<1%	5%	<0.5%	10%
Area (μm^2)	40	8663.1	6292.3	21,846	184,420	14,400

charge regions). The Schottky barrier heights (0.29 eV in the LRS and 0.34 eV in the HRS) are very close to the values measured in the Ohmic regime. It is small compared to the band gap of HZO (>5.4 eV for insulating films [32]), and compares to activation energies measured for the recombination of oxygen vacancies in HfO_2 [33]. It implies that the oxygen vacancies in HZO confer semiconducting properties to this ferroelectric layer. The oxygen content in HZO is controlled by the growth and annealing conditions and is an additional knob (with the thickness) to tune the conductance of the junctions. Finally, in Fig. 10 d) the multi-branch fitting for a temperature of 25°C is represented. The circles (resp. diamonds) are the experimental data for the non-switching, positive bias (LRS). in light (resp. dark) blue is the current density corresponding to the Ohmic regime, calculated using the parameters obtained from Fig. 10 a). The orange (resp. red) line corresponds to the current density in the MSE regime, calculated using equation (2) and the parameters obtained from Fig. 10 b) and c). The sum of the current density in the Ohmic and MSE regime (yellow, resp. green line) describes perfectly the experimental curve (Fig. 10 d). In Figure 2, it was observed that the ON/OFF decreases with the voltage, which can be explains as follows: upon polarization reversal, defects in the HZO layer are rearranged to self-screen the polarization charges, which results in a modulation of the Ohmic conduction withing HZO. Screening also occurs in the WO_x layer, however the device's LRS corresponds to the situation where WO_x is depleted in electrons, showing that the resistive switching originated from the HZO and not from the metal oxide interlayer. The barrier height is only moderately modified upon polarization reversal, which results in a moderate modulation of the conduction in the Modified Schottky Emission regime, as the bias increases.

V. CONCLUSION

The ferroelectric analog non-volatile memory technology presented in this works shows characteristics comparable to other technologies (Table 1).

The low thermal budget process makes it a promising candidate for the fabrication of crossbar arrays for deep-neural networks accelerators. The devices show analog potentiation/depression with constant field or constant pulse width schemes. This first generation of BEOL, ferroelectric 2-terminals memristors shows non-linearity of (1.9/-4), ON/OFF ratio up to 10 and cycle to cycle and device to device variation <10%. From temperature dependent experiments, it was determined that the presence of oxygen vacancies in the HZO layer play a crucial role in the transport properties and the resistive switching across the device, providing guidelines for future device development.

ACKNOWLEDGMENT

The authors acknowledge the Binnig and Rohrer Nanotechnology Center (BRNC).

REFERENCES

[1] Z. Sun, G. Pedretti, A. Bricalli, and D. Ielmini, "One-step regression and classification with cross-point resistive memory arrays," *Sci. Adv.*, vol. 6, no. 5, p. eaay2378, Jan. 2020, doi: 10.1126/sciadv.aay2378.

[2] R. Yang, "In-memory computing with ferroelectrics," *Nat. Electron.*, vol. 3, no. 5, pp. 237–238, May 2020, doi: 10.1038/s41928-020-0411-2.

[3] R. Berdan *et al.*, "Low-power linear computation using nonlinear ferroelectric tunnel junction memristors," *Nat. Electron.*, vol. 3, no. 5, pp. 259–266, May 2020, doi: 10.1038/s41928-020-0405-0.

[4] Z. Yan, J. Chen, R. Hu, T. Huang, Y. Chen, and S. Wen, "Training memristor-based multilayer neuromorphic networks with SGD, momentum and adaptive learning rates," *Neural Netw.*, vol. 128, pp. 142–149, Aug. 2020, doi: 10.1016/j.neunet.2020.04.025.

[5] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems," *Nano Lett.*, vol. 10, no. 4, pp. 1297–1301, Apr. 2010, doi: 10.1021/nl904092h.

[6] M. Prezioso, F. Merrikh-Bayat, B. D. Hoskins, G. C. Adam, K. K. Likharev, and D. B. Strukov, "Training and operation of an integrated neuromorphic network based on metal-oxide memristors," *Nature*, vol. 521, no. 7550, pp. 61–64, May 2015, doi: 10.1038/nature14441.

[7] S. R. Nandakumar, I. Boybat, M. Le Gallo, E. Eleftheriou, A. Sebastian, and B. Rajendran, "Experimental demonstration of supervised learning in spiking neural networks with phase-change memory synapses," *Sci. Rep.*, vol. 10, no. 1, p. 8080, Dec. 2020, doi: 10.1038/s41598-020-64878-5.

[8] A. Renner, F. Sheldon, A. Zlotnik, L. Tao, and A. Sornborger, "Implementing backpropagation for learning on neuromorphic spiking hardware," in *Proc. Neuro-Inspired Comput. Elements Workshop*, Heidelberg Germany, Mar. 2020, pp. 1–3, doi: 10.1145/3381755.3381768.

[9] A. Serb, J. Bill, A. Khiat, R. Berdan, R. Legenstein, and T. Prodromakis, "Unsupervised learning in probabilistic neural networks with multi-state metal-oxide memristive synapses," *Nat. Commun.*, vol. 7, no. 1, Nov. 2016, Art. no. 12611, doi: 10.1038/ncomms12611.

[10] M. Hansen, F. Zahari, H. Kohlstedt, and M. Ziegler, "Unsupervised Hebbian learning experimentally realized with analogue memristive crossbar arrays," *Sci. Rep.*, vol. 8, no. 1, p. 8914, Dec. 2018, doi: 10.1038/s41598-018-27033-9.

[11] S. Boyn *et al.*, "Learning through ferroelectric domain dynamics in solid-state synapses," *Nat. Commun.*, vol. 8, no. 1, Apr. 2017, Art. no. 14736, doi: 10.1038/ncomms14736.

[12] B. Max, M. Hoffmann, H. Mulaosmanovic, S. Slesazeck, and T. Mikolajick, "Hafnia-based double-layer ferroelectric tunnel junctions as artificial synapses for neuromorphic computing," *ACS Appl. Electron. Mater.*, vol. 2, no. 12, pp. 4023–4033, Dec. 2020, doi: 10.1021/acsaelm.0c00832.

[13] M. Halter *et al.*, "Back-end, CMOS-compatible ferroelectric field-effect transistor for synaptic weights," *ACS Appl. Mater. Interfaces*, vol. 12, no. 15, pp. 17725–17732, Apr. 2020, doi: 10.1021/acsami.0c00877.
[14] M. Jerry *et al.*, "Ferroelectric FET analog synapse for acceleration of deep neural network training," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, Dec. 2017, pp. 1–4, doi: 10.1109/IEDM.2017.8268338.
[15] Y. W. Yin *et al.*, "Enhanced tunnelling electroresistance effect due to a ferroelectrically induced phase transition at a magnetic complex oxide interface," *Nat. Mater.*, vol. 12, no. 5, pp. 397–402, May 2013, doi: 10.1038/nmat3564.
[16] X. Liu, Y. Wang, J. D. Burton, and E. Y. Tsymbal, "Polarization-controlled Ohmic to Schottky transition at a metal/ferroelectric interface," *Phys. Rev. B, Condens. Matter,*, vol. 88, no. 16, Oct. 2013, Art. no. 165139, doi: 10.1103/PhysRevB.88.165139.
[17] Z. Xi *et al.*, "Giant tunnelling electroresistance in metal/ferroelectric/semiconductor tunnel junctions by engineering the Schottky barrier," *Nat. Commun.*, vol. 8, no. 1, Aug 2017, Art. no. 15217, doi: 10.1038/ncomms15217.
[18] Y. Heo, D. Kan, Y. Shimakawa, and J. Seidel, "Resistive switching properties of epitaxial $BaTiO_{3-\delta}$ thin films tuned by after-growth oxygen cooling pressure," *Phys. Chem. Chem. Phys.*, vol. 18, no. 1, pp. 197–204, 2016, doi: 10.1039/C5CP05333A.
[19] J. Li *et al.*, "Giant electroresistance in ferroionic tunnel junctions," *iScience*, vol. 16, pp. 368–377, Jun. 2019, doi: 10.1016/j.isci.2019.05.043.
[20] T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, "Ferroelectricity in hafnium oxide thin films," *Appl. Phys. Lett.*, vol. 99, no. 10, Sep. 2011, Art. no. 102903, doi: 10.1063/1.3634052.
[21] S. Fujii, M. Yamaguchi, S. Kabuyanagi, K. Ota, and M. Saitoh, "Improved state stability of HfO2 ferroelectric tunnel junction by template-induced crystallization and remote scavenging for efficient in-memory reinforcement learning," in *Proc. IEEE Symp. VLSI Technol.*, Honolulu, HI, USA, Jun. 2020, pp. 1–2, doi: 10.1109/VLSITechnology18217.2020.9265059.
[22] L. Bégon-Lours, M. Halter, Y. Popoff, and B. J. Offrein, "Ferroelectric, analog resistive switching in back-end-of-line compatible TiN/$HfZrO_4$/TiO_x junctions," *Phys. Status Solidi RRL Rapid Res. Lett.*, vol. 15, no. 5, Dec. 2020, Art. no. pssr.202000524, doi: 10.1002/pssr.202000524.
[23] E. Salje, "Polarons and bipolarons in tungsten-oxide, WO3−x," *Eur. J. Solid State Inorg. Chem.*, vol. 31, nos. 8–9, pp. 805–821, 1994.
[24] É. O'Connor *et al*., "Stabilization of ferroelectric HfxZr1−xO_2 films using a millisecond flash lamp annealing technique," *APL Mater.*, vol. 6, no. 12, Dec. 2018, Art. no. 121103, doi: 10.1063/1.5060676.
[25] S. Boyn, "Ferroelectric tunnel junctions: memristors for neuromorphic computing," Ph.D. dissertation, Dept. Mater. Sci., Université Paris Saclay, Gif-sur-Yvette, France, 2016, p. 175.
[26] P.-Y. Chen, X. Peng, and S. Yu, "NeuroSim: A circuit-level macro model for benchmarking neuro-inspired architectures in online learning," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 37, no. 12, pp. 3067–3080, Dec. 2018, doi: 10.1109/TCAD.2018.2789723.
[27] K.-H. Kim *et al.*, "A functional hybrid memristor crossbar-array/CMOS system for data storage and neuromorphic applications," *Nano Lett.*, vol. 12, no. 1, pp. 389–395, Jan. 2012, doi: 10.1021/nl203687n.
[28] W. J. Merz, "Domain formation and domain wall motions in ferroelectric BaTi$\mathrmO_3$ single crystals," *Phys. Rev.*, vol. 95, no. 3, pp. 690–698, Aug. 1954, doi: 10.1103/PhysRev.95.690.
[29] J. Lee, F. Chiu, and P. Juan, *Handbook of Nanoceramics and Their Based Nanodevices*, vol. 4. Stevenson Ranch, CA, USA: Amer. Sci. Publ., 2009.
[30] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. Hoboken, NJ, USA: Wiley, 2007.
[31] J. G. Simmons, "Richardson-Schottky effect in solids," *Phys. Rev. Lett.*, vol. 15, no. 25, pp. 967–968, Dec. 1965, doi: 10.1103/PhysRevLett.15.967.
[32] S. Heo *et al.*, "Band alignment of atomic layer deposited $(HfZrO_4)_{1-x}$ $(SiO_2)_x$ gate dielectrics on Si (100)," *Appl. Phys. Lett.*, vol. 107, no. 18, Nov. 2015, Art no. 182101, doi: 10.1063/1.4934567.
[33] A. Padovani, L. Larcher, O. Pirrotta, L. Vandelli, and G. Bersuker, "Microscopic modeling of HfO_x RRAM operations: From forming to switching," *IEEE Trans. Electron Devices*, vol. 62, no. 6, pp. 1998–2006, Jun. 2015, doi: 10.1109/TED.2015.2418114.
[34] L. Begon-Lours *et al.*, "A BEOL compatible, 2-terminals, ferroelectric analog non-volatile memory," in *Proc. 5th IEEE Electron Devices Technol. Manuf. Conf. (EDTM)*, Chengdu, China, Apr. 2021, pp. 1–3, doi: 10.1109/EDTM50988.2021.9420886.
[35] L. Begon-Lours *et al.*, "A back-end-of-line compatible, ferroelectric analog non-volatile memory," in *Proc. IEEE Int. Memory Workshop (IMW)*, Dresden, Germany, May 2021, pp. 1–4, doi: 10.1109/IMW51353.2021.9439611.