Received 9 July 2021; revised 28 August 2021; accepted 29 August 2021. Date of publication 1 September 2021;
date of current version 13 December 2021. The review of this paper was arranged by Editor D. Misra.

Digital Object Identifier 10.1109/JEDS.2021.3109347

High Temperature Reverse Bias (HTRB) & Temperature Humidity Bias (THB) Reliability Failure Mechanisms and Improvements in Trench Power MOSFET and IGBT

AI LOON OOI, DAVID GOH, AND VOON CHENG NGWAN

RND Technology Development, STMicroelectronics Pte Ltd., Singapore 569508

CORRESPONDING AUTHOR: D. GOH (e-mail: eng-hui.goh@st.com)

ABSTRACT High Temperature Reverse Bias (HTRB) reliability failure is found to be caused by huge amount of undesirable hydrogen proton (H^+) ions from packaging resin or external environment, while Temperature Humidity Bias (THB) reliability failure is known to be caused by moisture accumulation. A commonly known method of improving HTRB is by increasing phosphorus concentration in the PMD layer to enhance device gettering capability against H^+. However, this is usually achieved at the expense of THB reliability as excessive phosphorus on the PMD surface gives rise to moisture accumulation and caused THB failure. In this paper, we performed a series of experiments to uncover two elements in PMD that are responsible to getter H^+, which are Phosphorus-Oxygen-Hole-Center (POHC) and dangling bonds. We also discussed 2 possible ways to boost these H^+ gettering elements to improve HTRB reliability without the adverse impact on THB reliability: Utilization of Plasma Enhanced Chemical Vapor Deposition (PECVD) Phospho-Tetraethyl-Orthosilicate (PTEOS) in PMD layer to replace the commonly used Atmospheric Pressure Chemical Vapor Deposition (APCVD) or Sub Atmospheric Chemical Vapor Deposition (SACVD) Boro-Phospho-Tetraethyl-Orthosilicate (BPTEOS) and the introduction of Tetraethyl-Orthosilicate (TEOS) capping layer on PMD layer. Both methods have proven to greatly alleviate HTRB and THB reliability marginality problems.

INDEX TERMS Trench power device, power MOSFET, IGBT, reliability, HTRB, THB, Vth drift, Idss drift, PMD.

I. INTRODUCTION

With the widespread commercialization of trench-based power devices such as trench field plate power Metal Oxide Semiconductor Field Effect Transistor (MOSFET), trench super junction MOSFET, trench field-stop Insulated Gate Bipolar Transistor (IGBT) and trench MOS barrier Schottky (TMBS) to minimize on-state power consumption, reliability weaknesses such as High Temperature Reverse Bias (HTRB) and Temperature Humidity Bias (THB) are starting to surface as potential threat to hamper future technology development efforts, especially in the area of device scaling, edge termination design as well as the use of smaller, thinner and greener packages [1]–[3].

One of the common failure modes of HTRB is threshold voltage (Vth) drift, which can be caused by a convolution of many factors such as trench corner rounding, trench oxide interface quality, plasma charging, mobile ions, alpha-particles radiated from package [4], molding compound material [5], moisture [6], and so on. To prevent HTRB Vth drift, often, good protective dielectric layers such as post metal passivation or Pre-Metal Dielectric (PMD) or a combination of both are needed. These dielectric layers are usually made of BPTEOS film or PTEOS film [7] and they play several roles in the fabrication and operation of the circuit. First, it acts as an insulating layer between polysilicon and metal. Second, it reduces the parasitic capacitance between metal

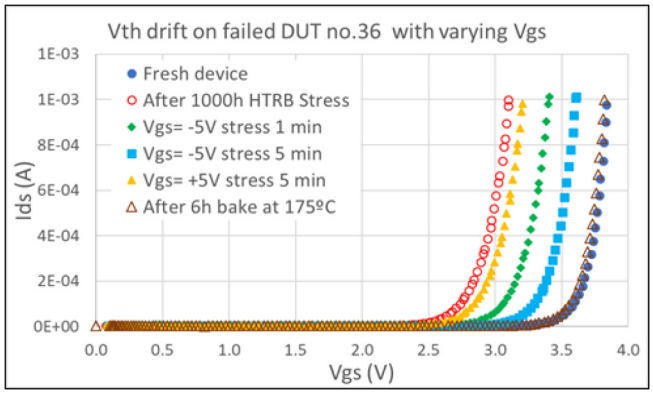

FIGURE 1. HTRB Vth failed DUT after HTRB stress and with ±5V gate stress for the time indicated [9].

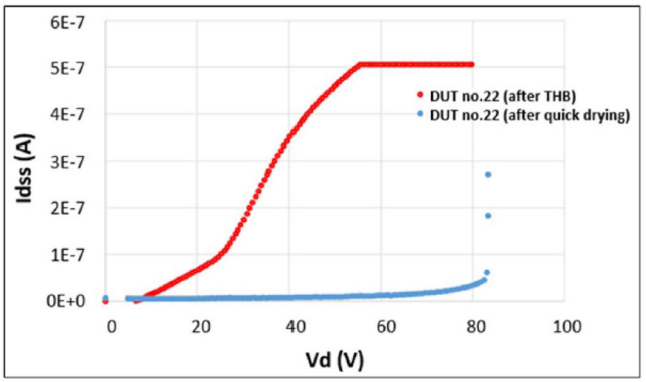

FIGURE 2. THB Idss failed DUT before and after quick drying at 175°C [10].

and the substrate. Third, and most importantly, in the reliability aspect, the addition of Phosphorus binds mobile atoms within the doped oxide, preventing them from reaching the gate oxide and altering device Vth [8].

In EDTM 2020 [9], we concluded that HTRB reliability failure in trench power MOSFET was a result of unwanted H^+ ions from external perturbations, likely from organic resin material in the package. Without strong dielectric protective layers, some of the H^+ ions may penetrate into device gate oxide and degrade the device performance, especially Vth. We identified H^+ ion as the source of contaminant by applying positive and negative gate stress on the HTRB failed part as shown in Fig. 1. It was observed that Vth recovered when negative gate voltage stress was applied, and the amount of recovery correlates with the stress time. On the other hand, when a positive gate stress was applied, Vth degraded in the same way as HTRB stress. This observation implies that the contaminants which diffused into the gate oxide during HTRB stress were positively charged. Subsequently, the same failed part was placed in the oven at 175°C for 6 hours and a full Vth recovery was observed. The fact that these positively charged ions were highly mobile at room temperature and completely moved away from gate oxide under oven bake further confirmed the identity of the contaminant as H^+ ion.

In EDTM 2021 [10], we also determined that THB reliability failure was a result of moisture accumulation on PMD surface due to high amount of Phosphorus. As shown in Fig. 2, by applying a quick high temperature to dry the failed THB part which was doped with high percentage of Phosphorus, a full Idss recovery was observed. This observation reconfirms the theory that Phosphorus being hydrophobic in nature [11], had prevented moisture absorption during THB reliability test and left an abundance of moisture accumulation on PMD surface. Thus, an electrical leakage path was formed on the PMD surface that ultimately brought about THB failure. In short, simply by increasing Phosphorus percentage in BPTEOS PMD to improve HTRB reliability cannot be done without an adverse impact to THB reliability.

Hence, to resolve these two reliability problems, it was imperative that we determined the elements in PMD layer that were responsible to getter H^+ and then focus on the solution to increase these amount of H^+ gettering elements. Our following experiments and results confirmed that these two elements were Phosphorus-Oxygen-Hole-Center (POHC) and dangling bonds.

Thereafter, we present two possible solutions in this paper to boost the amount of POHC or dangling bonds. First solution is the replacement of conventionally used PMD deposition technique of SACVD or APCVD with PECVD. The PECVD technique has effectively amplified the overall H^+ gettering capability by increasing the dangling bond density [9], [12]. The superior HTRB results were demonstrated in our experiment on both low voltage trench power MOSFET and high voltage trench field stop IGBT.

Second solution is a brand new PMD stack, with TEOS capping layer on top of the normal BPTEOS layer. Without the capping layer, it was impossible to find an optimized Phosphorus percentage in the PMD to balance both HTRB and THB performances. With capping layer, we can produce a PMD surface free of Phosphorus that prevents moisture build-up, and thus improves THB while keeping the PMD bulk with high level of Phosphorus percentage for more H^+ gettering sites and better HTRB performance.

II. EXPERIMENTAL

We fabricated 2 different types of power devices with 2 distinct voltage classes: a low voltage 80V n-channel trench power MOSFET device and a high voltage 650V n-channel trench field stop IGBT.

A 80V trench power MOSFET was produced with 1.3µm trench depth, 1.2µm trench pitch and 600Å gate oxide as shown in Fig. 3. The source, gate and edge termination electrodes were defined by Aluminium (Al) metallization, while drain electrode was formed by backgrinding process, followed by sputtering of back metallization layers Titanium (Ti)/Nickel Vanadium (NiV)/Silver (Ag). The top view of the interconnected metal electrode was illustrated in Fig. 4. Post metal passivation layer was omitted due to cost consideration. As such, PMD was the only device protection

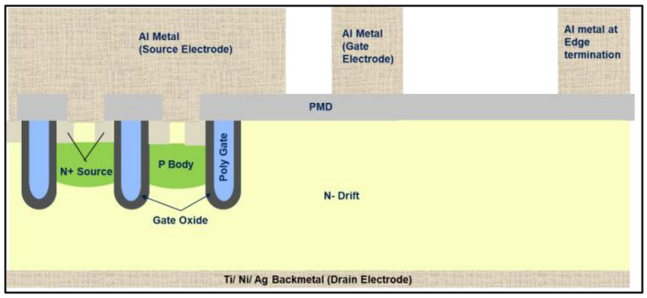

FIGURE 3. Schematic of 80V trench power MOSFET.

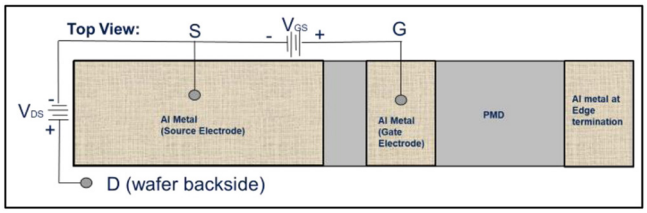

FIGURE 4. Top view of 80V trench power MOSFET.

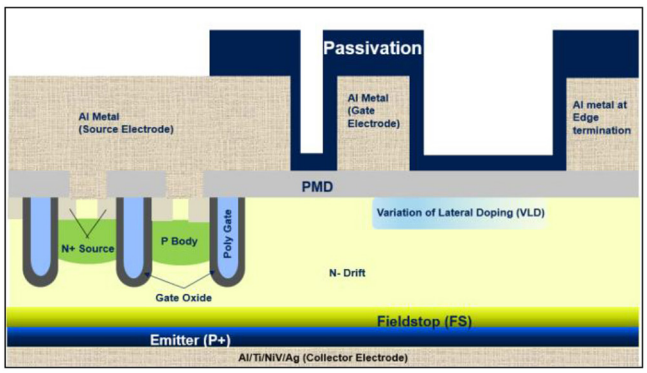

FIGURE 5. Schematic of 650V Trench Field Stop IGBT.

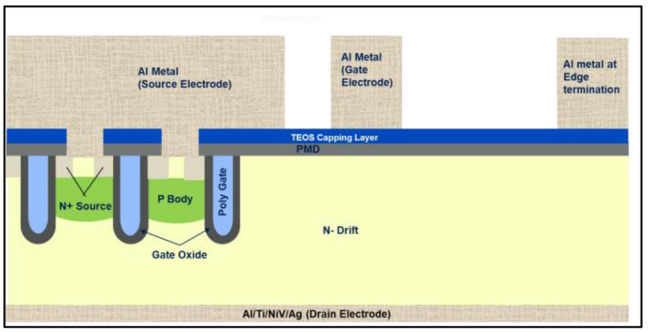

FIGURE 6. Schematic of 80V Trench MOSFET with Caping Layer.

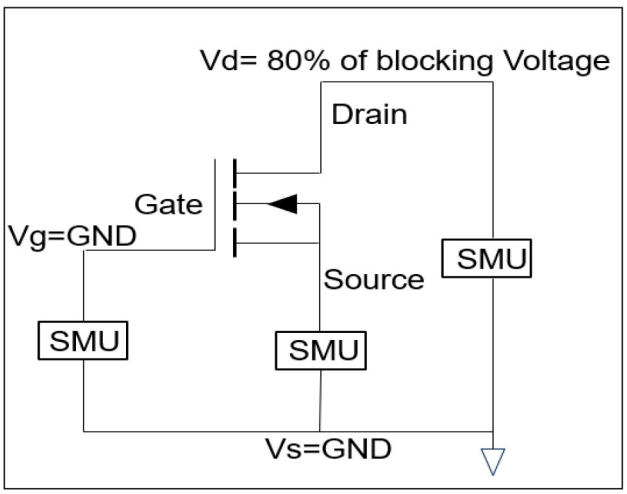

FIGURE 7. HTRB and THB Reliability Test Setup.

layer in the opening area between source electrode to gate electrode or gate electrode to edge termination metal.

A 650V trench field stop IGBT device was fabricated with 5.0μm trench depth, 4.0μm trench pitch and 1100Å gate oxide as shown in Fig. 5. Likewise, source, gate and edge termination electrodes were defined by Alumnium (Al) metallization. Backside of the device was formed by back-grinding process, followed by backside implant to form the P^+ emitter and N^+ Field-Stop (FS) region, and completed with backside metallization stack of (Al/Ti/NiV/Ag). As opposed to low voltage power MOSFET, in addition to PMD layer, post metal passivation was deposited to further protect the opening area between source electrode to gate electrode and gate electrode to edge termination metal. With the presence of passivation in IGBT device, THB failure was no longer our concern as Silicon Nitride (SiN) passivation was a good barrier to block external moisture.

Experiments were conducted with focus to determine the elements in PMD layer which were responsible to getter the H^+, and to invent possible solutions to increase these elements with the eventual target to improve HTRB reliability and at the same time, reduce its possible impact to THB reliability. Firstly, during PMD BPTEOS deposition process, a series of different Phosphorus percentage (by weight %) samples were prepared by varying the flow of precursor triethylphosphate (TEPO). Secondly, various PMD deposition techniques were studied, the APCVD, SACVD and PECVD. Thirdly, the use of PECVD technique in PMD deposition as HTRB solution was repeated on high voltage trench field stop IGBT device. Lastly, the solution of using TEOS capping layer was introduced on top of the existing PMD layer as shown in Fig. 6. The thickness of the entire PMD stack was optimized to factor in technical difficulties in contact formation and metal plasma etching.

All experimental wafers were assembled and packaged with several Device Under Test (DUTs) selected per wafer per condition for HTRB and THB reliability tests as shown in Fig. 7 with a duration of 168 hours, 500 hours, and 1000 hours, in accordance with JEDEC standard [13].

HTRB test was performed with a thermal stress set at 175°C, whereas THB was performed with less thermal stress of 85°C, but with additional 85% relative humidity (R.H.) of moisture. In both HTRB and THB, the same amount of electrical stress was applied which was 80% of blocking

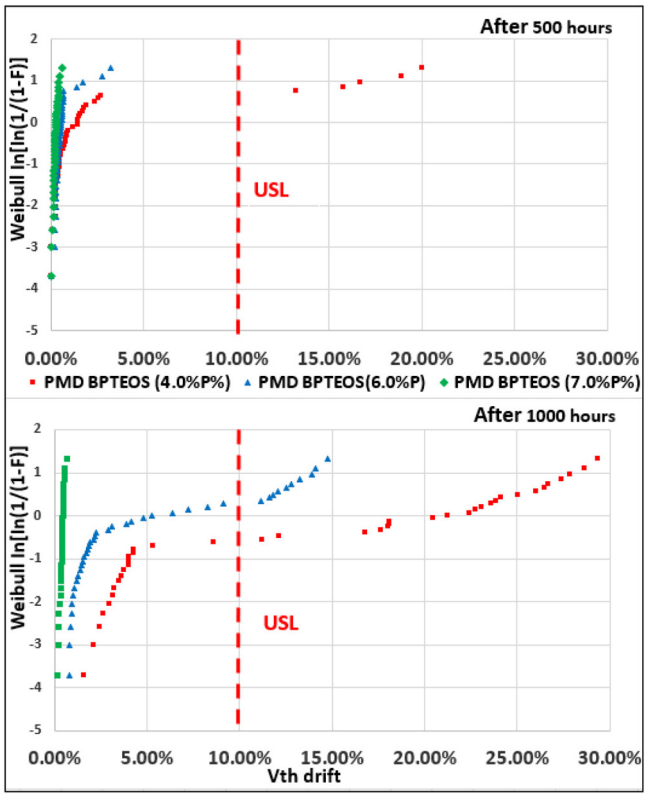

FIGURE 8. Weibull Distribution of HTRB Vth Drift after 500 and 1000 hours with various Phosphorus percentage [10].

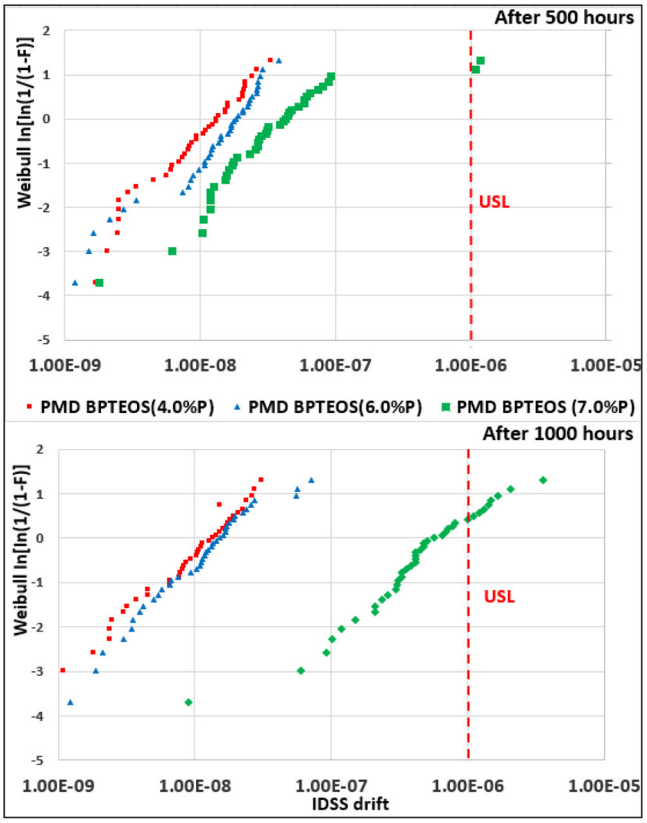

FIGURE 9. Weibull Distribution of THB Idss values after 500 and 1000 hours with typically 1μA as spec limit [10].

voltage to the drain electrode, at 64V for MOSFET and 520V for IGBT. Both gate and source electrodes were grounded.

Electrical parameters such as Vth and drain to source leakage current (Idss) were measured at room temperature, before and after HTRB and THB stress tests. Vth was tested with source electrode grounded, Vg = Vd and Vg(Vth) was measured when Id = 250μA.

III. RESULTS AND DISCUSSION

First experiment was done with the conventional approach by increasing the amount of Phosphorus in PMD BPTEOS which was deposited with the common SACVD technique. HTRB results were shown in Fig. 8. With relatively low Phosphorous percentage of 4.0% and 6.0%, it was observed that the Vth of some DUTs began to drift at 500 hours and the amount of drift got worse after 1000 hours, with a significant number of DUTs failed the 10% reliability spec. By further increased the Phosphorous percentage to 7.0%, there was basically, no Vth drift seen. At first glance, the HTRB reliability solution should be simply to apply the 7.0% phosphorus concentration in PMD BPTEOS layer.

However, with the exact same condition of 7.0% Phosphorus concentration, the corresponding THB reliability test (Fig. 9) showed huge number of DUTs having Idss drift and failed the 10% specification. In short, by adjusting Phosphorous percentage alone as the solution had resulted in a tradeoff between HTRB and THB performances. Therefore, there was a need to develop a new solution.

In the second set of experiment, the impact of HTRB reliability on different PMD deposition techniques was studied in detail. As shown in Fig. 10, PECVD PTEOS (4.0%P) showed the best performance with insignificant Vth drift. SACVD BPTEOS (4.0%P) and APCVD BPTEOS (4.0%P) presented catastrophic failures after 1000hrs of HTRB test.

It was initially postulated that PMD PTEOS contained two types of H^+ gettering centers, the POHC [14] and the dangling bonds [15]. POHC was a center with a hole trapped on a non-bridging oxygen atom bonded to a phosphorous atom while dangling bond consisted of an unpaired electron in trivalently bonded silicon atom [6], [16].

To confirm the presence of POHC and dangling bond as H^+ gettering centers, Fourier Transform Infrared Resonance (FTIR) absorption spectrum was carried out for three different PMD deposition techniques SACVD, APCVD & PECVD as shown in Fig. 11. The spectrum was normalized by subtracting the substrate spectra followed by the identification and deconvolution of P = O peaks, and the main analysis was to quantify the P = O bonding by integrating the area under the P=O peak. The PECVD (4.0%P) P = O peak was centered at 1306 cm^{-1} and presented an area of 0.62 while APCVD (4.0%P) and SACVD (4.0%P) areas were 0.28 and 0.20 respectively.

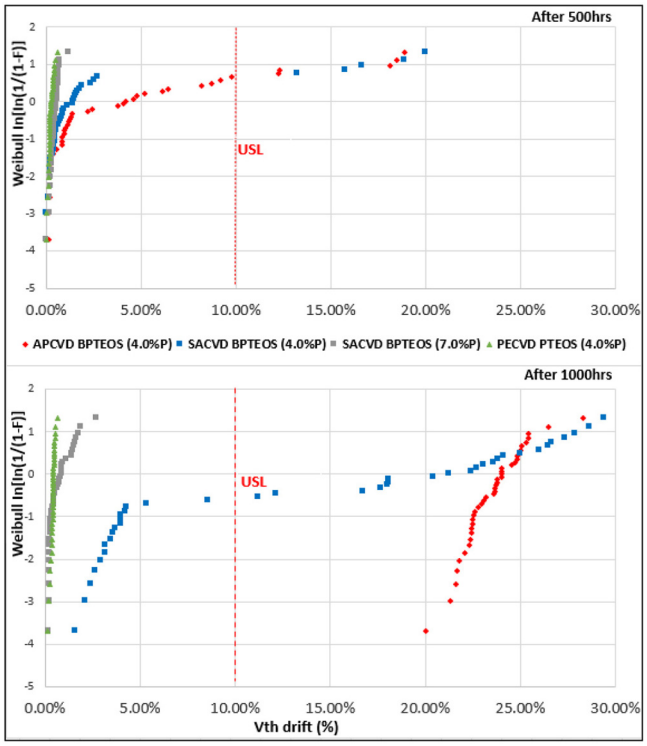

FIGURE 10. Weibull Distribution of HTRB Vth Drift after 500 and 1000 hours with different PMD deposition techniques [9].

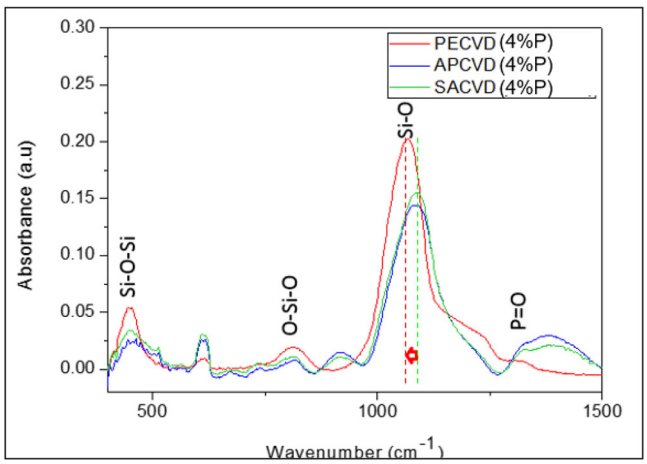

FIGURE 11. FTIR spectrum of PECVD (4%P4), APCVD (4%P) and SACVD (4%P) [9].

These sets of results implied that the quantity POHC sites which can be characterized by P = O double bonds [16] was the highest in PECVD (4.0%P) film, and hence, better HTRB performance [9].

In addition, we observed a shift of Si-O peak in PECVD film at wavelength of 1068cm^{-1} comparing to the Si-O peak of 1166 cm^{-1} from both APCVD and SACVD films. This showed a variation in the vibrational frequency that suggested a variation of the bond's hybridization state or a change of an atom in the bonding system. In this case, a Si-O shift towards lower frequencies indicated an increase

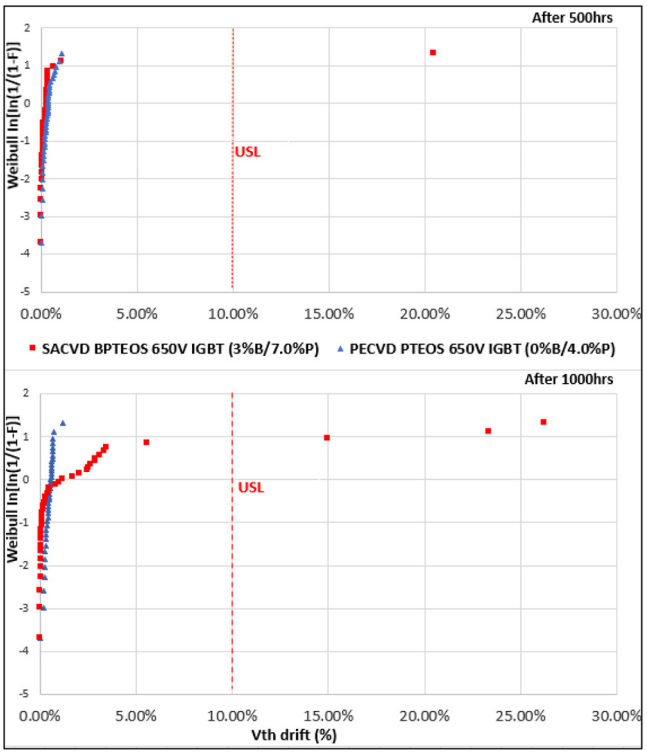

FIGURE 12. Weibull Distribution of HTRB Vth Drift after 500 and 1000 hours for 650V Trench Field Stop IGBT.

of non-stoichiometric oxide SiOx (x < 2) bonding [10]. Therefore, we deduced qualitatively that PECVD technique produced more dangling bond gettering sites [17].

With PECVD PTEOS PMD stood out as the best candidate for HTRB reliability for having the most abundant amount of H^+ gettering elements POHC & dangling bonds, a high voltage 650V n-channel trench field stop IGBT with PECVD PTEOS was put to test with HTRB stress. From Fig. 12, it was observed that after 500 hours of HTRB stress, there was one Vth drift part from SACVD BPTEOS while the whole population of PECVD PTEOS remained good. After 1000 hours, more parts with SACVD BPTEOS started to drift while parts with PECVD PTEOS continued to show resilience against Vth drift. This confirmed that PECVD PTEOS was the best solution to block the external H^+ and this solution not only work in low voltage power devices, but in high voltage power devices as well.

Nonetheless, not all power devices are suited to use PMD PTEOS deposition technique as some products require PMD planarization due to constraint in contact design. PECVD deposition technique, unlike SACVD or APCVD has inferior performance in terms of planarization. Hence, a second solution was required. This solution will need an exposed SACVD PMD surface which is free of Phosphorus to avoid moisture pile up while maintaining high amount of Phosphorus in the BPTEOS bulk layer. With this in consideration, an undoped TEOS capping layer was introduced on top of BPTEOS.

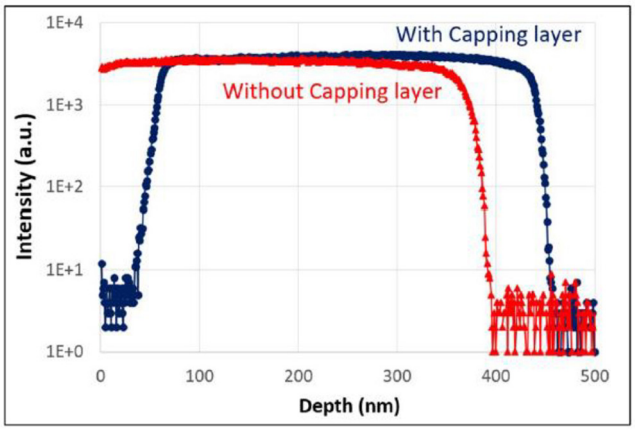

FIGURE 13. TOF-SIMS analysis of the PMD stack with and without the TEOS capping [10].

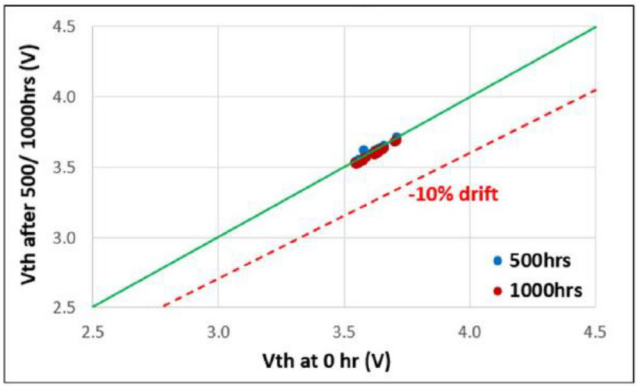

FIGURE 14. Vth performance for devices with TEOS capping layer before and after HTRB stress at 500 and 1000 hours [10].

Fig. 13. showed the Time-of-flight Secondary Ion Mass Spectrometry (TOF-SIMS) analysis of the PMD stack with and without the TEOS capping layer. Without the capping layer, there was a high Phosphorus concentration on the PMD surface and with the presence of capping layer, there was a thin layer of exposed PMD surface ~700Å with insignificant Phosphorus concentration. The corresponding HTRB and THB reliability performances were shown in Figs. 14 & 15. It is clearly indicated that with TEOS capping layer, the initial HTRB and THB weaknesses were completely resolved.

IV. CONCLUSION

In this paper, we discussed the failure mechanism of HTRB reliability Vth drift and THB Idss drift. HTRB reliability failed because of excessive H^+ entering the gate oxide region due to poor gettering capability of PMD layers. THB Idss drift was a by-product of high Phosphorus percentage in the PMD layer which was normally adjusted to improve gettering capability. With high Phosphorus percentage on PMD surface, moisture was trapped and thereby causing THB failure.

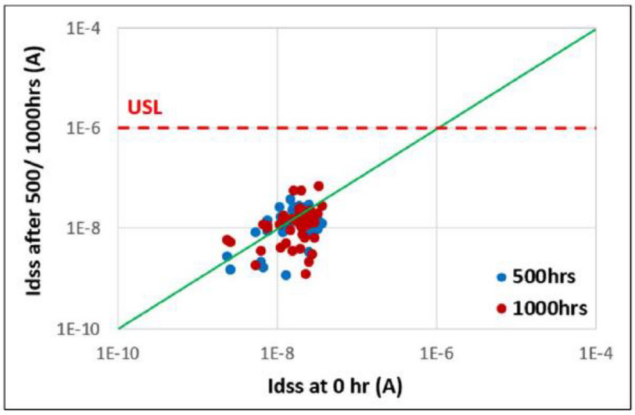

FIGURE 15. Idss performance for devices with TEOS capping layer before and after THB stress at 500 and 1000 hours [10].

With the above known failure mechanisms, we conducted experiments to verify the elements in PMD layer which were responsible for H^+ gettering. Both POHC and dangling bonds were proven to have the ability of trapping H^+ ions and preventing them from reaching device gate oxide region.

One of the PMD deposition techniques PECVD was shown to produce dielectric film with abundance of both POHC and dangling bonds. This solution was proven to be effective, not only in 80V trench power MOSFET, but also in high voltage class 650V trench field stop IGBT.

However, for technology that requires smooth topology and planarization, PECVD solution might not be applicable. Considering this limitation, another innovation technique: TEOS capping layer was introduced in the PMD stack. This layer allowed PMD surface to be almost free of Phosphorus (better THB) while maintaining high Phosphorus percentage in the bulk (better bulk). In conclusion, this new technique basically resolved the HTRB-THB trade-off.

ACKNOWLEDGMENT

The authors would like to thank D. Adnan, K. M. Wong, B. K. Tung, C. T. Yong, C. W. Khor, S. Amico, N. Sabes, L. F. Lai, D. Corona, M. Micciche for wafer fabrication and testing, E. Carollo for the many helpful technical discussions, T. C. Lee and M. Castorina for project sponsorship.

REFERENCES

[1] D. Mishra *et al.*, " Packaging innovations for high voltage (HV) GaN technology," in *Proc. IEEE 67th Electron. Compon. Technol. Conf.*, May/Jun. 2017, pp. 1480–1484.

[2] J. Hao, M. Rioux, and O. O. Awadelkarim, "Observation of negative bias temperature instabilities in parasitic P-channel mosfets occurring during high-temperature reverse-bias stressing of trench-gated N-channel MOSFETs," in *Proc. IEEE Int. Integr. Rel. Workshop*, Oct. 2011, pp. 129–132.

[3] C. Zorn and N. Kaminski, "Acceleration of temperature humidity bias (THB) testing on IGBT modules by high bias levels," in *Proc. ISPSD*, May 2015, pp. 385–388.

[4] T. Nishiwaki *et al.*, "Alpha-particle shielding effect of thick copper plating film on power MOSFETs," in *Proc. ISPSD*, 2019, pp. 91–94.

[5] A. Scandurra, R. Zafarana, Y. Tenya, and S. Pignataro, "Breakdown voltages phenomena at molding compound-chip interface," in *Proc. 26th IEEE/CPMT Int. Electron. Manuf. Technol. Symp.*, Santa Clara, CA, USA, 2000, pp. 1–9.

[6] M. Yoshimaru and H. Matsuhashi, "Moisture resistance of annealed borophosphosilicate glass films for very large scale integrated circuit applications," *J. Electrochem. Soc.*, vol. 143, no. 9, p. 3032, 1996.
[7] G. S. Wolf and R. N. Tauber, *Silicon Processing for the VLSI Era*, vol. 1. Sunset Beach, CA, USA: Process Tecnol. SE Lattice Press, 2000.
[8] E. P. Ferlito, G. Pizzo, R. De Gregorio, G. Anastasi, R. Ricciari, and D. Mello, "TOF-SIMS characterization of Boron and phosphorus distribution in sub-atmospheric chemical vapour deposition borophosphosilicate glass (SA-CVD BPSG) films," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2013, pp. 5B.3.1–5B.3.7, doi: 10.1109/IRPS.2013.6532026.
[9] C. Jacquemont, K. M. Wong, and D. Goh, "Hydrogen proton induced HTRB reliability degradation in trench power devices," in *Proc. IEEE Electron Devices Technol. Manuf. Conf.*, Apr. 2020, pp. 1–3.
[10] D. Goh, W. J. Chen, F. Tahir, S. P. Lee, and V. C. Ngwan, "HTRB & THB reliability improvement using capping layer in power discrete trench devices," in *Proc. EDTM*, 2021, pp. 1–3.
[11] A. G. Thorsness and A. J. Muscat, "Moisture absorption and reaction in BPSG thin films," *J. Electrochem. Soc*, vol. 150, no. 12, p. F219, 2003.
[12] W. M. Paulson and R. W. Kirk, " The effects of phosphorus-doped passivation glass on the corrosion of aluminum," in *Proc. 12th Ann. Rel. Phys. Symp.*, Apr. 1974, pp. 172–179.
[13] *Temperature, Bias, and Operating Life*, JEDEC Standard JESD22A-108, 2009.
[14] M. Fanciulli, E. Bonera, E. Carollo, and L. Zanotti, "EPR and UV-Raman study of BPSG thin films: Structure and defects," *Microelectron. Eng.*, vol. 55, nos. 1–4, pp. 65–71, 2001.
[15] W. L. Warren, M. R. Shaneyfelt, D. M. Fleetwood, P. S. Winokur, and S. Montague, "Electron and hole trapping in doped oxides," *IEEE Trans. Nucl. Sci.*, vol. 42, no. 6, pp. 1731–1739, Dec. 1995.
[16] P. M. Lenahan, "Hole traps and trivalent silicon centers in metal/oxide/silicon devices," *J. Appl. Phys.*, vol. 55, no. 10, p. 3495, 1984.
[17] D. V. Tsu, G. Lucovsky, and B. N. Davidson, "Effects of the nearest neighbors and the matrix on SiH stretching vibrations in the amorphous SiO_r:H ($0<r<2$) alloy system," *Phys. Rev. B, Condens. Matter*, vol. 40, p. 1795, Jul. 1989.

AI LOON OOI received the master's degree from the University of Technology Malaysia in 2014. She has seven years of experience in semiconductor industry mainly focus on high voltage IGBT and Diode. She is currently working as a Process Integration with STMicroelectronics, Singapore.

DAVID GOH received the Engineering degree (Hons.) from University Putra Malaysia in 1999. He is a Technology Development Manager working with STMicroelectronics, Singapore. He has more than 20 years of experience in semiconductor manufacturing, bringing ideas to industrial products under mass production. He is well-versed in technology, such as diode, advance bipolar, IGBT, low and high voltage power MOSFET. He has authored/coauthored in a few papers and patents focusing in IGBT and reliability.

VOON CHENG NGWAN received the M.Eng. degree. He was a Research Scholar with the National University of Singapore. He has 20 years of experience in semiconductor research, wafer fabrication, and testing. He is currently working with STMicroelectronics, Singapore, researching in power device physics, process, and reliability.