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Subthreshold Swing in Silicon Gate-All-Around Nanowire and Fully Depleted SOI MOSFETs at Cryogenic Temperature

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ABSTRACT Subthreshold swing (SS) in a silicon gate-all-around (GAA) nanowire MOSFET with zero body factor is examined from room temperature (RT) down to 4 K. A fully depleted (FD) SOI MOSFET is also evaluated. The values of SS of both transistors decrease in proportional to temperature (T) but start to saturate below 18K, similar to transistors with non-zero body factor in the literature, indicating that the body factor is not related to the SS saturation phenomena at very low temperatures.

INDEX TERMS Nanowire, MOSFET, subthreshold swing.

I. INTRODUCTION

The quantum computer has attracted much attention for solving certain complex problems much faster than classical computers. In the real applications of quantum computers, qubits will be integrated with large-scale CMOS circuits operating at cryogenic temperatures. Therefore, the characterizations of MOSFETs at cryogenic temperatures become increasingly important. One of the merits of cryogenic temperature MOSFET operation is the suppressed subthreshold leakage current, because subthreshold swing (SS) is given by

$$SS = (k_B T/q)\ln 10(1+\gamma), \quad (1)$$

$$\gamma = C_D/C_{ox}, \quad (2)$$

under the assumption that the short channel effect is negligible, where k_B is the Boltzmann constant, T the temperature, q the elementary charge, γ the body factor, C_D the depletion capacitance, and C_{ox} the gate capacitance [1]–[2]. According to Eq. (1), the ideal value of 60 mV/dec at T = 300K (room temperature) is achieved when $\gamma = 0$. SS decreases in proportion to the temperature and its value should be as small as 0.79 mV/dec at 4K when $\gamma = 0$. However, it has been reported that the measured SS value is not in proportion to the temperature at very low temperatures and saturates around 10mV/dec [3]–[9]. The reasons for this saturation phenomena have been argued and one of the possible mechanisms would be the increased interface traps at low temperatures [4]–[6], [8]–[9].

In this work, we focused on the effect of body factor (γ) in Eq. (1) on the SS saturation phenomena. γ is given by Eq. (2) and is an indicator of how strongly the body is coupled to the channel. From the electric characteristics point of view, on the other hand, γ is an indicator of the body effect and defined as,

$$\gamma = |V_{TH}/V_{BS}|, \quad (3)$$

where V_{TH} is the threshold voltage and V_{BS} the body voltage [1]–[2]. γ shows how much V_{TH} is shifted by V_{BS}. At given temperature, the minimum and ideal SS is achieved in a transistor with $\gamma = 0$, where the coupling between the gate and the channel is strongly enough and the body coupling is negligible. A gate-all-around (GAA) nanowire transistor, in which the nanowire channel is completely surrounded by the gate electronide, is one of the structures that can attain $\gamma = 0$.

Most of the previous work on the SS measurements at low temperature have been done for transistors with large γ, and few measurements have been reported on transistors with zero body factor. In order to investigate the effect

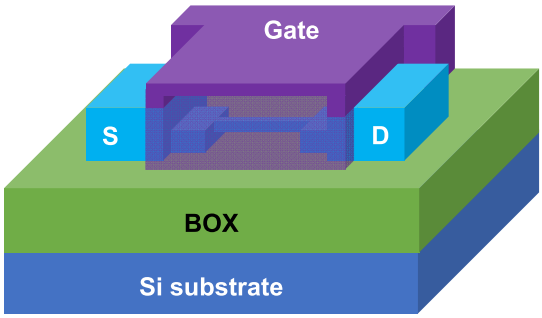

FIGURE 1. A three-dimensional schematic view of a fabricated silicon GAA nanowire MOSFET.

of γ on the SS saturation, we fabricated silicon gate-all-around (GAA) nanowire transistors with $\gamma = 0$ and SS = 60mV/dec at room temperature and carefully measured SS at various temperatures. As a reference, fully depleted (FD) SOI MOSFETs are also fabricated and evaluated. This paper is the extended version of Reference [10], but all the data in this paper were re-measured and the device temperature was accurately calibrated by a pn diode temperature sensor.

II. DEVICE FABRICATION AND BODY FACTOR

Fig. 1 shows a three-dimensional schematic of the n-type GAA nanowire transistor. The fabrication process is based on references [11]–[12]. An SOI substrate with the SOI thickness of $t_{SOI} = 80$ nm and the buried oxide thickness of $t_{BOX} = 200$ nm was used. The active region of SOI was locally thinned down to 15 nm by oxidation by which source/drain regions remained thick to reduce parasitic resistance. The nanowire pattern was defined by the electron beam lithography and reactive ion etching, followed by the wet-etching process which etches BOX under the nanowire forming a suspending nanowire from BOX. A gate oxide was thermally grown ($t_{ox} = 7$ nm) and poly-Si was deposited for a gate electrode by which the GAA structure is formed. Length (L) and width (W) of nanowire are 250 nm and 10 nm, respectively. Effective width (W_{eff}) is the peripheral of the nanowire and is 50 nm. The gate length is 30μm, so the source/drain edges locate outside of nanowire. The source/drain doping concentration is approximately $2x10^{20}$ cm^{-3}. For a reference, a planar n-type FDSOI MOSFET with W = 20 μm and L = 30 μm was also fabricated and evaluated, where $t_{SOI} = 15$ nm in the SOI channel and $t_{SOI} = 80$ nm in source/drain regions.

I_{DS} - V_{GS} characteristics were carefully measured with gate voltage (V_{GS}) at an interval of 2.5 mV. Fig. 2 shows measured I_{DS} - V_{GS} characteristics with different V_{BS} at room temperature. The I_{DS} - V_{GS} curve is shifted by V_{BS} in the FD SOI MOSFET. The γ value is 0.036, where γ is defined in Eq. (3). On the other hand, the curve is never shifted in the GAA nanowire MOSFET. The zero body factor in the GAA nanowire MOSFET is confirmed.

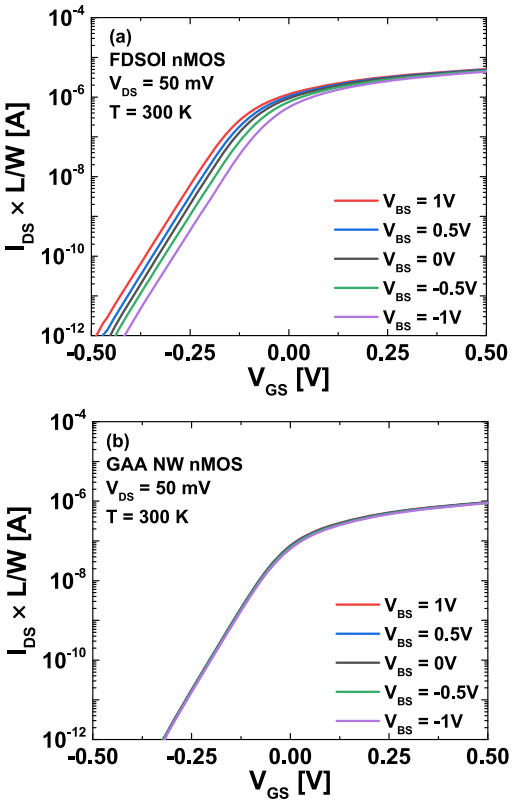

FIGURE 2. Measured I_{DS}-V_{GS} characteristics with different V_{BS} at room temperature in (a) FDSOI and (b) GAA nanowire nMOSFETs. V_{DS} is 50mV. I_{DS} is normalized to W/L for fair comparison, where W_{eff} is used for W in the nanowire MOSFET.

In this study, SS is defined as an average value in the range from $I_{DS} \times L/W = 10^{-11}$ to 10^{-10} [A]. SS at room temperature is 62.5 mV/dec for the FDSOI MOSFET and 60.45 mV/dec for the nanowire MOSFET. It is confirmed that the GAA nanowire transistor shows an almost ideal value of SS as well as zero body factor at room temperature.

III. CHARACTERISTICS AT CRYOGENIC TEMPERATURE

Fig. 3 shows the temperature dependence of I_{DS} - V_{GS} characteristics of the FDSOI and GAA nanowire MOSFETs. As the temperature decreases, V_{TH} increases, drain current at on-state increases, and the subthreshold slope becomes steeper in both FDSOI and GAA nanowire MOSFETs.

Fig. 4 shows the SS values as a function of normalized I_{DS} ($I_{DS} \times L/W$) in FDSOI and GAA nanowire MOSFETs. SS decreases with the temperature but the decrease in SS becomes gradual below 18K in both MOSFETs. SS values at 18K, 10K, and 4K are the almost the same in the FDSOI MOSFET. In the nanowire MOSFETs, the oscillations of SS are observed at 10K and 4K, and the SS value in the range of $I_{DS} \times L/W$ from 10^{-11} to 10^{-10} [A] increases at 4K due to the SS peak. It is found that these oscillations are observed in other nanowire MOSFETs. The oscillations are different depending on nanowire transistors, but in the same nanowire

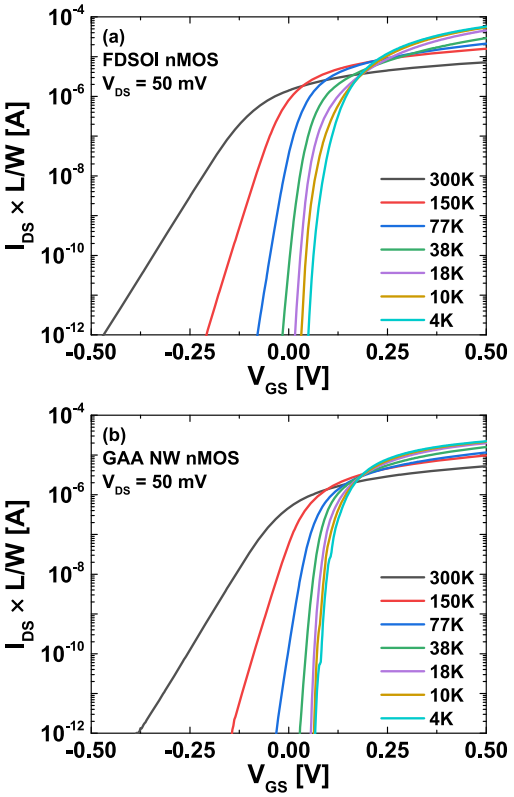

FIGURE 3. Measured subthreshold characteristics at different temperatures from 300K down to 4K in (a) FDSOI and (b) GAA nanowire MOSFETs.

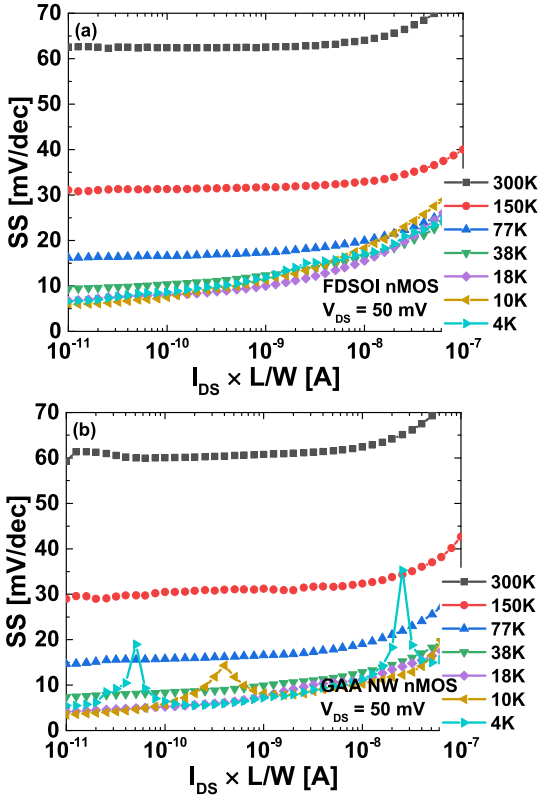

FIGURE 4. Measured SS as a function of normalized I_{DS} at different temperatures in (a) FDSOI and (b) GAA nanowire MOSFETs. SS is defined as an average value between I_{DS}×L/W=10^{-11} and 10^{-10} [A].

transistor the oscillations are reproducible when repeatedly measured as shown in Fig. 5. The SS oscillations may be caused by the Coulomb blockade due to the potential fluctuation in nanowire channel caused by the slight nanowire width fluctuations [11]. The SS oscillations are never observed in FDSOI MOSFETs.

Fig. 6 shows the SS values as a function of the temperature. The ideal SS with $\gamma = 0$ ((k_BT/q) ln10) is shown as a straight line. For the FDSOI MOSFETs, SS is slightly larger than the ideal SS line at room temperature. SS decreases along with the ideal SS, starts to deviate at 18K, and almost saturate below 10K. At 18K, SS is 7.5 mV/dec in the FDSOI MOSFETs, which is 2.1 times larger than the ideal value. For the nanowire MOSFETs, SS is on the ideal SS line and decreases along with the ideal SS. At 18K, SS is 4.7 mV/dec in the nanowire MOSFETs, which is 1.3 times larger than the ideal value, indicating that the SS saturation starts at 18K.

The effect of the Coulomb blockade is superimposed below 10K in the nanowire MOSFET, but the SS value smaller than 4.7 mV/dec is not observed in any I_{DS}×L/W range as shown in Fig. 4(b). It is concluded that the SS saturation at low temperature occurs even in a nanowire MOSFET with $\gamma = 0$. Fig. 6 also shows reported SS in the literature [3]–[8]. Irrespective of SS at room temperature, all transistors show the SS saturation below around 50K.

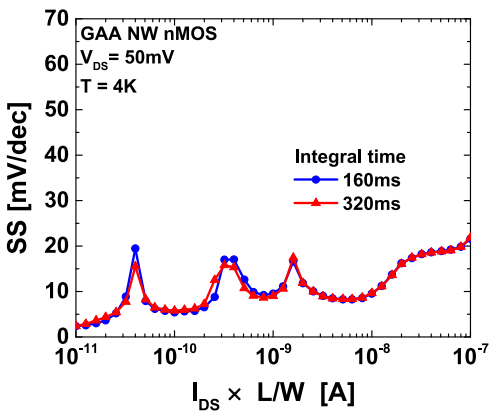

FIGURE 5. Measured SS as a function of normalized I_{DS} at 4K in another GAA nanowire MOSFET. Different oscillations from those in Fig. 4(b) are observed. The oscillations are reproducible even when the measurement integral time is varied.

It is considered that the simple interface trap model cannot explain the observed phenomena either, because one have to assume impossibly high N_{it} ($\sim 10^{16}$ cm^{-2}) in this model [5]. Recently, the band-tail extension model has been proposed to explain the temperature-independent SS at low temperature [3]. For quantum computing with peripheral large-scale CMOS circuits, accurate device models at low temperature are strongly required.

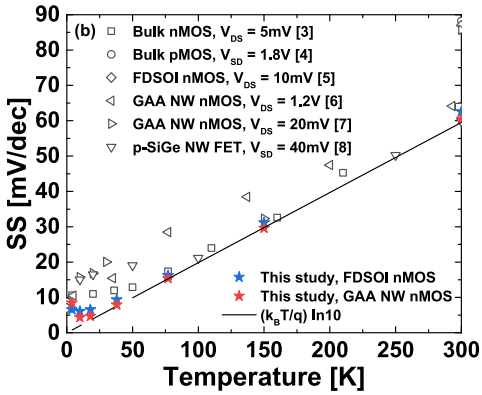

FIGURE 6. Measured SS as a function of the temperatures in FDSOI and GAA nanowire MOSFETs. Reported SS in the literature [3]–[8] are also shown.

IV. CONCLUSION

Subthreshold swing in a GAA nanowire transistor with zero body factor and ideal SS at room temperature was investigated at cryogenic temperature. It is experimentally confirmed that the SS saturation phenomena at low temperatures occurs even in the transistor with no body factor.

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