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New Compact Modeling Solutions for Organic and Amorphous Oxide TFTs

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ABSTRACT We review recent compact modeling solutions for Organic and Amorphous Oxide TFTs (OTFTs and AOS TFTs, respectively), which were developed, under the framework of the EU-funded project DOMINO, to address issues specifically connected to the physics of these devices. In particular, using different approaches, analytical equations were formulated to model the Density of States (DOS), different transport mechanisms, trapping/de-trapping, drain current, stress, capacitances, frequency dispersion and noise. The final TFT models were, after implementation in Verilog-A, validated by means of the design and simulation of test circuits.

INDEX TERMS Thin film transistors, organic thin film transistors, semiconductor device modeling, semiconductor device noise.

I. INTRODUCTION

Printed and flexible TOLAE (thin, organic and large area electronics) circuit design has been limited because to the lack of available compact device models to carry out accurate designs of TOLAE circuits. The design community at large need a user-friendly integration of OTFT and Amorphous Oxide Semiconductor (AOS) TFT compact models into industry standard Electronic Design Automation (EDA) design tools to reduce design cycle duration [1]–[7].

Some of the drawbacks of many organic and AOS TFT compact models are their weak physical basis, a limited accuracy, a difficult parameter extraction procedure, and too cumbersome expressions with a high computation cost for industrial applications. Very often, the lack of physical parameters leads to a remarkable process fabrication dependent accuracy [8], [9].

In addition, compact organic and AOS TFT models need to be fast to be used in future applications without sacrificing accuracy [10]. In active matrix backplanes for high resolution

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displays, the number of TFTs to be simulated could reach 10^7, so fast and computationally efficient models are needed.

The EU-funded DOMINO project (2014-18) aimed at filling the gap between printed and flexible technology and design by developing compact organic and AOS TFT model libraries, to be integrated in commercial Electron Design Automation (EDA) environments for full large area low cost circuit design for novel printed and flexible applications.

The development of those compact models was possible by proposing new solutions to address the main physical effects which control the behavior of OTFTs and AOS TFTs: DOS, charge transport, trapping, stress, noise, frequency dispersion, ...

This paper reviews the main compact modeling approaches developed to target the main physical effects and mechanisms in OTFTs and AOS TFTs, as well as the resulting device models derived from these approaches. We will also review the validity of those models when used for TFT circuit simulation.

Two modeling approaches were used for each type of device. OTFTs were modeled using a charge approach (Section II-A) which, after linearization around a zero drain-source voltage and additional approximations can be reduced to the formulation of the so-called Unified Modeling and Extraction Method (UMEM), which allows simpler expression and a straightforward parameter extraction procedure (Section II-B).

In Section III-A, AOS TFTs were modeled basing on assuming a double exponential DOS and trap-limited conduction and percolation as the dominant transport mechanism, which is valid for mature technologies with a gate voltage operation range approaching the conduction band. In Section III-B an adapted UMEM approach is applied if both deep and tail states have to be considered and the operation range is such that the Fermi level is far enough to the conduction band to neglect percolation effects.

Section IV targets the low frequency noise in organic and AOS TFTs. Finally, Section V show results of the incorporation of the models to circuit design tools by means of their implementation in Verilog-A. Good agreement was observed between modeled results and experimental data and TCAD simulations of several test circuits.

II. OTFT MODELING

As indicated in Section I, two approaches were used to develop a compact OTFT model: a charge-based approach [3, 3a] and a simplified model based on the so-called Unified Modeling and Extraction Method (UMEM), which allows direct extraction of model parameters [13], [14].

Actually, the UMEM model can be derived from a linearization, with respect to an effective drain-source voltage, of the charge-based model for the drain current. Both approaches assumed a charge transport based on Variable Range Hopping [15], [16] and a single exponential DOS. The expressions of the drain current in both approaches have the same form as in crystalline MOSFETs (charge-based in one

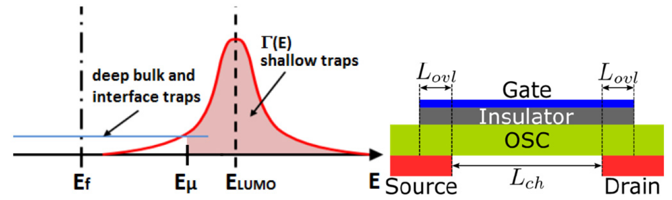


FIGURE 1. **(a) Simplified picture of shallow traps with Gaussian DOS Γ(E) and constant density of deep traps and interface states in an OSC. (b) Cross section of a staggered device.**

case, and linearized in the other case), but with a power-law effective mobility.

In this Section, voltages and currents are indicated in absolute voltages, so that we can use positive values for p-channel OTFTs.

A. CHARGE-BASED OTFT MODEL

The charge-based OTFT model [11] led to compact expressions of the drain current and total charges as functions of the channel charge densities at the drain and source ends of the channel. Quasi-free carriers with drift-diffusion transport were assumed. The effects of hopping transport is represented by using a power-law mobility model. Electrical parameters as threshold voltage and subthreshold slope are inherently included in the approach and directly related to physical parameters.

The effect of the source injection current was also studied and modeled in both staggered and coplanar OTFT structures by means of a 2D analysis using conformal mapping.

The model provides two views. In one view it preserves a close link to physical parameters in terms of trap densities by providing equations to calculate the threshold voltage and subthreshold slope of the device from these parameters. Furthermore, a second view of the model has been derived which is beneficial from a circuit designer's point of view.

A.1. PHYSICS-BASED MODEL PARAMETERS

The model is based on a simplified picture of the trap density in the organic semiconductor (OSC) as it is shown in Fig. 1 for the case of n-type material. The main current transport mechanism is via hopping between localized shallow trap states with a Gaussian DOS Γ(E). In subthreshold operation it is essential to include the bias dependent filling of deep bulk states and interface states, though they do not contribute to the device current. Filling of these states influences the electrostatics and therefore the accumulated charge density. This effect results in a degradation of the subthreshold swing with respect to the theoretical limit of 60 mV/dec at 300 K.

We approximate the accumulated charge density Q'_m in shallow traps per gate area in a channel of thickness d_m by filling the trap states above energy E_μ according to Boltzmann statistics:

$$Q'_m = qd_m \int_{E_\mu}^{\infty} \Gamma(E)f(E)dE$$

$$\approx qd_mN_{st}\exp\left(\frac{q(\phi_c - V) - E_g/2}{kT}\right) \tag{1}$$

Here N_{st} is a fitting parameter representing the equivalent shallow trap density, E_g the gap between HOMO and LUMO level, V is the voltage drop along the channel, and ϕ_c is the channel midgap potential in the accumulated channel. It should be noted that Eq. (1) is an approximation assuming the non-degenerate case, where the Fermi level is far from the center of the Gaussian DOS.

In [11], from solving Poisson's equation the following expression for the accumulated charge density has been derived using the first branch of Lambert's W function L_W:

$$Q'_{ms/d} = \frac{\alpha kT}{q}C_{ox}L_W\left\{\frac{Q'_{m0}}{C_{ox}\alpha kT/q}\cdot \exp\left(\frac{V_{GS/D} - V_{fb} - \frac{E_g}{2q} - \frac{qN'_{t,max}}{C_{ox}}}{\alpha kT/q}\right)\right\} \tag{2}$$

with the insulator capacitance per gate area C_{ox} and flatband voltage V_{fb}. Thereby parameter α describes the degradation of the subthreshold swing S with respect to the ideal thermal swing:

$$\alpha = 1 + \frac{q^2N'_t}{C_{ox}} = \frac{S}{\ln(10)\ kT/q}. \tag{3}$$

Here, charges in deep traps, i.e., in the tail states of the Gaussian DOS below energy E_μ, and interface states are represented in a simplified form by a constant density N'_t per gate area and per energy.

Parameter $N'_{t,max}$ in (2) is the density of deep trap and interface states which are filled if the channel potential is $\phi_c = E_g/(2q)$, which can be considered as threshold condition. Parameter Q'_{m0} is the charge in shallow traps at the same bias, and from (1) at $V = 0$ is given by:

$$Q'_{m0} = qd_mN_{st} \tag{4}$$

In the final current model charges in shallow traps are treated as quasi-free carriers with drift-diffusion transport, whereby the effect of hopping transport is considered by an effective field-effect mobility:

$$I_{DS} = \mu_{FET}W\left[\frac{kT}{q}\cdot\frac{Q'_{ms} - Q'_{md}}{L} + \frac{Q'^2_{ms} - Q'^2_{md}}{2LC_{ox}}\right] \times (1 + \lambda(V_{DS} - V_{DSx})) + \frac{V_{DS}}{R_{leak}} \tag{5}$$

$$\mu_{FET} = \frac{\kappa\left(\frac{Q'_{ms}}{C_{ox}}\right)^\gamma}{1 + \kappa\left(\frac{Q'_{ms}}{C_{ox}}\right)^\gamma \frac{W}{L}(R_c + R_sb)Q'_{ms}}. \tag{6}$$

We use an empirical power-law mobility model [17] with parameters κ and γ, incorporating a linear contact resistance R_c [18] and a non-linear contact resistance of a Schottky barrier R_{sb} by a first order approximation similar to [19]. Additionally, a leakage current is considered in (5) by resistance R_{leak}. Channel length modulation has been included by parameter λ and the expression:

$$V_{DSx} = \frac{1}{C_{ox}}\left(Q'_{ms} - Q'_{md}\right). \tag{7}$$

The introduction of parameter $Q'_{ms/d}$ from (2) in (5) to (7) ensures a one-piece expression for all regions of operation.

With (2) the final current equation preserves a close link to physical parameters like shallow and deep trap densities and avoids the introduction of a threshold voltage and subthreshold slope as purely electrical parameters.

B. ELECTRICAL MODEL PARAMETERS

Assuming $V_{ds} \approx 0$, in the on state of the device the density of quasi-mobile charges can be formulated by the definition of a threshold voltage V_{T0}:

$$Q'_{ms} = C_{ox}(V_{GS} - V_{T0}). \tag{8}$$

If this expression is equated to (2), for $V_{GS} >> V_{T0}$ an expression for the threshold voltage can be derived [11]:

$$V_{T0} = V_{fb} + \frac{E_g}{2q} + \frac{qN'_{t,max}}{C_{ox}} - \frac{\alpha kT}{q}\ln\left(\frac{Q'_{m0}}{C_{ox}\alpha kT/q}\right) \tag{9}$$

Combining this result with (2) the quasi-mobile charge densities at the source and drain end of the channel can be written as:

$$Q'_{ms/d} = \frac{\alpha kT}{q}C_{ox}L_W\left\{\exp\left(\frac{V_{GS/D} - V_{T0}}{\alpha kT/q}\right)\right\}. \tag{10}$$

Together with (5) to (7) a compact and one-piece expression for the device current is given which now provides a close link to electrical parameters as threshold voltage and subthreshold swing from a designer's perspective.

From this expression of the accumulated channel charge a closed-form model for the drain-current variability due to carrier-number and correlated mobility fluctuations has been derived, relating these statistical variations to the trap density in the channel. For detailed model equations please refer to [20].

C. SHORT CHANNEL EFFECTS

If the channel length is in the submicron regime, short channel effects like VT-roll-off, DIBL (drain-induced barrier lowering) and subthreshold swing degradation come to the fore. In [21] closed-form expressions for these effects have been derived by applying the conformal mapping technique:

$$\Delta V_{T,roll-off} = -V_{bi}f \tag{11}$$

$$\Delta V_{DIBL} = fV_{DS}/2 \tag{12}$$

V_{bi} is the built-in potential of the source/drain Schottky diodes

$$S_{sc} = \frac{kT}{q}\cdot\frac{\ln(10)}{1-f} \tag{13}$$

$$f = \frac{4(t_{sc} + t_{ox}\varepsilon_{sc}/\varepsilon_{ox})d_{poi}}{4(t_{sc} + t_{ox}\varepsilon_{sc}/\varepsilon_{ox})^2 + L^2}. \tag{14}$$

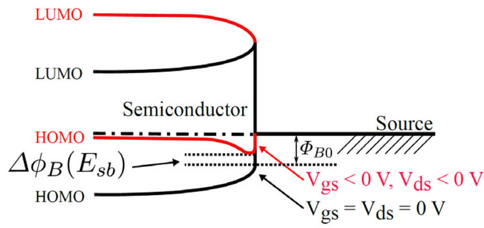


FIGURE 2. Band diagram of the SB at the source side for a p-type OSC. In case of an applied bias (red) the barrier height is lowered by $\Delta\phi_B$ depending on the electric field E_{sb} at the barrier [9].

Here, parameter d_{poi} is used as fitting parameter representing the distance of the most conductive path in subthreshold region from the gate-to-dielectric interface. Therefore, in case of (11) parameter f is calculated by with (14) for $d_{poi} \approx \varepsilon_{sc}/\varepsilon_{ox}\ t_{ox}$, and in case of (12) and (13) parameter f is computed with $d_{poi} \approx \varepsilon_{sc}/\varepsilon_{ox}\ t_{ox}+t_{sc}$, which in case of (11) is $d_{poi} \approx t_{ox}$ and in case of (12) and (13) $d_{poi} \approx t_{ox}+t_{sc}$.

These expressions for short-channel effects have been implemented into the core model by replacing in (10) the threshold voltage V_{T0} by

$$V_T = V_{T0} - \Delta V_{T,roll-off} - \Delta\ V_{DIBL} \tag{15}$$

and combining (3) with (13) for calculating the slope degradation from

$$\alpha = \frac{1}{1-f}\left(1 + \frac{q^2 N'_t}{C_{ox}}\right). \tag{16}$$

These extensions of the model have been shown to accurately predict the DC characteristics of staggered OTFTs with a channel length down to 0.5 µm.

D. AC MODEL

In [22] a charge-based capacitance model including fringing capacitances in multi-finger structures has been derived from the general charge expressions (2) or (10). The quasi-static AC model has been verified by measurements on a fabricated differential amplifier with DNTT-OTFTs on a flexible substrate and accurately models the magnitude and phase response of the circuit up to a frequency of 10 kHz.

A consideration of non-quasistatic effects has been incorporated into the same model [23] following a transmission line approach. In the circuit simulation netlist, the TFT is replaced by a macro model consisting of a finite number of n single transistors. In this way, the model captures charging and discharging of the channel capacitance of each segment by the adjacent transistors. Therefore, the frequency dependence of the node-to-node capacitances of the full device is obtained.

E. NON-LINEAR CONTACT RESISTANCE

Coplanar device structures as well as staggered devices with short overlap length may show a superlinear behavior in the output characteristics if the barrier height between source electrode and the channel material is not negligible [24]–[28]. In this case the channel current is limited by the source injection current. Carriers have to overcome the reverse biased Schottky barrier (SB) at the source end of the channel (Fig. 2). The SB height ϕ_{B0} is modulated by the gate and drain potential, influencing the electric field E_{sb} at the barrier. A strong electric field allows more carriers to enter the channel due to thinning of the barrier and the image charge effect, which lowers the barrier by an amount of

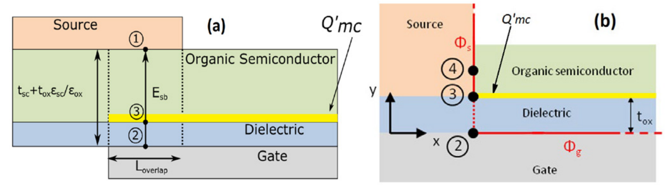


FIGURE 3. Model structure of the source region for (a) staggered and (b) coplanar device geometry.

$$\Delta\ \phi_B = \sqrt{\frac{qE_{sb}}{4\pi\,\varepsilon_{sc}}} \tag{17}$$

where ϵ_{sc} is the permittivity of the organic semiconductor [23].

For calculation of the electric field at the barrier, in case of a staggered device structure (Fig. 3a) the overlap region at source can be approximately treated as a one-dimensional problem and one can derive the following expression for the electric field at the barrier [26]:

$$E_{sb} = \frac{\phi_{B0} + \left(Q'_{ms} - Q'_{md}\right)/C_{ox}}{t_{sc} + t_{ox}\varepsilon_{sc}/\varepsilon_{ox}} \tag{18}$$

where t_{sc} is the thickness of the OSC in the overlap region.

Figure 3b depicts a coplanar device structure. At point 3, the bottom point of the injection region, a two-dimensional potential problem has to be solved. In [26], [27] a solution for the electric field at point 4, which is in a distance of d_B from the interface to the insulator, has been derived under use of the conformal mapping technique:

$$E_{sb} = \frac{2}{\pi} \cdot \frac{\phi_{B0} + \left(Q'_{ms} - Q'_{md}\right)/C_{ox}}{\sqrt{2d_B t_{ox}\varepsilon_{sc}/\varepsilon_{ox} + d_B^2}}. \tag{19}$$

In the model this solution is used as average electric field in the injection region, whereby d_B is used as fitting parameter.

In both cases, the accumulated charge Q'_{mc} at the source end of the channel (refer to Fig. 3) shields part of the gate potential from the barrier. In the operation region dominated by non-linear injection most of the voltage drops across the SB, therefore $V_c \approx V_{GS}$, and hence in the model we assume $Q'_{mc} = Q'_{md}$, which can be calculated from (2) or (10).

The injection current between source and the OSC can be calculated by the standard current equation of a reverse

biased SB with voltage drop V_c [29]:

$$I_{sb} = L_{inj} W A^* T^2 \cdot \exp\left(-\frac{\phi_{B0} - \Delta\phi_B}{\frac{\eta kT}{q}}\right)\left(exp\left(-\frac{V_c}{\frac{\theta kT}{q}}\right) - 1\right) \tag{20}$$

Parameter A^* is the effective Richardson constant and θ are ideality factors. For the case of staggered device structures parameter L_{inj} is the effective injection length in the source/drain-to-gate overlap region [18], [24]. For coplanar devices it is the thickness of the accumulation channel in the region of injection.

The effect of the SB is implemented into the current model via the effective mobility (6) as a non-linear resistance R_{sb} in series to R_c. In this way, in a circuit simulation an additional node for the calculation of the voltage drop across the SB is avoided. Using (20) the resistance can be derived to [26]:

$$R_{sb} \approx \frac{V_c}{I_{sb}} = \frac{\left(Q'_{ms} - Q'_{md}\right)}{t\ W\ A^* T^2\ C_{ox}} \cdot \exp\left(\frac{\phi_{B0} - \Delta\phi_B}{\frac{\eta kT}{q}}\right) \Big/ \left(exp\left(-\frac{V_c}{\frac{\theta kT}{q}}\right) - 1\right). \tag{21}$$

The voltage drop of $V_c \approx V_{DSx}$ is expressed by (7) in terms of the difference of the accumulation charges at the source and drain end of the channel, therefore ensuring a continuous formulation in all regions of operations. The non-ideality factor η has been introduced to allow for an improved fitting of the exponential current increase. The SB lowering $\Delta\phi_B$ is given by (17) together with (18) or (19). Additional effects arise from the forward biased SB at the drain contact. An extension of the model accounting for this effect is published in [27].

F. RESULTS

The model has been compared to measurements on DNTT OTFTs fabricated on a flexible PEN substrate with high-resolution silicon stencil mask lithography, aluminum gate electrode, gold source/drain contacts, AlOx/SAM gate dielectric with a thickness of 5.1nm, and a nominal thickness of the OSC of 25 nm [24], [27]. The effective charge carrier mobility is approximately 1.5 cm^2/Vs. The model has been verified for staggered and coplanar device geometry.

In Fig. 4 the charge-based DC model is compared to measurement data on staggered device structures. Since the compact model does not consider trapping-related hysteresis effects [30], their influence on the transfer characteristics of the transistors was accounted for by an empirical approach [8]. A good agreement is obtained without artificial smoothing in the transition from below to above threshold operation. Short channel effects as V_T-roll-off and DIBL are included. In the output characteristics the model accurately captures the pronounced superlinear region.

Figure 5a illustrates the model for drain-current variability due to carrier-number and correlated mobility fluctuations. The trap density in the channel has been used for fitting the model to the statistical data from the measurements.

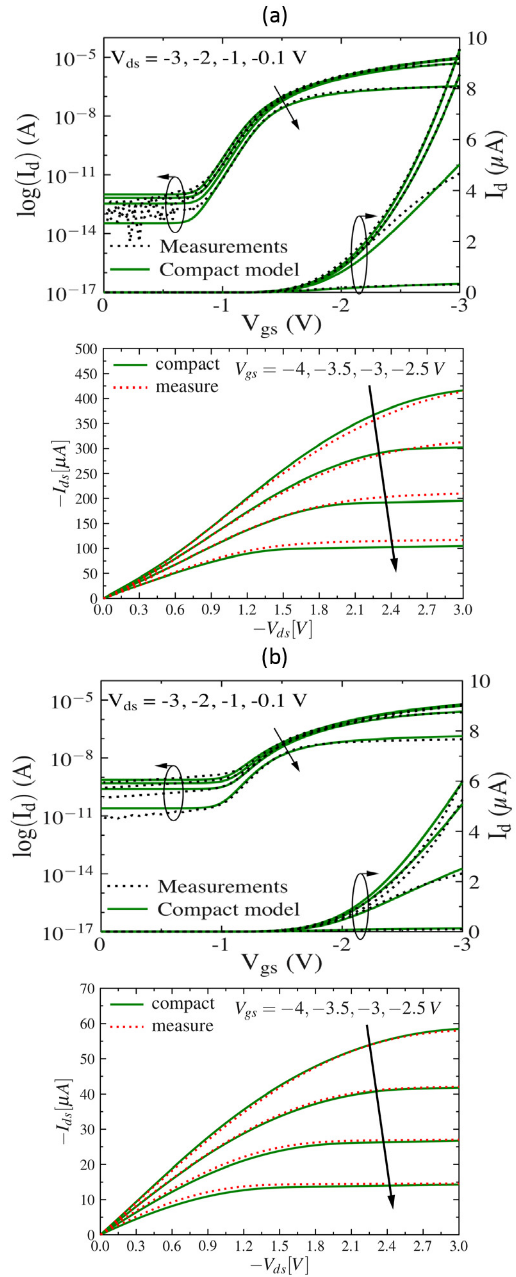


FIGURE 4. Results of the charge-based compact model compared to measurements on OTFTs with staggered structure. Transfer characteristics with a channel length of (a) 1 μm and (b) 0.5 μm. The current equation (5) has been extended by expressions for short-channel effects as DIBL and VT roll-off [21].

Figures 5b and c demonstrate the accuracy of the AC model compared to measurements.

III. UMEM-BASED OTFT MODEL

The UMEM-based OTFT model uses a similar formulation as in other TFT models, but adapted to the specificities of the OTFT [4].

A. DRAIN CURRENT MODEL

A single exponential DOS was assumed. Although a Gaussian DOS is a more accurate representation of a DOS

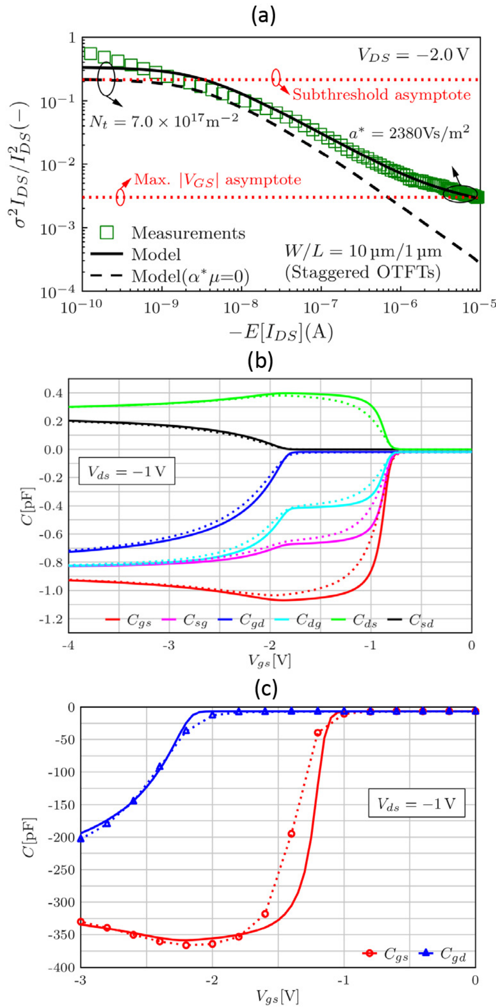


FIGURE 5. **(a) Normalized drain-current variance versus mean-value drain current of staggered organic TFTs with a channel length of 1 μm. The experimental mean values were calculated over a population of 16 nominally identical TFTs [20]. (b) and (c): Results of the charge-based capacitance model (full lines) for OTFTs with staggered structure compared to (a) TCAD Sentaurus simulations (dotted lines) at a frequency f = 0.01 Hz, and (b) measurements (dotted lines) at f = 500 Hz. Device dimensions: L = 200 μm, gate overlap at source/drain: 10 μm, width: (a) W = 1 μm, (b) W = 400 μm [22].**

in an OTFT (which could be also approximated by a two-exponential function [31]), it was demonstrated that an exponential DOS is accurate enough in the practical gate voltage range of operation. An analytical equation for the potential is obtained from Poisson's equation by neglecting free charge [32]. In the above threshold regime, by assuming variable range hopping as a transport mechanism [33], the OTFT drain current expression is derived as [34], [35]:

$$I_{DS} = \frac{-W\ C_{ox}\mu_0\left((V_{GTe} - V_{DSe})^{2+\gamma} - V_{GTe}^{2+\gamma}\right)(1 + \lambda V_{DSe})}{L\ V_{aa}^{\gamma}\ (2+\gamma)} \tag{22}$$

being W and L the channel width and length respectively, V_{DSe} and V_{GTe} are effective functions of the drain to source and gate overdrive voltages respectively, and C_{ox} is the insulator capacitance. μ_0 corresponds to the band mobility [33], The V_{aa} parameter depends on DOS parameters [33]. The effect of the contact resistance can be included as in other models such as [36] (in this case the current becomes an implicit function of the contact resistance), or alternatively, it can be externally incorporated (by means of external Schottky diodes if we consider a nonlinear contact [37]). The γ parameter depends on the DOS characteristic temperature (T_0) as:

$$\gamma = 2\frac{T_0}{T} - 2 \tag{23}$$

The UMEM-based model results from writing the drain current expression as in crystalline MOSFETs by using a field effect mobility expression. An equation of the drain current in the form of Eq (5) in Section II-A is obtained.

The field effect mobility is calculated as a power law [7], [8]:

$$\mu_{FET} = \mu_0 {V_{GT}}^{\gamma}/V_{aa}^{\gamma} \tag{24}$$

where $V_{GT} = V_{GS} - V_T$., being V_T the threshold voltage, which in OTFT can be written as in (15).

Finally, the resulting above threshold drain current expression is linearized around $V_{DS} = 0$ and an interpolation function is used to extend it in a continuous way to the saturation regime [4], [33]–[34].

$$I_{DS} = \frac{W}{L} \cdot C_{ox}\frac{\mu_{FET}(V_{GS} - V_T)}{\left(1 + R\frac{W}{L} \cdot C_{ox}\mu_{FET}(V_{GS} - V_T)\right)} \times \frac{V_{DS}(1 + \lambda \cdot V_{DS})}{\left[1 + \left[\frac{V_{DS}}{V_{DSsat}}\right]^m\right]^{\frac{1}{m}}} + I_o \tag{25}$$

The λ parameter is related to the slope of the output characteristics in saturation and m controls the transition from the linear to the saturation regime. The effect of R, the series resistance, was included up to the first order.

The saturation voltage is:

$$V_{DSsat} = \alpha_S(V_{GS} - V_T) \tag{26}$$

The effective drain-source voltage, which tends to V_{DS} for $V_{DS} << V_{DSsat}$ and to V_{DSsat} for $V_{DS} > V_{DSsat}$ can be therefore defined as:

$$V_{DSe} = \frac{V_{DS}}{\left[1 + (V_{DS}/\alpha V_{GT})^m\right]^{1/m}} \tag{27}$$

The drain current model in the subthreshold voltage is calculated, assuming diffusion transport, as:

$$I_{DSB} = I_{DS_0}e^{\frac{2.3(V_{GS} - V_T)}{S}} \tag{28}$$

where S gives the subthreshold swing and I_{ds0} gives the drain current as $V_{GS} = V_T$.

A unified model of the drain current, valid and continuous from subthreshold to the above threshold regime, is finally

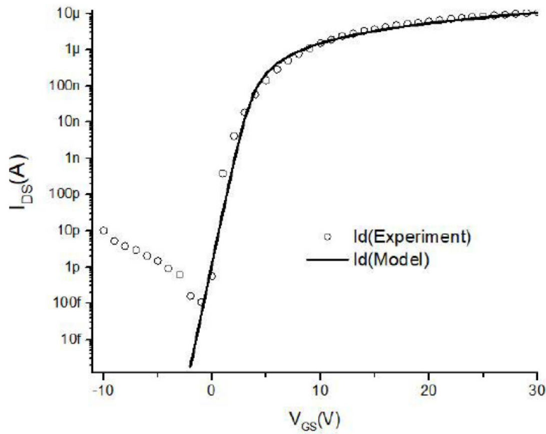


FIGURE 6. Model and experimental transfer characteristics. OTFTs from CEA-Liten with 13 fingers. *W* = 7980mm and *L* = 20mm. From [41]. The leakage current was not considered.

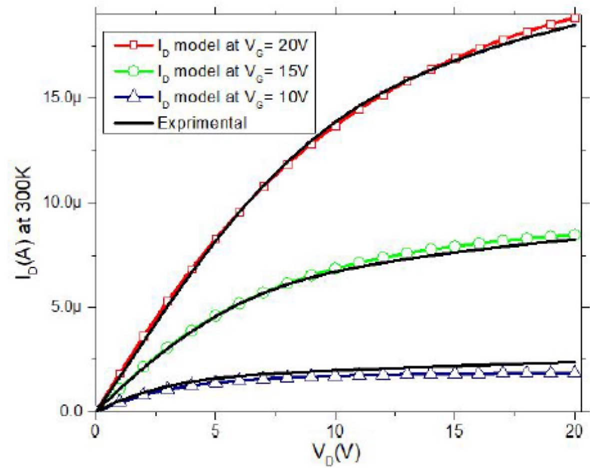


FIGURE 7. Model and experimental transfer characteristics. OTFTs from CEA-Liten. *W* = 2000mm and *L* = 20mm. From [42].

obtained by means of hyperbolic functions:

$$I_{DS} = \left(I_{DSA} \frac{1 + \tanh(V_{GS} - (V_T + DV)Q)}{2} \right) + \left((I_{DSB} + 0) \frac{1 + \tanh(V_{GS} - (V_T + DV)Q)}{2} \right. \quad (29)$$

where I_{DSA} is the above threshold current, given by (25), DV and Q are fitting parameters.

The UMEM-based model for OTFTs [4], was improved in order to include a physics-based gate-bias dependence expression of the contact resistance, valid in staggered OTFTs [38], [39]:

$$R_C = R_{C0} \frac{A/W}{V_{GTeff}{}^{\gamma+1}} \quad (30)$$

where R_{C0} is the nongateable R_C due to the injection at the contact, *A* is the proportionality constant due to the bulk and channel transport, and $V_{GTeff} = V_{GS} - V_T - V_{DS}/2$ [40].

This model takes into account the 2-D current path of a staggered transistor, using a modified current crowding model featured by a constant access resistivity *r*acc and power-law dependent bulk and channel resistivities (*rB* and *r*ch*)*. According to TCAD simulation results (using a Gaussian DOS). the gate voltage dependence of *rB* and *r*ch arise from the hopping transport through a Gaussian DOS of the disordered organic semiconductor.

To extract the key physical parameters in the above threshold regime, we apply the integral function $H(V_{GS})$ described by [4], [33], [41] to the I-V_{GS} characteristics at low V_{DS}, and use linear regression to extract parameters

$$H(V_{GS}) = \frac{\int_0^{V_{GS}} I_{DS}(x)dx}{I_{DS}(V_{GS})} = \frac{1}{2+\gamma}(V_{GS} - V_T) \quad (31)$$

V_T and γ are the intercept and the slope of (31) respectively.

The rest of extraction procedures are described in [4], [33], [42]–[44].

Alternatively, the so-called ratio method, can be applied [39] to get V_T and γ.

This drain current model was validated by comparison with experimental transfer and output characterizes from polymeric OTFTs fabricated by several technologies, including CEA-Liten (Grenoble, France), where relative permittivity of the dielectric is approximately 2, and the thickness is 700 *nm*; the semiconductor thickness is 40 nm with a relative permittivity close to four. Good agreement was observed in all operation regimes (Figs. 6–7).

B. CHARGE AND CAPACITANCE MODELS

On the other hand, a quasi-static model for total charges in OTFTs was developed to provide continuous expressions of the device capacitances from depletion to strong accumulation [34], [41]. This is an advantage over previous models, which are only valid in the strong accumulation regime [46], [47]. The development of this charge model followed the same procedure as in Section II-A.

The total gate charge is equal to the channel charge in absolute value. We use the expression derived from the integration of the channel charge density in accumulation [34], [41]. The expression of the drain current was not linearized (22).

$$Q_{CH} = \frac{-W\ C_{ox}^2}{I_{DS}} \mu_{FET0} \frac{(V_{GTe} - V_{DSe})^{3+\gamma} - V_{GTe}^{3+\gamma})}{3+\gamma} \quad (32)$$

μ_{FET0} is the value of mobility/V_{aa}^{γ} when $V_{GS} - V_T = 1$V: $\mu_{FET0} = \frac{\mu_0}{V_{aa}^{\gamma}}$.

We used an interpolation function for the effective gate overdrive voltage V_{GTe} in order to extend to the subthreshold regime the above threshold drain current model expression in a continuous and smooth way [41].

By differentiating (32) respect to V_{GS}, we obtain the expression of the gate to gate capacitance in accumulation.

The final capacitance model is obtained using an interpolation function which smoothly tends to $C_{GGa} = C_{GG} + 2C_{OVR}$, where C_{GG} is the gate-gate capacitance obtained by

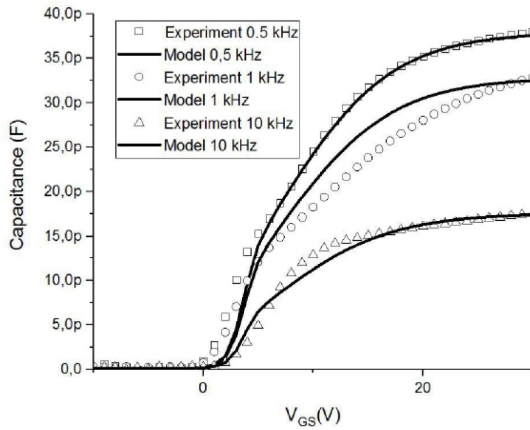


FIGURE 8. Modeled and experimental capacitances. Organic MIS capacitors from CEA-Liten. From [18].

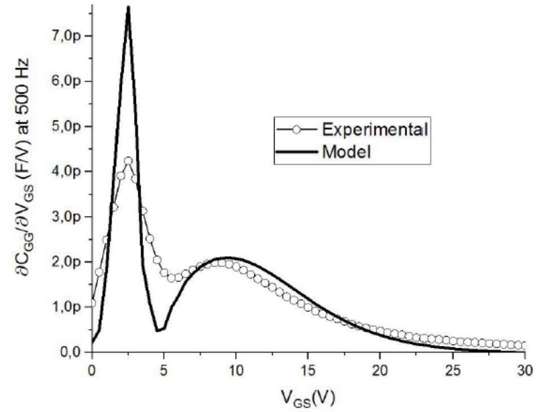


FIGURE 9. First derivative of the gate capacitance. Organic MIS capacitors from CEA-Liten. From [18].

differentiating (32) with respect to the gate voltage in accumulation, and the overlap capacitance is $C_{OVR} = L_{OVR}\ C_i\ W$, L_{OVR} being the overlapping length between gate and drain contacts and between gate and source contacts [41], [45]. In the subthreshold regime it tends to a C_{EQ} value, which takes into account the depletion capacitance [41].

$$C_{TOT} = \left(\left|C_{EQ}\right|\frac{1-\tanh(\beta)}{2}\right) + \left(\left|C_{GG}\right|\frac{1+\tanh(\beta)}{2}\right) \quad (33)$$

where $\beta = (V_{GT} + \Delta\ V_T)Q_2$ is a correction of V_T for capacitance in *C-V* measurements. Q_2 is a fitting parameter in the knee region.

At medium and high frequencies, the quasi-static approximation cannot be applied, and several physical phenomena determine OTFT operation [48], [49]. The capacitance model described in this section was extended to non quasi-static conditions using a frequency-dependent dielectric permittivity

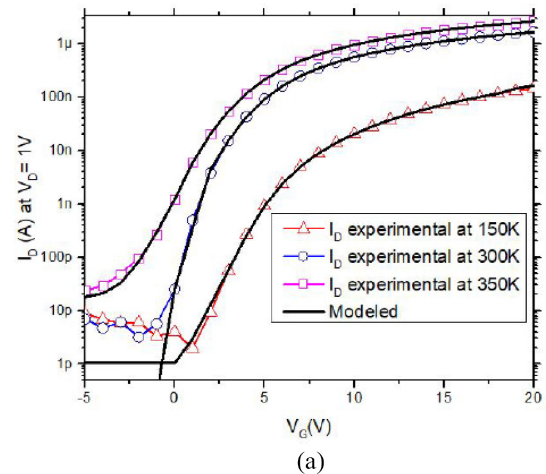
$$\varepsilon_i = \varepsilon_{i\infty} + \frac{(\varepsilon_{i0} - \varepsilon_{i\infty})}{\left[1 + j\omega\tau\right]^p} \quad (34)$$

This capacitance model was validated by comparison of measurements of organic MIS capacitors fabricated by CEA (France).

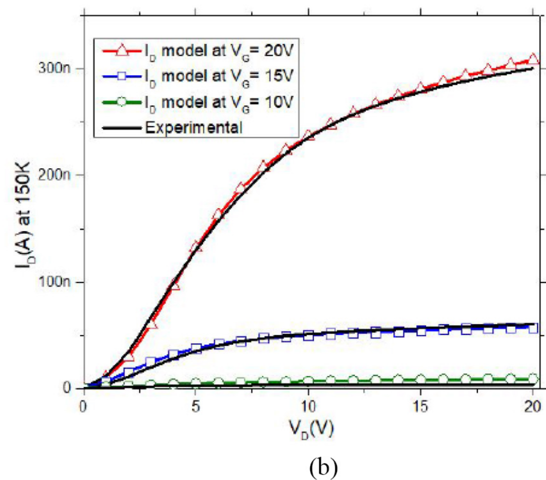
Very good agreement (up to 10 KHz) was observed (Fig. 8), not only for the capacitance, but also for its first-order derivative [18] (Fig. 9). Besides, we found that our model reproduced well the observed two peaks of the first-order capacitance derivative, the first one corresponding to the onset of partial depletion, and the second one to the onset of accumulation (Fig. 9).

C. TEMPERATURE EFFECTS

Very little work has been done so far in the modeling of OTFT at low and high temperatures, and only a few parameters were addressed [50]–[53]. The UMEM OTFT model was also adapted to different temperatures, from 150 K to 340 K. Measurements were done at both low and high temperature conditions. Model parameters were extracted for each temperature. The model was demonstrated to be valid



(a)



(b)

FIGURE 10. (a). Modeled and experimental transfer characteristics at different temperatures. OTFTs from CEA-Liten. From [42]. (b). Modeled and experimental output characteristics at 150K. OTFTs from CEA-Liten. From [42].

in the range of temperatures from 150 K to 350 K [42]. Fig. 10(a) shows the transfer characteristics at 150, 300 and 350K. Fig. 10(b) shows the output characteristics at 200K [42]. In all these cases, very good agreement is observed between modeled and experimental results.

At low temperatures the model must include the effects of the nonlinear contact resistance. It was carried out by considering Schottky diode at the contact. The procedure explained Section II-A can also be applied [42].

Furthermore, capacitance-voltage measurements of OTFT capacitors were done in the temperature range from 150 K to 350 K, and our capacitance model was demonstrated to accurately reproduce the measurements in this temperature range, up to a frequency of 10 KHz.

IV. AOS TFT MODELING

Two approaches were used to develop a compact model for AOS TFTs: one based on two exponential DOS and a transport mechanism based on the combination of trap-limited conduction (TLC) and percolation, and another one based on a UMEM formulation with two exponential DOS and a transport mechanism based on the combination of hopping and drift diffusion (which actually means trap-limited conduction). Both approaches lead to the same type of drain current expressions and finally physically based expressions were found for the mobility parameters of the UMEM-based model.

A. TLC/PERCOLATION BASED MODEL

The above threshold model is based on a mobility model that combines trap-limited conduction (TLC) with percolation conduction [54]. An exponential DOS is assumed. On the other hand, the resulting subthreshold model takes into account diffusion and drift current components [55]. A power-law expression was used for the drift component(in terms of the gate voltage overdrive) and an exponential expression was used for the diffusion component.

A small-signal model was developed by means of an equivalent circuit [56].

Compared with a-Si TFTs, the oxide system has unique properties, which need to be captured. For example, localized traps or band tail states in oxides do not exist to the same extent as a-Si [57]. Their tail state density is much lower and hence trap-limited conduction is generally insignificant [57], [58]. In addition, more complex systems such as amorphous indium gallium zinc oxide (a-IGZO) can have compositional disorder due to random distribution of metal constituents [57], [58] This gives rise to potential barriers above the conduction band minima (E_m), suggesting the presence of percolation conduction [57]–[63].

In the following, compact models for the terminal current-voltage behavior are presented taking into account the different transport mechanisms in the device for the above- and sub-threshold regimes of TFT operation. The former is based on a mobility model that combines trap-limited conduction (TLC) with percolation conduction. The latter takes into account diffusion and drift current components [64]. A unified model is then presented that covers both regimes based on a single expression that uses a reference voltage V_{FB} rather than V_T [65], [66]. Good agreement with measured terminal characteristics is obtained over the entire range of $V_{GS} > V_{FB}$ for the test TFTs with an a-IGZO channel.

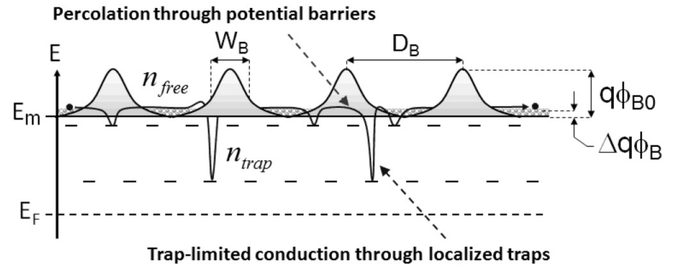


FIGURE 11. Illustration of carrier transport combining percolation with trap-limited conduction (TLC) for oxide semiconductor TFTs (Here, D_B and W_B denote spatial distance and width of potential barriers, respectively).

B. ABOVE-THRESHOLD MODEL

As illustrated in Fig. 11, oxide TFTs have potential barriers above E_m due to compositional disorder, suggesting percolation conduction when electrons are released into the conduction band. Moreover, there are localized tail states within the gap states, implying trap-limited conduction. In particular, oxide semiconductors can have a shallow slope of the tail states (kT_t) ~ 20meV, smaller than the thermal energy (kT) at 300K, leading to different mobility behavior. This suggests that the field effect mobility (μ_{FE}) model needs to be modeled based on TLC and percolation conduction, although the former is significant as compared to a-Si.

B.1. TRAP-LIMITED CONDUCTION (TLC)

The effect of trap-limited conduction (TLC) can be considered as ratio (γ_{TLC}) of free carrier density (n_{free}) and trapped carrier density (n_{tail}), yielding $\gamma_{TLC} = n_{free}/(n_{free}+n_{tail})$. Here, $n_{free} = N_C \exp[(E_F-E_m)/kT]$, where N_C is effective density of free carriers and kT the thermal energy. And the expression for n_{tail} is approximated with $kT_t <$ kT using exponential distribution of tail states. This yields $n_{tail} = N_{tc}\, kT_{vt} \exp[(E_F-E_m)/kT]$. Now, we have γ_{TLC} as just a constant,

$$\gamma_{TLC} \equiv \frac{n_{free}}{n_{free}+n_{tail}} \approx \frac{N_C}{N_C+N_{tc}kT_t}. \tag{35}$$

B.2. PERCOLATION CONDUCTION

Percolation conduction associated with potential barriers above E_m can be considered as mobility scaled from band mobility (μ_0), assuming Gaussian random distribution of potential barriers with mean (ϕ_{B0}) and variance (σ_{B0}). This yields $\mu_0{}^* = \mu_0 \exp[-q\phi_{B0}/kT+(q\sigma_{B0})^2/(kT)^2]$. Here, ϕ_{B0} can be reduced by $\Delta\phi_{B0}$ due to thermally released

electrons, depending on Fermi level change (ΔE_F), as described in Fig. 11. The thermally reduced barrier height can be expressed as $\phi_{B0}\cdot\exp(-\gamma_B\Delta E_F/kT)$, where $\gamma_B \equiv (D_B - W_B)/D_B$, which can be approximated as $\phi_{B0}(1-\gamma_B\Delta E_F/kT)$ when $\gamma_B\Delta E_F/kT << 1$ by Taylor expansion. Thus, $\Delta\phi_{B0}$ is defined as $\gamma_B\Delta E_F/kT\phi_{B0}$. These conditions yield the percolation mobility (μ_{Per}) as follows,

$$\mu_{Per} \equiv \mu_0 \exp\left(-\frac{q(\phi_{B0} - \Delta\phi_B)}{kT} + \frac{(q\sigma_{B0})^2}{2(kT)^2}\right), \\ = \mu_0^* \exp\left(\frac{\gamma_B\Delta E_F}{kT}\phi_{B0}\right) \quad (36)$$

where $\mu_0^* = \mu_0 \exp[-q\phi_{B0}/kT + (q\sigma_{B0})^2/2(kT)^2]$ considered as an effective band mobility.

B.3. COMBINED MOBILITY MODEL WITH V_{GS} DEPENDENCE

In Eq.(36), the ΔE_F is controlled by gate voltage (V_{GS}). The relationship between them can be derived by solving Poisson's equation, yielding $\Delta E_F = 2(kT/q)\ln[C_{ox}(V_{GS}-V_T)/Q_{ref}]$, where C_{ox} is gate-insulator capacitance, V_T threshold voltage which can be extracted independently using second derivative method reported in [54]–[56], and $Q_{ref} \equiv [2\epsilon_S N_C kT\exp[(E_{F0}-E_m)/kT]^{0.5}$.

Combining TLC with percolation from Eqs. (1) to (36), we now have the V_{GS} dependent mobility relation,

$$\mu_{FE} \equiv \mu_{Per}\gamma_{TLC} \\ = \mu_0^*\left(\frac{N_C}{N_C + N_{tc}kT_t}\right)\left(\frac{C_{ox}}{Q_{ref}}\right)^{\alpha_p}(V_{GS} - V_T)^{\alpha_p}. \quad (37)$$

As can be seen, Eq.(37) follows a power law. Here, $\alpha_p \equiv 2q\phi_{B0}\cdot\gamma_B/kT$, related to percolation. In Eq. (37), TLC affects the constant term, while the exponent is determined by percolation.

B.4. CURRENT-VOLTAGE RELATION

With Eq. (37) and the definition of drift current: $I_{DS} = \mu_{FE} C_{ox}(V_{GS}-V_T-V_{ch})dV_{ch}/dx$, current-voltage relation $I_{DS}(V_{GS})$ can be derived with the integral ranges: x = 0 to L and channel potential (V_{ch}) = 0 to V_{DS},

$$I_{DS} \equiv \mu_0^*\left(\frac{N_C}{N_C + N_{tc}kT_t}\right)\frac{W}{L'}\frac{C_{ox}^{\alpha_p+1}}{Q_{ref}^{\alpha_p}}(V_{GS} - V_T)^{\alpha_p+1}V'_{DS}. \quad (38)$$

In Eq. (38), L' is defined as $L-\Delta L$, where ΔL is channel expansion, and effective drain voltage $V'_{DS} = V_{DS} - 2R_C I_{DS}$, where R_C is contact resistance. For saturation regime expression, Eq. (38) can be reformed with a saturation parameter (β_{sat}), replacing V'_{DS} by $\beta_{sat}(V_{GS}-V_T)$. Fig. 12(a) shows a comparison between measured and modeled transfer characteristics (I_{DS} vs. V_{GS}) of IGZO TFTs at $V_{DS} = 0.1$V, providing a good agreement. The measured saturation characteristics at $V_{DS} = 20$V is also well matched with the modeled results, as seen in Fig. 12(b).

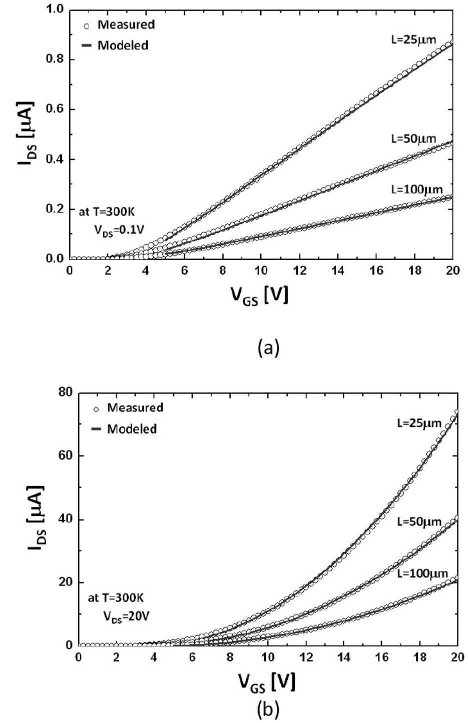


FIGURE 12. Comparison between measured and modeled transfer characteristics of IGZO TFTs. (a) linear regime with $V_{DS} = 0.1$V and (b) saturation regime with $V_{DS} = 20$V.

The examined IGZO TFT to verify this model in Fig. 12 and the other figures in this section has the following geometrical and physical parameters : W = 100μm, channel thickness t_S = 40nm, channel permittivity $\epsilon_S = 11.5\epsilon_0$ (where ϵ_0 is vacuum permittivity), $V_{FB} \sim 0.6V$, $V_T \sim 4$V, C_{ox} = 11.5 nF/cm^2, μ_0 = 15 cm^2/V-s, and $N_C = 5\text{x}10^{18}$ cm^{-3} at 300K. We extracted, $2R_C \equiv R_{SD} = 9637\Omega$ for W = 100 μm (equivalent to R_{SD} W = 96.37 Ω−cm) and $\Delta L = -3.5\mu$m (L' = L−Δ L = L+3.5μm).

We measured and simulated the drain current as a function of gate bias for different temperatures, e.g., 100K, 200K, and 300K, respectively. As seen in Fig. 13(a), there is good agreement between the measurements and the model, Eq. (38). For purposes of validation, the modeled values of exponent (α_p) in the power-law, Eq. (38), are compared with the extracted values from the best fit since it has a unique signature of percolation conduction, i.e., $a = \alpha_p + 1 \equiv 2q\phi_{B0}\cdot\gamma_B/kT + 1$). As seen in Fig. 13(b), the proposed percolation model for $\phi_{B0}\cdot\gamma_B$ = 2.5meV shows better agreement compared to the conventional model (e.g., trap-limited conduction model with $a = 2kT_t/kT-1$ for kT_t = 30 meV).

C. SUBTHRESHOLD MODEL

The subthreshold current in the limit of low V_{GS} shows a linear dependence on V_{GS} in a semi-log plot, as illustrated in Fig. 4, suggesting diffusion current, as follows,

$$I_{Diff} \approx \mu_0\frac{kT}{q}\frac{W}{L'}Q_{fi}\exp\left(\frac{q}{kT}\left(\frac{V_{GS} - V_{FB}}{1 + q^2D_{it}/C_{ox}}\right)\right)$$

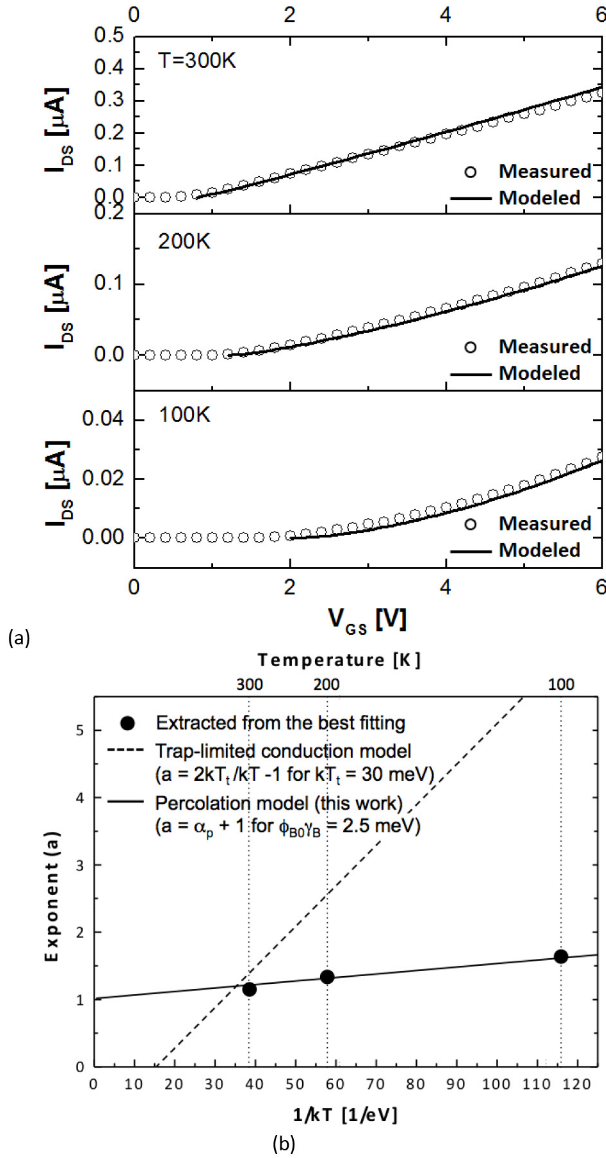


FIGURE 13. (a) Measured and modeled IGZO TFT $I_{DS}-V_{GS}$ characteristics for above-threshold regime at $V_{DS} = 0.1V$ for different temperatures (100K, 200K, 300K, respectively). (b) Retrieved exponent (a) vs. temperature.

$$\times \left(1 - \exp\left(-\frac{qV'_{DS}}{kT}\right)\right), \tag{39}$$

where μ_0 is the band mobility for electrons. The sub-threshold slope (S) can be derived from Eq. (39) as $dV_{GS}/d\log I_{DS}$,

$$S = ln1\ 0\frac{kT}{q}\left(1 + \frac{q^2 D_{it}}{C_{ox}}\right). \tag{40}$$

As described in Fig. 14, interface states are occupied first, followed by filling deep states located in the bulk at higher V_{GS}. So, As the E_F moves to the location of deep states for increasing V_{GS}, the drain current can be defined as a drift

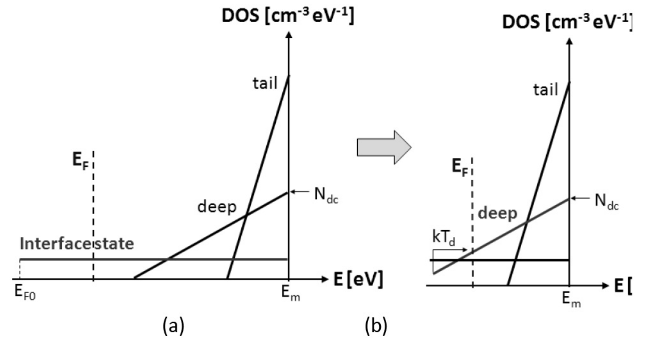


FIGURE 14. Density of states profile with (a) Fermi level within interface states at low gate voltage, and (b) the case of deep states dominant with increasing gate voltage corresponding Fermi level now within deep states.

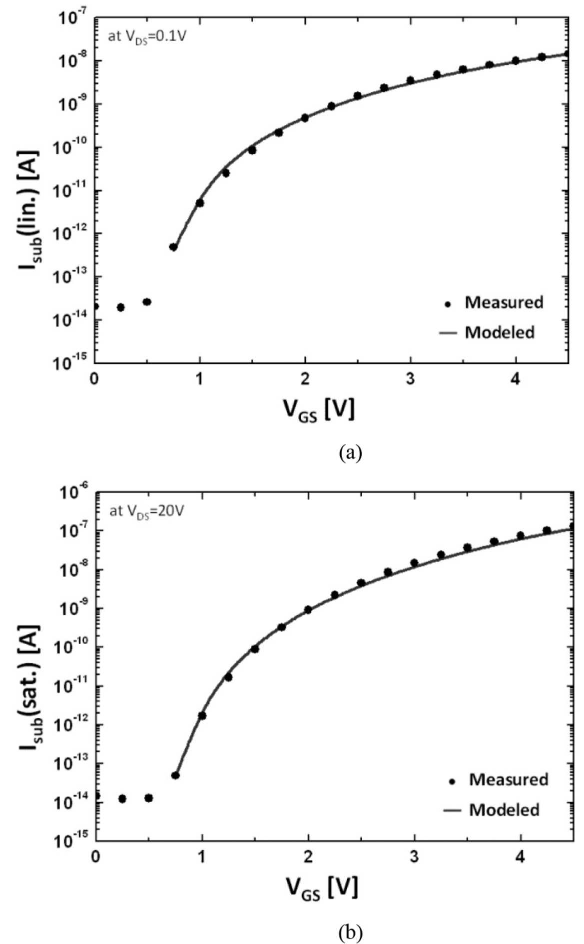


FIGURE 15. Measured and modeled IGZO TFT sub-threshold current (I_{sub}) as a function of V_{GS} for (a) linear regime with $V_{DS} = 0.1V$ and (b) saturation regime with $V_{DS} = 20V$.

current (I_{Drift}),

$$I_{Drift} \approx \mu_0 \frac{W}{L'} \frac{C_{ox}^{\alpha_d+1}}{Q_d^{\alpha_d}} (V_{GS} - V_{FB})^{(\gamma+1)} V'_{DS}, \tag{41}$$

where Q_d is a reference charge density associated with deep states, γ is power-law exponent defined as $2(T_d/T-1)$, and T_d is the characteristic temperature of deep states.

TABLE 1. Extracted subthreshold parameters at T = 300K.

Parameters	Value
S	0.19 V/dec
D_{it}	1.64×10^{11} cm^{-2}eV^{-1}
I_{off}	2×10^{-14} A
Q_{fi}	7.05×10^{-14} C/cm^2
α_d	2.26
T_d	639K
Q_d	7.8×10^{-8} C/cm^2

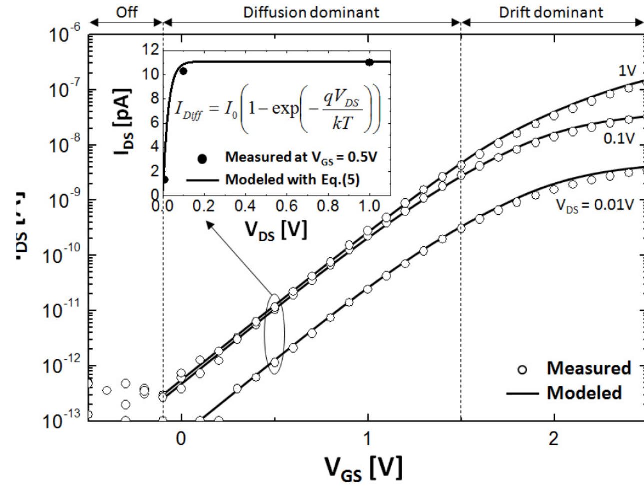


FIGURE 16. **Measured and modeled IGZO TFT I_{DS} vs. V_{GS} at sub-threshold regime for a different V_{DS}. Inset: Measured and modeled I_{DS} vs. V_{DS} for V_{GS} = 0.5V. Here, the equation is simplified from Eq. (5) introducing the pre-constant I_0 which is around 10pA at V_{GS} = 0.5V.**

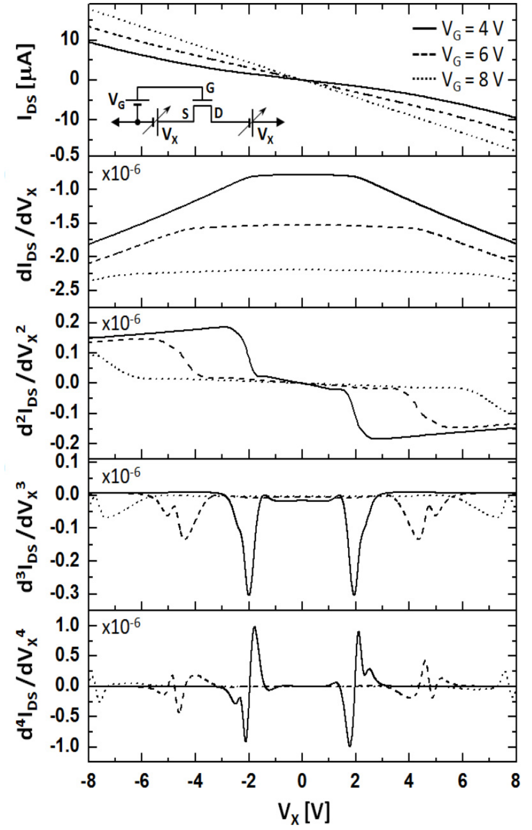


FIGURE 17. **(a) Calculated I_{DS} vs. V_X of the combined above- and sub-threshold model for different V_G (4, 6, 8V). (b) First, (c) second, (d) third, and (e) fourth derivatives of I_{DS} with respect to V_X. The inset of (a): test circuit configuration of the GST.**

We now have the current-voltage relations for both diffusion and drift components as given by Eqs. (40) & (41). These equations can be combined as a total drain current (I_{sub}) in the sub-threshold regime using a harmonic average,

$$I_{sub} \equiv \left(I_{Diff}^{-m} + I_{Drift}^{-m}\right)^{-1/m}, \tag{42}$$

The examined IGZO TFT to verify this model in Figs. 15–16 has the parameters indicated above in Section III-A1, with L = 100μm. The extracted sub-thresholdmodel parameters are summarized in Table 1. Fig. 15 shows the measured sub-threshold characteristics for a different V_{DS}, providing a good agreement with each other.

To validate the sub-threshold model in terms of the diffusion component in the examined transistors, we measured the drain current for small V_{DS} = 0.01, 0.1, and 1V. Comparing to the model, we get good agreement as seen in Fig. 16. In particular, as shown in the inset of Fig. 16, the measured I_{DS} vs. V_{DS} at the diffusion dominant regime of V_{GS} (e.g., V_{GS} = 0.5V) is compared with the Eq. (39). Here, the dependence of the drain current on V_{DS} is found to follow the law of $(1-\exp(-qV_{DS}/kT))$ of Eq.(39) which is a signature of the presence of the diffusion current.

To validate the sub-threshold model in terms of the diffusion component in the examined transistors, we measured the drain current for small V_{DS} = 0.01, 0.1, and 1V. Comparing to the model, we get good agreement as seen in Fig. 16. In particular, as shown in the inset of Fig. 16, the measured I_{DS} vs. V_{DS} at the diffusion dominant regime of V_{GS} (e.g., V_{GS} = 0.5V) is compared with the Eq. (39). Here, the dependence of the drain current on V_{DS} is found to follow the law of $(1-\exp(-qV_{DS}/kT))$ of Eq. (39) which is a signature of the presence of the diffusion current.

Regarding continuity and symmetry of the compact model where above- and sub-threshold models are combined, the model was subject to the Gummel symmetry test (GST) [67]. As seen in the inset of Fig. 17(a), V_X represents a symmetrical voltage applied on source and drain sides, respectively. Fig. 17 demonstrates perfect continuity and symmetry as a function of V_X even for the 4th derivative of I_{DS} with respect to V_X, suggesting it has successfully passed the GST. For this, we employed smoothness and continuity functions for the effective drain voltage and threshold voltage terms [68].

D. UNIFIED MODEL

The current-voltage relation needs to be derived separately to describe the sub-threshold and above-threshold characteristics. Here, we need separate expressions for the sub-threshold and above-threshold regimes, implying two

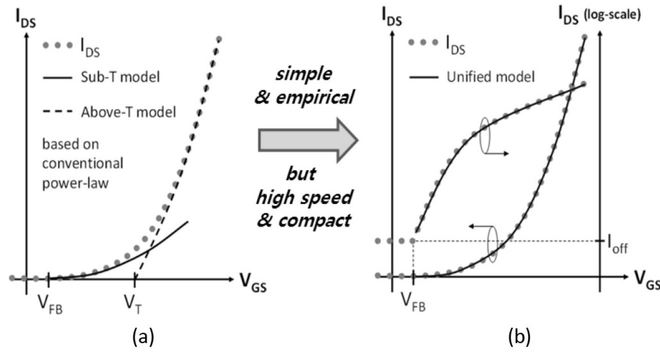


FIGURE 18. (a) Schematic I_{DS} vs. V_{GS} curves (gray circles) with the conventional power-law models for sub-threshold (Sub-T, solid line) and above-threshold (Above-T, dot line) characteristics. In this case, we need two models for these two different operational regimes. Here, V_{FB} and V_T are on-voltage and threshold voltage, respectively. (b) Schematic I_{DS}-V_{GS} curves (gray circles) with only one model: unified model which can cover sub-threshold as well as above-threshold regimes at the same time.

TABLE 2. Extracted parameters for unified model at T=300K.

Parameters	Value
G_0	2.34x10^{-5}ohm^{-1}
κ	-10.812 V$^{-\alpha}$
α	-0.675

different equation systems to describe total current (see Fig. 18a). Moreover, in this case, threshold voltage (V_T) is not immediately apparent from the I-V plot and needs to be extracted from above-threshold region of the characteristic as a fitting parameter. However, the extracted value of V_T can be quite different depending on extraction method and the I-V data range chosen for the fit. In contrast, turn-on-voltage (V_{FB}) is the gate voltage (V_{GS}) at which drain current (I_{DS}) starts increasing rapidly, thus it is easy to identify V_{FB} on a semi-log plot of I_{DS} vs. V_{GS}.

We can unify this to cover both sub-threshold and above-threshold characteristics. The proposed unified model is a single expression with a reference voltage level V_{FB} rather than V_T, providing good agreement with measured terminal characteristics over the entire range of $V_{GS} > V_{FB}$ for the test TFTs with an amorphous InGaZnO (a-IGZO) channel, which is the same TFT used in the previous sections. The derived equation for this model is as follows,

$$I_{DS} = G_0\left(\frac{W}{L'}\right)\exp\left(\kappa(V_{GS} - V_{FB})^{\alpha}\right)V'_{DS} + I_{off}, \quad (43)$$

where $G_0 = \mu_0(\epsilon_S\ kTN_C)^{1/2}$, $\kappa = \zeta/2kT$, and ζ & α are related to trap states. The extracted model parameters are summarized in Table 2.

As shown in Fig. 18(b), the unified model provides good agreements with the measured characteristics. Also, it was found to exhibit small average errors < 5% over a wide range of V_{GS} from 5 to 20V. Interestingly, the proposed model using only one equation covers both the sub- and above-threshold regimes at the same time. This is mainly due to a combination of the exponential function and power-law. Additional advantage of this unified model is that it just needs a few model parameters to be implemented in model code description, e.g., Veriog-A, thus providing a higher-speed simulation.

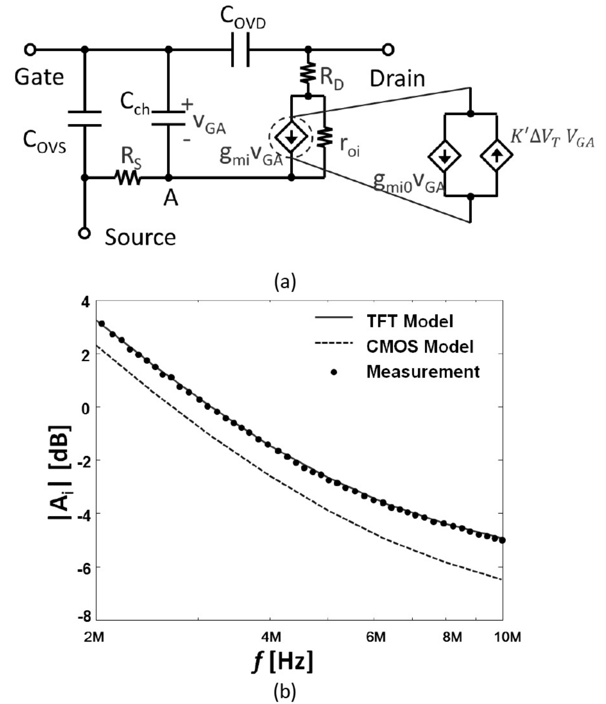


FIGURE 19. (a) Small signal model for IGZO TFT. V_{GA} is the voltage difference between gate and the node 'A', where $V_{GA} = V_{GS} - I_{DS}R_S$ (b) Short-circuit current gain (A_i) for the TFT with channel width (W) = 100μm and channel length (L) = 10μm, which is converted from the S-parameter measurement.

E. SMALL SIGNAL MODEL

The small signal model for IGZO TFT is illustrated in Fig. 19(a) which takes into account the contact resistance (R_S and R_D), parasitic capacitance (C_{OVS} and C_{OVD}), channel capacitance (C_{ch}) and threshold voltage shift ($\Delta\ V_T$) [69], while introducing internal transconductance (g_{mi}) and output resistance (r_{oi}) [56]. The model yields a 1% error in predicting the unity gain frequency, in contrast to 12.5% error using the CMOS model as shown in Fig. 19(b).

Theoretical analysis suggests that accuracy improvement stems from C_{ch} & R_C connection in the TFT model which further improves the fitting of the TFT's s-parameters leading to a better accuracy in predicting the unity gain frequency. The measurement results and modeled values are shown in Fig. 20.

F. UMEM-BASED MODEL

The second modeling approach for AOS TFTs considers initially two exponential DOS [72]–[74]. One of the exponential terms accounts for the deep states and the other one for the acceptor states [75]–[78], as in a-Si:H TFTs [79]–[81]. In

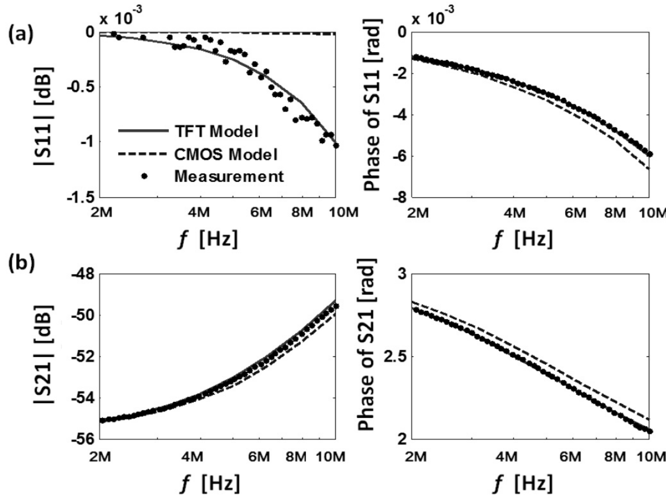


FIGURE 20. (a) Amplitude and phase plots for S_{11} and (b) those of S_{21}, respectively.

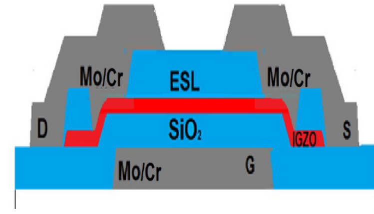


FIGURE 21. Cross section of the IGZO TFT under study, fabricated at TNO.

both regimes the transport is assumed to be due to a combination of drift and hopping between localized states. The resulting expressions of the drain current are power law functions of the gate voltage overdrive. In the deep subthreshold regime diffusion transport is assumed to be the dominant mechanism. A unified expression of the drain current was developed by combining those components by means of an interpolation function.

G. DRAIN CURRENT MODEL

It was found that in mature technologies such as targeted IGZO TFT devices from TNO had a negligible deep density of states, so that they could be modeled assuming only tail states and therefore only one exponential DOS [34].

The modeling in the above threshold regime is carried out in a similar way as in Section III-A, and has actually a UMEM-based formulation, but initially neglecting the percolation effects. In the above threshold regime, the Fermi level is assumed to be in the tail states but below the conduction band if the gate voltage or the temperature are not high enough and therefore, percolation can be neglected). Besides, this model considers that in the above threshold regime the dominant conduction mechanism is multiple trapping and release, combined band conduction. In the subthreshold regime, the model assumes that diffusion transport dominates. Both free and trapped charges are considered.

Several previous physically-based AOS TFT models have a surface-potential formulation, and the drain current is written as a symmetric function of the surface potentials at the source and drain ends of the channel, which in turn, depend on the source and drain potentials [70]. These potentials can be explicitly written in terms of the applied voltages [71]. The UMEM model is based on linearizing the drain current expression at $V_{DS} = 0$, and use an interpolation function to control the transition from the linear regime to saturation. This allows simple direct methods to extract parameters. The drain current model above threshold voltage (V_T) is given by:

$$I_{DSA} = \frac{W}{L} C_{ox} \frac{\mu_{FET}(V_{GS} - V_T)}{\left(1 + R\frac{W}{L} C_{ox}\mu_{FET}(V_{GS} - V_T)\right)} \times \frac{V_{DS}(1 + \lambda V_{DS})}{\left(1 + \left(\frac{V_{DS}}{V_{DSsat}}\right)^m\right)}^{1/m} + I_0 \tag{44}$$

where I_0 is the leakage current, R is the series resistance, λ accounts for the channel length modulation in the saturation regime. The parameter m controls the smoothness of the transition between the linear and the saturation regimes.

The effective mobility is modeled as [72]–[74]:

$$\mu_{FET} = \mu_{FET_0}(V_{GS} - V_T)^{\gamma} \tag{45}$$

μ_{FET0} is the value of mobility/Vaa$^{\gamma}$ when $V_{GS} - V_T = 1V$: $\mu_{FET0} = \frac{\mu_0}{V_{aa}^{\gamma}}$ The parameter γ is related to T_0 and is calculated by $\gamma = 2(T_0/T - 1)$. T is the operation temperature of the device under study. In [74] an expression for μ_{FET0} is given, in terms of the band mobility, γ, trap density and Fermi potential, and density of states in the bottom of the conduction band. The saturation modulation parameter (α_S) defines the saturation voltage as $V_{DSsat} = \propto_S(V_{GS} - V_T)$.

The drain current model in the subthreshold regime is calculated, assuming diffusion transport, as:

$$I_{DSB} = I_{DS_0} e^{\frac{2.3(V_{GS} - V_T)}{S}} \tag{46}$$

where S is the subthreshold swing and is extracted from the $\log(I_D) - V_{GS}$ characteristics in subthreshold. The value of I_{DS_0} is calculated from (1) when $V_{GS} = V_T + DV$, which corresponds to the threshold of diffusion conduction. DV is a fitting parameter.

A unified and continuous expression of the drain current is obtained by combining the above threshold expression and the subthreshold expression by means of interpolation functions:

$$I_{DS} = \left(I_{DSA}\frac{1 + \tanh(V_{GS} - (V_T + DV)Q)}{2}\right) + ((I_{DSB} + I_m)\frac{1 + \tanh(V_{GS} - (V_T + DV)Q)}{2} \tag{47}$$

where Q is a fitting parameter. I_m corresponds to the minimum experimental drain current value (leakage current).

In technologies where deep states need to be considered, a subthreshold regime is defined as the voltage range where

the Fermi level is in the deep states [72]. The transport mechanism in this regime is similar to the above threshold regime well below the conduction band (hopping and drift of released carriers), but the concentration of free charge is lower than in the above threshold regime. When deeps states cannot be neglected, the regime below the flat-band voltage, where diffusion transport dominates is now called deep subthreshold regime.

The modeling of the subthreshold regime, where the Fermi level is in the deep states, is similar to the above threshold regime, but parameters have different values, related to the DOS of the deep states. The drain current can be described as [72]:

$$I_{bt}(V_{GS}, V_{DS1}) = K\frac{(V_{GS} - V_{FB})^{1+\gamma_b}}{V_{bb}{}^{\gamma_b}}V_{DSe1} \tag{48}$$

where V_{FB} is the flat band voltage and V_{DSe1} is n effective drain-source voltage in subthreshold, Eq(48). V_{bb} and γ_{b} are parameters defining the variation of mobility with gate bias in the subthreshold regime and are extracted analytically according to [72]; γ_b depends on the temperature T and on the characteristic temperature of the deep states distribution (T_2) (See Eq. (44)).

$$V_{DSe1} = V_{DS}\left[1 + \left(\frac{V_{DS}}{\alpha(V_{GS} - V_{FB})}\right)^m\right]^{-\frac{1}{m}} \tag{49}$$

with $\alpha = 0.8$.

A unified subthreshold current model is obtained by sewing together both parts of the subthreshold region: (Eqs.(46) and (48)):

$$I_{t1} = |I_{DSB}|\left[\frac{1 - tanh[(V_{GS} - (V_{FB} + V_1))Q_1]}{2}\right] + |I_{bt}|\left[\frac{1 + tanh[(V_{GS} - (V_{FB} + V_1))Q_1]}{2}\right] \tag{50}$$

where Q_1 is a fitting parameter.

The expression of the total drain current is obtained by binding the above threshold, subthreshold, and deep subthreshold regions, i.e., I_{ab} and I_{t1}; and in adding the off-current I_{m}.. Thus, the total drain-to-source current is described by (51):

$$I_{DS} = \pm\left[|I_m| + I_{DSA}\left[\frac{1 - tanh[(V_{GS} - (V_T + V_0))Q_0]}{2}\right] + |I_{t1}|\left[\frac{1 + tanh[(V_{GS} - (V_T + V_0))Q_0]}{2}\right]\right] \tag{51}$$

V_0 and Q_0 are adjustable parameters. V_0 is selected so that the value V_T+ V_0 is slightly over V_T to provide a correct sewing point of both regions; Q_0 modifies controls the transition between the subthreshold and the above threshold regimes.

To extract the key physical parameters in the above threshold regime, we apply the integral function H(V_{GS}) described by [98] to the I-V_{GS} characteristics at low V_{DS}, and use linear regression to extract parameters. This is the same procedure as in [69], but applied separately to the subthreshold and the above threshold regimes.

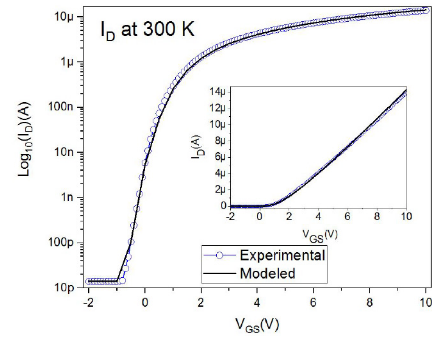


FIGURE 22. Modeled I_D vs V_{GS} at 300K (V_D = 0.5V). From [39].

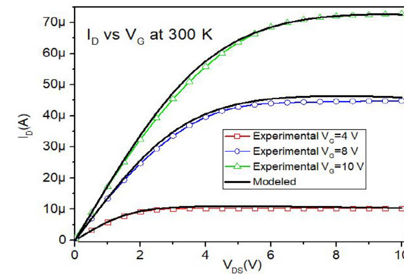


FIGURE 23. I_D vs V_{DS} experimental and modeled at 300K. From [93].

The model was validated by comparison with experimental I-V data from different AOS TFT technologies, including IGZO TFTs from TNO (Eindhoven, The Netherlands). These transistors have a top Etch Stop Layer (ESL) (Fig. 1). The device under study has a channel length of $L = 21\mu$m and channel width of $W = 100\mu$m. The insulator capacitance is $C_{ox} = 20nF/cm^2$, the relative dielectric constant is $\varepsilon r = 4.7$, the insulator thickness is $t_i = 200nm$ and the thickness of the ESL is $t_d = 100nm$.

As seen in the Figures 22–23, good agreement was observed with experimental transfer and output characteristics through all operation regimes.

When the Fermi level is close to the conduction band, percolation effects have to be considered. In this case, and after accounting for percolation effects in the mobility expressions, the UMEM.

This model was formulated in a physical way by means of developing an expression of the field-effect IGZO TFTs mobility in terms of physical device parameters. Both trapped and free carriers are considered. Percolation effects (percolation over potential barriers in the conduction band) can be included.

In addition, a simple procedure was developed, to determine the localized density of states at conduction band energy, gato and its characteristic temperature Tt, with the advantage of requiring only a measured linear transfer

characteristic at room temperature to which the extraction procedure to model IGZO TFTs previously developed in the Unified Model and Extraction Method (UMEM) adapted to AOS TFT is applied.

The procedure developed allows to calculate the relation of the empirical mobility model parameters which up to now are usually obtained by extraction methods, with device physical parameters. An empirical analytical expression to represent the dependence of the surface potential on the gate voltage was developed and validated. Using this expression, the procedure described to calculate the above mentioned parameters is completely analytical. The procedure also allows to calculate the gate voltage for which the Fermi level reaches the lower edge of the conduction band, much simpler than reported before

The tail density at the edge of the conduction band (g_{ato}) is calculated from [34]:

$$g_{ato} = \frac{Nc\frac{2}{\sqrt{\pi}}[\int_0^{\infty} \frac{\sqrt{x}}{1+e^{x-\frac{\varphi s-\varphi f}{\varphi t}}}dx - (\int_0^{\infty} \frac{\sqrt{x}}{1+e^{x}}dxe^{\frac{-\varphi f}{kb\bullet T_0}}}{(kbT_T)\left[\left(\int_0^1 \frac{1}{1+z^{\frac{T_T}{T}}}dze^{\frac{\varphi f}{kb\bullet T_0}}\right) - \left(\int_0^{\frac{\varphi f-\varphi s}{e^{\varphi tt}}} \frac{1}{1+z^{\frac{T_T}{T}}}dze^{\frac{\varphi f}{kb\bullet T_T}}\right)\right]} \tag{52}$$

where, ϕ_s is the surface potential, φ_f is the fermi level potential, ϕ_t is the thermal potential and ϕ_{tt} is the characteristic potential, $T_T = 2T_0 - T_T$. N_C is the free electron concentration conduction band.

From S we extracted the density of interface states, Dit following [82]:

$$D_{it} = \frac{\left(\frac{SqCi}{kT\ln(10)} - Ci - C_D\right)}{q} \tag{53}$$

where C_D is the depletion capacitance of the IGZO layer, calculated as in [82].

H. CHARGE AND CAPACITANCE MODEL

On the other hand, a charge model for AOS TFTs based on the same principles as the DC model explained above was developed [83]. A few previous papers [84]–[86] presented models of the IGZO capacitances, but demonstrated only the agreement between the gate capacitance and simulations/measurements.

Charge expressions (gate, drain and source charges) are obtained for both the subthreshold and above-threshold current assuming that deep states dominate in the former regime and tail states in the latter.

Using an analysis similar to the one in Section II-A. Reference [82] to develop charge and capacitance models for organic TFTs and considering only the first exponential term (deep states) in the DOS defined in (1), we developed the charge and capacitance models for both the subthreshold (Fermi level in deep states) and the above threshold regime (Fermi level in tail states). The expressions of total charges have the same form in both regimes, but parameters are related to the densities of deep and tail states, respectively.

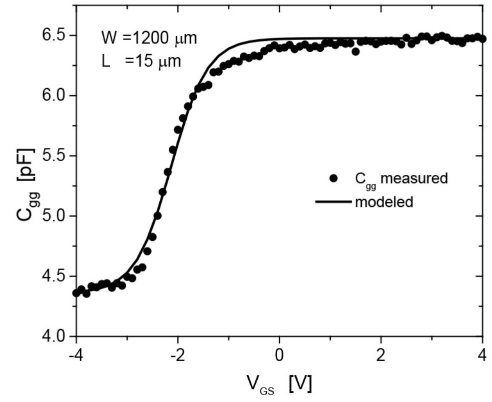


FIGURE 24. Comparison of measured and modeled C_{gg} capacitance at V_{DS}= 0 V. . IGZO TFTs experimentally targeted in Figs. 21–22. From [87].

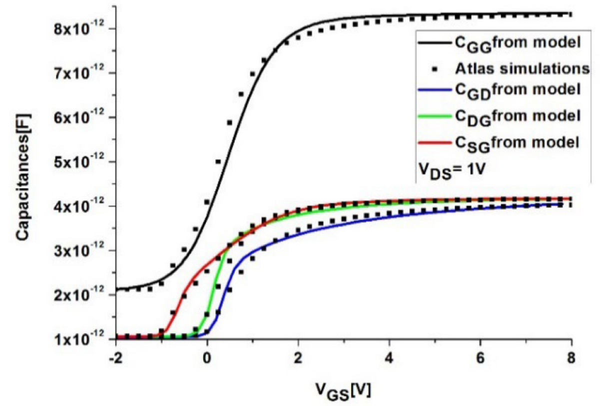


FIGURE 25. Capacitances (C_{GG}, C_{GD}, C_{DG}, C_{SG}) vs. V_{GS} for V_{DS} = 1V. IGZO TFTs experimentally targeted in Figs. 21–22. From [83].

For example, in the above threshold regime, the total gate charge is written as:

$$Q_{\mathrm{CHd}} = \frac{W^2C_{ox}^2}{I_{\mathrm{DSa}}}\mu_{FET0}\left[\frac{(V_{\mathrm{GT}} - V_{\mathrm{DSed}})^{3+\gamma} - (V_{\mathrm{GT}})^{3+\gamma}}{3+\gamma}\right] \tag{54}$$

I_{DSa} is a non. linearized expression of the above threshold current (44), with the same form as (22).

The total charges at the drain and the source are obtained following the Ward-Dutton channel charge partitioning scheme [83], where the capacitances are computed using the equivalent charge densities at the source and drain ends of the channel.

An interpolation function to combine both the subthreshold and the above threshold charge expressions. The intrinsic capacitance expressions are found by differentiating the resulting charge expressions with respect to the applied bias, as explained in [83]: $C_{\mathrm{ijd}} = \frac{-\partial Q_{\mathrm{id}}}{\partial V_j} i \neq j$, $C_{\mathrm{ijd}} = \frac{\partial Q_{\mathrm{id}}}{\partial V_j} \mathrm{i} = \mathrm{j}$, where i and j indicate the gate, source or drain electrodes.

The resulting capacitance model was validated by comparison with experimental and TCAD results from ESL IGZO TFTs, as we see in Figs. 24–25.

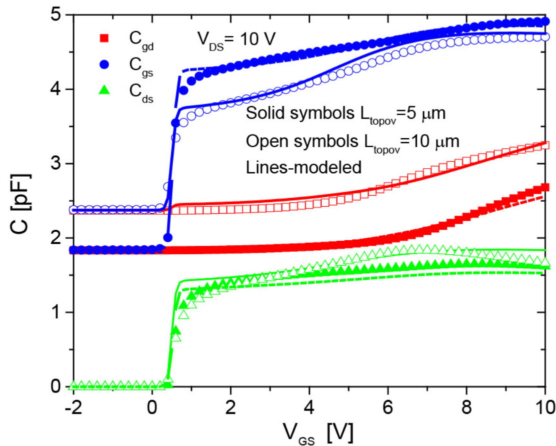


FIGURE 26. Comparison of simulated and modeled capacitance for an IGZO TFT with 5 and 10 μm of top metal overlap. From [87].

On the other hand, bias-dependent overlap capacitances have to be included in order to adequately model the saturation regime [87], [88]. In staggered bottom gate structures the effect of the top metal overlap contacts (for example when using an etch stop layer, ESL [89]–[92]). The top metal overlap near the drain serves as a second gate with a voltage applied equal to V_{DS}. An expression to account for this effect was included in the model, as well as the effect of the overlap capacitance between gate and drain/source and the reduction of the channel capacitance with the increase of drain voltage. The calculated capacitance is a function of the threshold voltage, (V_T), the mobility and saturation parameters which are extracted using the Unified Model and Extraction Method (UMEM) for AOSTFTs. Very good agreement was observed between the modeled and TCAD-simulated and experimental characteristics shows a very good agreement (Fig. 26).

I. TEMPERATURE EFFECTS

Most studies of temperature effects in AOS TFTs are so far limited to high temperatures [94]. The UMEM AOS TFT model was also adapted to different temperatures, from 210 K to 370 K. Measurements were done at both low and high temperature conditions. Model parameters were extracted for each temperature. The model was demonstrated to be valid in the range of temperatures from 210 K to 370 K [93] (Fig. 27).

V. LOW FREQUENCY NOISE MODELING

Measurements of low frequency noise of IGZO TFTs and OTFTs (fabricated by TNO and CEA, respectively) were carried out to determine the main mechanism which contributes to noise and to develop noise compact models.

It was found that the power spectral density (PSD) is proportional to 1/f (being f the frequency) in log-log scale in both devices (Fig. 28). Therefore, it was confirmed that the low frequency noise was Flicker noise.

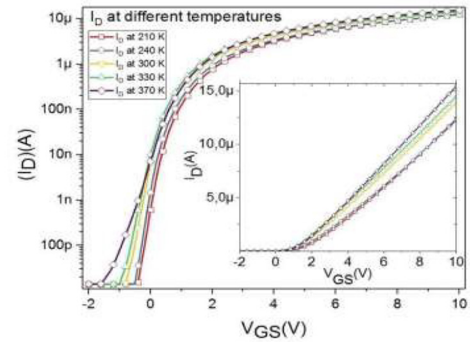


FIGURE 27. Modeled (lines) and measured transfer characteristics of IGZO TFTs. Same device process as [93].

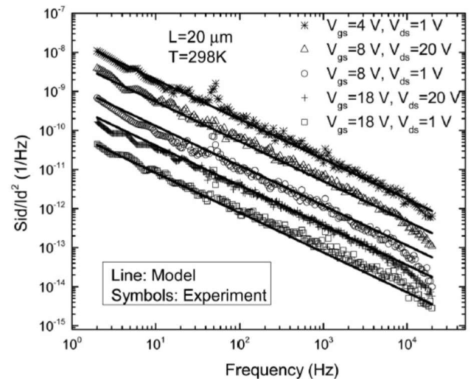


FIGURE 28. Measured and modeled normalized 1/f noise power spectral density of 15 x 100 μm²· IGZO TFT (from TNO) over a range of frequencies in subthreshold, linear, and saturation regime operation at 298 K. From [95].

TABLE 3. Comparison of the carrier number fluctuation, mobility fluctuation and unified models in linear regime.

Models	
ΔN	$\frac{S_{ID}}{I_D^2}=\frac{k^*}{f}\frac{1}{C_{ox}^2WL}\frac{1}{(V_{GS}-V_{th})^2}$
Δμ	$\frac{S_{ID}}{I_D^2}=\frac{q}{C_{ox}WL}\frac{\alpha_H}{f}\frac{1}{(V_{GS}-V_{th})}$
ΔN - Δμ	$\frac{S_{ID}(f)}{I_D^2}=\left[1\pm\alpha_s\mu_{eff}C_i\frac{I_D}{g_m}\right]^2\left[\frac{g_m}{I_D}\right]^2S_{V_{FB}}(f)$

The 1/f noise in semiconductor devices can be due to carrier number fluctuations, bulk mobility fluctuations, or a combination of surface mobility and carrier number fluctuations ("unified model"). Each of these models lead to a different expression of the power spectral density (Table 3).

In the devices targeted the normalized drain current spectral density was inversely proportional to the channel length, what indicated that the Flicker noise was mostly generated in the channel and not in the contacts [95]–[97].

To determine the dominant noise mechanism, I-V measurements were carried out in order to extract model parameters. It was found that the case of the targeted IGZO TFTs, the normalized drain current spectral density was

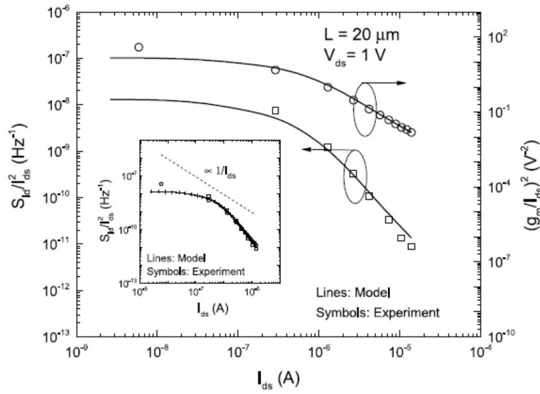


FIGURE 29. Plot of model-experimental data comparison for $S_{id}/I_d{}^2$ (left) and $[g_m/I_{ds}]^2$ (right) with respect to drain current for a 20 × 100μm^2 IGZO TFT. V_{ds} = 1 V. From [96].

inversely proportional to the inverse of $(V_{gs}-V_T)^2$, being Vgs the gate source voltage and V_T the extracted threshold voltage and also proportional to $(g_m/I_d)^2$ (being gm the transconductance and Id the drain current), as shown in Fig. 29. Therefore, we concluded that the main dominant noise mechanism as the fluctuation on the number of carriers (which takes place at the interface). In previous published papers other authors found that it was the fluctuation of mobility (which takes place in the film) the dominant mechanism [98]–[101]. However, the IGZO TFTs we targeted were much thinner (15 nm IGZO film) than those previously reported and besides they were Edge Stop Layer (ESL) structures. This means that the surface effects are stronger that in the previously reported devices, and as a result, the fluctuation on the number of carriers. Besides, we extracted a density of states of the targeted devices which resulted to be quite low, what means that the quality of the IGZO film was good, and this decreases the contribution to noise of traps in the film [95], [96].

Afterwards, a full compact model for the Flicker noise in IGZO TFT was developed and successfully compared with experimental data [96] (Fig. 29).

Similarly, Flicker noise in OTFT devices was analyzed from two polymeric technologies fabricated by CEA-Liten. In the oldest and lower mobility technology, the normalized drain current spectral density ($S_{ID}/I_D{}^2$) was inversely proportional to the inverse of $(V_{gs}-V_T)$ and not proportional to $(gm/Id)^2$, demonstrating that the main noise mechanism were mobility fluctuations. This was observed in other technologies [102]–[106].

However, in the new and higher mobility OTFTs it was proportional to $(gm/Id)^2$, and therefore noise was mostly due to carrier number fluctuation at the interface. This was related to the fact that the extracted degree of amorphity (quality of the organic layer) was larger in the high mobility TFTs than in the lower mobility ones. Afterwards, a full compact model for the Flicker noise in OTFT was developed and successfully compared with experimental data (Fig. 30) [97].

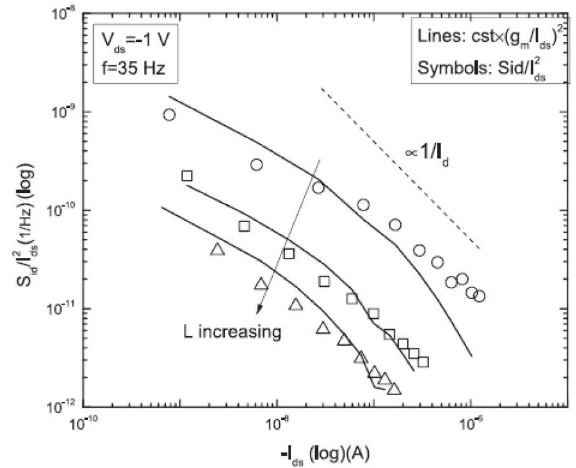


FIGURE 30. Comparison of drain current intensity variation of $S_{id}/I_d{}^2$ and $[g_m/I_{ds}]^2$ in the linear regime. The dotted line corresponds to 1/Ids for a 10 μm OTFT from CEA-Liten. From [97].

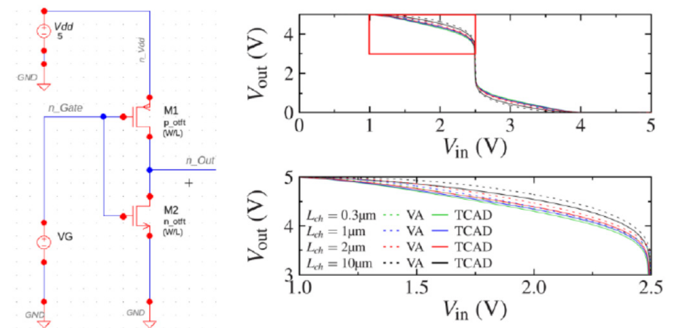


FIGURE 31. Comparison between the TCAD and Verilog-A model inverter with various channel length from 10 μm down to 0.3 μm.

VI. COMPACT MODEL VALIDATION

The compact models for AOS TFTs and OTFTs were implemented in Verilog-A files. The implementation of these models was evaluated by means of the simulation of test circuits. Once it was demonstrated that their implementations were correct, we proceeded to validate these models by comparison with TCAD and experimental results from test circuits.

For example, a TCAD simulation of a single OTFT was carried out and the charge-based OTFT Verilog-A model described in Section II-A. was fitted to this data. A n-type OTFT was emulated with the same characteristics as the p-type OTFT to create a CMOS inverter. Ultimately, four CMOS inverters were simulated with Silvaco's ATLAS software of which both OTFTs have channel lengths of 0.3, 1, 2 and 10 microns. The scaling from 10 microns down to 0.3 microns was done using the same fitting parameters in order to test the scalability of the Verilog-A model. The agreement between the TCAD simulation results and the ones obtained using our compact model in the Verilog-A code (Fig. 31).

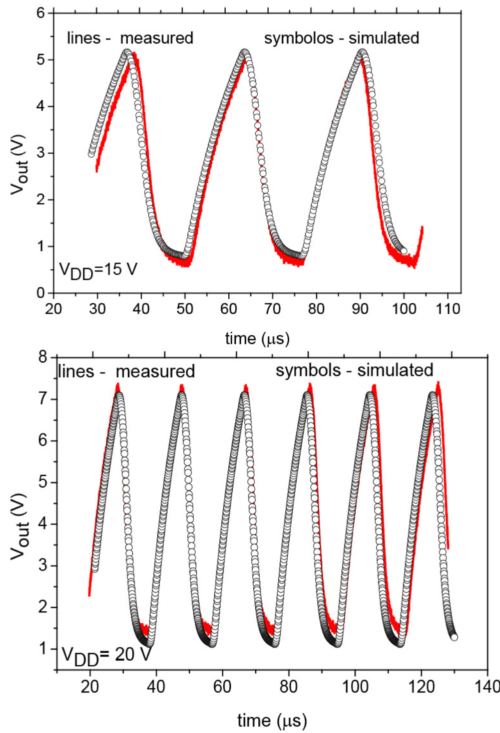


FIGURE 32. **Comparison between the output signals (measured and simulated) of the 19-stages ring oscillator at (a) V_{DD}= 15 V and (b) V_{DD}= 20 V. From [107].**

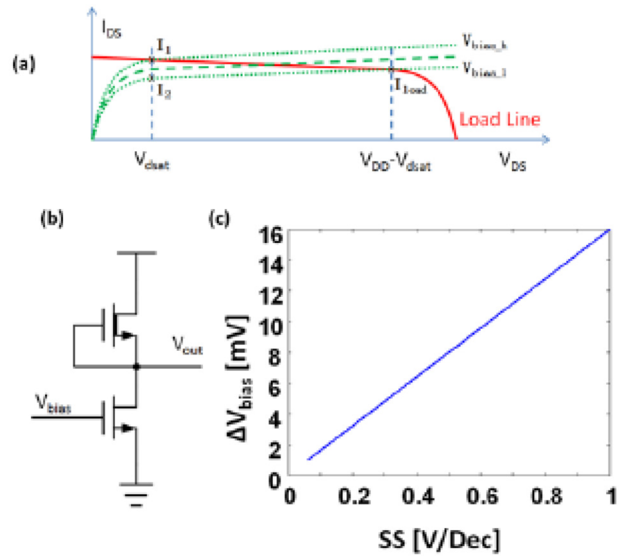


FIGURE 33. **Useful bias range for a depletion load common-source amplifier. (a) Conceptual figure of the load line and transfer curve of the amplifier, where the green curve illustrates the correct bias condition and blue curves illustrates the one or the other TFT in non-saturation. (b) Circuit schematic of the amplifier indicating the useful bias range with respect to SS. (c) Useful bias range with respect to SS based on data extracted from IGZO TFT, where VDD = 2V and Vdsat = 0.48V.**

Several circuits were designed and fabricated using the developed models.

A 19-stage IGZO TFT Ring Oscillator (RO) was experimentally characterized to validate the AOS TFT model [107]. The dynamic behavior of the simulated circuit, when the TFT internal capacitances are increased or decreased and for different supply voltages of 10, 15 and 20 V, was compared with measured characteristics, obtaining a very good agreement (Fig. 32). Afterwards, the model was used to simulate the dynamic behavior of a pixel control circuit for a light emitting diode active matrix display (AMOLED), using an AOSTFT.

Besides, using the compact model, a common-source amplifier was demonstrated with a peak gain of 260 V/V and maximum circuit power consumption of $<$1 nW (Fig. 33).

VII. CONCLUSION

Physics-based compact models for OTFTs and AOS TFTs were developed by means of several new approaches to account for the physical effects determining the behavior of these devices. The resulting DC, AC and low-frequency noise models reproduced very accurately the experimental characteristics of OTFTs and AOS TFTs under a broad range of applied bias, device dimensions, frequencies and temperatures. After implementation in Verilog-A, the models were successfully validated by means of the design and simulation of test circuits.

ACKNOWLEDGMENT

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