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Investigation Influence of Channel Transport on Output Characteristics in Sub-100nm Heterojunction Tunnel FET

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ABSTRACT In this paper, the influences of channel transport on the output characteristic in sub-100nm heterojunction tunnel FET have been investigated through TCAD simulation. The calibrated tunneling and transport parameters with experiment have been adopted. The influences of the parameters characterizing channel transport, i.e., mobility, channel length, and saturation velocity, are analyzed in detail under different biases. It is found that the channel transport has stronger impact on the performance of the device biased in the linear region and with smaller mobility, longer channel, and higher saturation velocity. The saturation drain voltage can be reduced by improving the mobility and reducing the saturation velocity. However, the latter will reduce the current simultaneously. What's more, considering quantum confinement, the variation in performance of the device induced by the change of mobility is still visible after some optimization strategies are used.

INDEX TERMS Channel transport, heterojunction tunnel FET, mobility, quantum confinement, saturation velocity.

I. INTRODUCTION

Tunnel FETs are regarded as the promising successors to MOSFETs in Internet of Things applications due to their steep subthreshold slope (SS) and low OFF-state current [1]–[4]. Although there are two transport processes in TFETs: band-to-band tunneling (BTBT) at the tunneling junction and the subsequent channel transport along the channel, the influence of the latter is often concealed due to the drawback of low On-state current. However, with the developments of fabrication process, the encouraging results, such as SS of 48mV/decade combined with I_{60} (the current at which the SS is equal to 60mV/decade) of 0.31μA/μm, and high On-current of 433μA/μm at 0.5V of drain bias, have been experimentally reported in III-V heterojunction TFET (H-TFET) [5], [6], and the channel length in H-TFETs are also scaling down to sub-100nm [5], [7]. At this time, how the channel transport influences the performance of H-TFETs toward state-of-the-art should be investigated in details for their industrial design and implementation in circuit. Although the influences of channel transport have been mentioned in previous works [8], [9], the detailed research and deep understanding of its impact on output characteristic of H-TFETs are missing. Considering that channel transport has much more significant influence when TFETs turn on, its impact on output characteristics merit further study.

This paper presents the detailed analysis of the output performance in the popular combination As/Sb H-TFET with channel transport. First, the device structure and parameters used during the simulation are given in Section II. Then, the influences of mobility, channel length, and saturation velocity which characterize the transport in the channel are investigated, followed by the quantum confinement effect in Section III. At last, conclusion is drawn in Section IV.

II. DEVICE STRUCTURE AND SIMULATION SET-UP

Fig. 1 shows the structure of an n-type double-gate H-TFET studied in this work. As a representative example, we choose

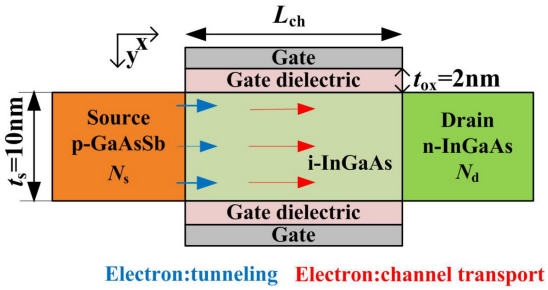

FIGURE 1. Structure of DG H-TFET. t_{ox} = 2nm, t_s = 10nm, N_s = 5×10^{19}cm^{-3}, and N_d = 5×10^{18}cm^{-3}.

$GaAs_{0.5}Sb_{0.5}$ as source material and $In_{0.53}Ga_{0.47}As$ as channel material [10]. The gate dielectric is HfO_2. The source doping $N_s = 5\times10^{19}$cm^{-3}, drain doping $N_d = 5\times10^{18}$cm^{-3}, body thickness t_s = 10nm, oxide thickness t_{ox} = 2nm, and channel length L_{ch} = 50nm are taken as default values unless otherwise specified. The H-TFET performance is characterized by Sentaurus TCAD numerical simulator [11]. During the simulation, the dynamic nonlocal band-to-band tunneling, band gap narrowing, and Fermi statistics within the drift-diffuse channel transport framework with high-field saturation are activated.

To retain the drift-diffuse framework in short-channel devices, the quasi-ballistic correction is used [12], [13], and at this time the effective mobility (μ_{eff}) in low-field region is written as

$$\mu_{eff} = (1/\mu_{sc} + 1/\mu_{bl})^{-1} \tag{1}$$

by using the Matthiessen′s rule. μ_{sc} is the scattering-limited mobility, and $\mu_{bl} = \nu_t L_{ch}/(2V_t)$ is the ballistic mobility (ν_t is the thermal velocity and V_t is the thermal voltage) [13]. Furthermore, the Canali model is used to describe the mobility in the high-field region, as shown below

$$\mu = \mu_{eff}/\left[1 + \left(\mu_{eff}F/\upsilon_{sat}\right)^{\beta}\right]^{1/\beta} \tag{2}$$

where F is the electric field, υ_{sat} is the saturation velocity, and β is the exponent factor.

Table 1 and 2 give the calibrated BTBT and channel transport parameters used during the simulation, respectively. Since β is usually as an empirical fitting factor [12], [14], combined with 5.97×10^7cm/s of υ_{sat}, the non-even and best fit value of β = 1.395 is used as in [12]. The verified TCAD result against experimental data [15] is shown in Fig. 2(a). The good agreement between the TCAD simulation and experiment is observed under different drain biases. The measured 43mV/decade of SS at low drain bias further demonstrates the advantages of TFET in low-power applications. It should be noted that during the calibration process, the trap-assisted tunneling (TAT) is also activated to fit the subthreshold behavior with 5×10^{11}eV^{-1}cm^{-2} of midgap trap at the oxide/channel interface. However, TAT is not considered in the following simulation about the output characteristic since it generally plays a major role in the subthreshold region [16].

TABLE 1. Calibrated tunneling parameters with experiment data [15].

Symbol	Parameter	GaAsSb	InGaAs
$E_{g,eff}$ / eV	effective tunneling barrier height	0.42	
m_e / m$_0$	electron effective mass	0.0447	0.041
m_{lh} / m$_0$	light hole effective mass	0.066	0.052
A_{btbt} / cm^{-3}s^{-1}	tunneling prefactor	1.4×10^{20}	1.3×10^{20}
B_{btbt} / Vcm^{-1}	tunneling exponential factor	6.4×10^6	5.7×10^6

TABLE 2. The range of channel transport parameters used in this paper. The bold is calibrated data with experiment result [15].

Symbol	Parameter	InGaAs channel
μ_{sc} / cm^{2}V^{-1}s^{-1}	scattering-limited mobility	160, **1600**, 16000
υ_{sat} / cms^{-1}	saturation velocity	**5.97×10^7**, 1.07×10^7
β / 1	exponent factor	**1.395**

Since μ_{sc} is defined as scattering-limited mobility, different scattering mechanism and degree make it have a large range [17]. Thus, for comparison, the cases with 160cm^2/Vs and 16000cm^2/Vs of μ_{sc} are also investigated except the calibrated 1600cm^2/Vs of μ_{sc}, as shown in Table 2. Generally, the III-V materials-based long channel FETs have been demonstrated to have a μ_{sc} ranging from several hundred to several thousand cm^2/Vs under different processes and parameters [17]–[21]. For example, in [18], ∼1600cm^2/Vs of electron mobility has been demonstrated in 10μm-long and 10nm-thick of InGaAs-on-InP device with "self-cleaning" Al_2O_3-based dielectric stacks. The similar value of ∼1500cm^2/Vs is also achieved in 5μm-long of InGaAs-OI FET on Si substrate by direct wafer bonding with optional chemical mechanical polishing [21]. However, when the scattering degree is aggravated, such as by the degraded oxide/channel interface quality, μ_{sc} will decrease dramatically [17]. On the contrary, μ_{sc} will increase [12], [17], [22]. Thus, 160cm^2/Vs and 16000cm^2/Vs of μ_{sc} can be regarded as the cases with severer and weaker scattering mechanisms, respectively, compared to the calibrated case with 1600cm^2/Vs of μ_{sc} which the current process generally can achieve [18], [21]. Note that the range of μ_{eff}, which actually works, is not as large as μ_{sc} due to the influence of μ_{bl}. As for the other comparison case with 1.07×10^7cm/s of υ_{sat} given in Table 2, it can be regarded as the high temperature situation [11], [14]. Unless otherwise specified, the calibrated channel transport parameters are used.

III. RESULTS AND DISCUSSIONS

Fig. 2(b) plots the dependence of $I_{ds} - V_{gs}$ characteristic on the channel transport based on the calibrated TCAD. It can be seen that the channel transport hardly affects the SS of TFET due to the relatively small current in subthreshold region, but its influence gradually emerges with the increase of V_{gs} and thus the current, further indicating the necessity of this study.

Fig. 3 shows the $I_{ds} - V_{ds}$ curves under three sets of mobility parameters presented in Table 2. From Fig. 3, it

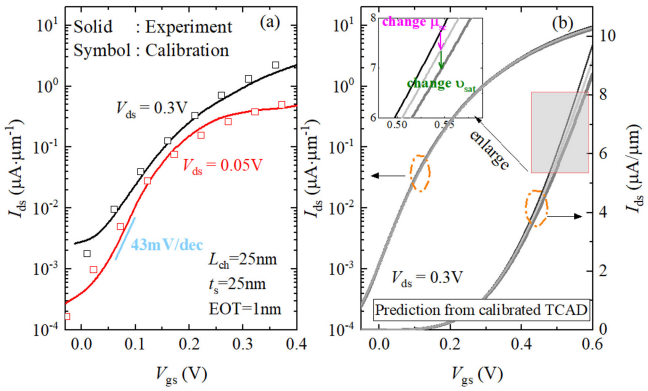

FIGURE 2. **(a) Comparison between TCAD result and experimental data [15]. The calibrated BTBT and channel transport parameters are presented in Table 1 and 2, respectively. The TAT is included during this calibrated simulation with the midgap trap density of 5×10^{11}eV^{-1}cm^{-2}. (b) The influence of channel transport on the $I_{ds} - V_{gs}$ characteristic.**

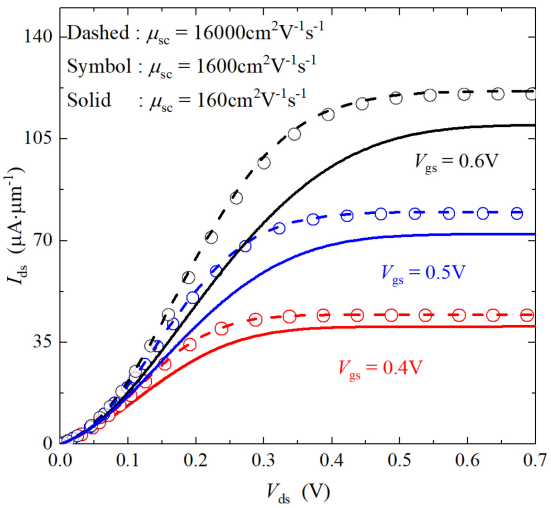

FIGURE 3. **$I_{ds} - V_{ds}$ characteristics under different mobilities and gate biases.**

is plain to see that the drain current increases when μ_{sc} increases from 160cm^2/Vs to 1600cm^2/Vs. In order to manifest the dependences of different operation states of the output characteristic on the channel transport, the current in linear/saturation ($I_{ds,lin}$/$I_{ds,sat}$) region under different mobilities at $V_{gs} = 0.5$V is shown in Fig. 4. $I_{ds,lin}$ and $I_{ds,sat}$ are enhanced by 23.5% and 9.43%, respectively at $L_{ch} = 50$nm with μ_{sc} increasing from 160cm^2/Vs to 1600cm^2/Vs. The corresponding band-diagrams are plotted in Fig. 5, to give a deep insight into the influence of the mobility. From Fig. 5, it can be observed that the valence band in the source, the conduction band in the channel and thus the tunneling window are barely affected by the channel transport. The major impact of the channel transport is on the change of the electron quasi-Fermi potential (e-QFP), i.e., the available states. Hence, the corresponding enlarged e-QPF profiles near the tunneling junction are presented in the insets of Fig. 5. The e-QFP lowers with the increase of mobility, meaning that more parts of V_{ds} drop over the tunneling junction under

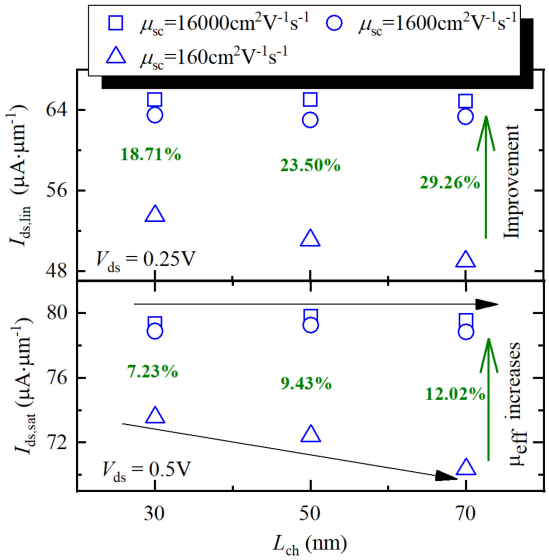

FIGURE 4. **Dependence of current in linear and saturation regions on channel length and mobility at $V_{ds} = 0.25$V and 0.5V, respectively. $V_{gs} = 0.5$V.**

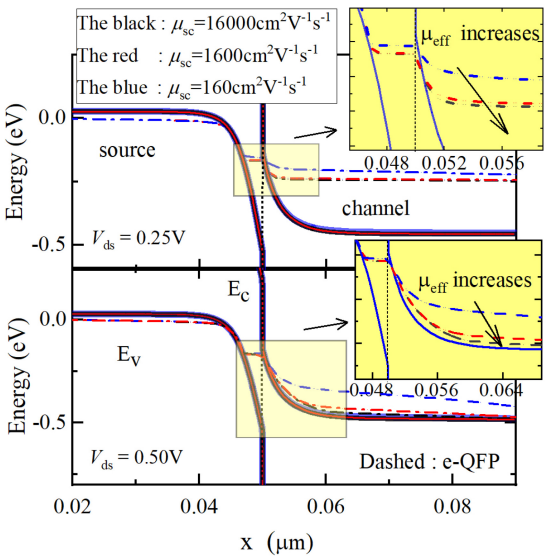

FIGURE 5. **Band-diagram in linear and saturation regions under different mobilities. The dash line is the electron quasi-Fermi potential profile. The inset is the enlarged band-diagram around the tunneling junction. $V_{gs} = 0.5$V.**

higher mobility. Thus, the available states and the current increase with the mobility.

From Fig. 5, for $\mu_{sc} = 160$cm^2/Vs and 1600cm^2/Vs, the e-QFP is -0.21V and -0.24V in linear region, and it is equal to -0.38V and -0.45V in saturation region, respectively. Compared to the case in linear region, although the difference of the e-QFP is bigger in saturation region, the change of the current is smaller, as shown in Fig. 4. This can be explained by analyzing the relationship between the dominant states (around the state where the shortest tunneling distance is), and the e-QFP. In the former, the differences of the e-QFPs near the tunneling junction locate in the dominant states, and

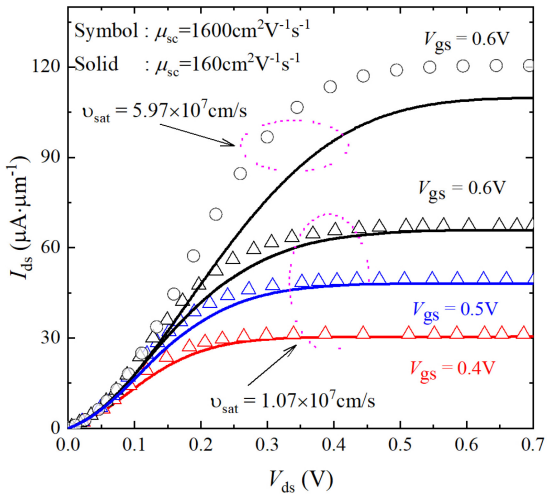

FIGURE 6. $I_{ds} - V_{ds}$ characteristics at $\upsilon_{sat} = 1.07\times10^7$cm/s under different gate biases. For comparison, the case with $\upsilon_{sat} = 5.97 \times 10^7$cm/s at $V_{gs} = 0.6$V is also shown.

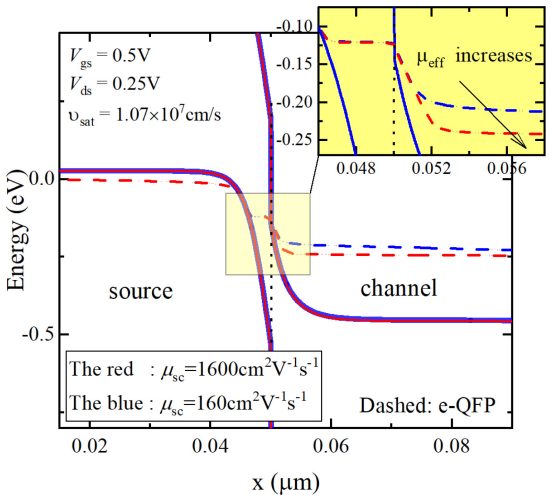

FIGURE 7. Band-diagram at $V_{gs} = 0.5$V and $V_{ds} = 0.25$V under $\upsilon_{sat} = 1.07 \times 10^7$cm/s and different mobilities. The inset is the enlarged band-diagram around the tunneling junction.

the differences in the latter are out those states. Therefore, the stronger dependence of the current on the mobility in the former, i.e., linear region, is observed.

When μ_{sc} varies from 1600cm^2/Vs to 16000cm^2/Vs, there is almost no change in the current, as shown in Figs. 3 and 4. When keeping increasing μ_{sc}, the mobility is gradually dominated by the same μ_{bl} because of the fixed L_{ch}. As a result, the differences of the e-QFP profiles (Fig. 5), and thus the current in these two cases are very small. This also suggests that materials with high bulk mobility in TFETs are more attractive from the perspective of variability induced by the fluctuation of interface quality.

Fig. 4 also plots the dependence of the current on the channel length. As expected, the impact of channel transport becomes stronger under longer L_{ch}. Besides, for the smaller mobility, the current decreases with the increase of L_{ch}, for example $I_{ds,lin}$ is 53.5, 51.1, and 49.0μA/μm for L_{ch} = 30, 50, and 70nm, respectively under μ_{sc} = 160cm^2/Vs. However, for the bigger mobility, the current is almost independent on L_{ch}, since the channel transport can be approximately regarded as quasi-ballistic type.

Furthermore, the output characteristics under different gate voltages at $\upsilon_{sat} = 1.07 \times 10^7$cm/s are shown in Fig. 6, to investigate the influence of saturation velocity. It can be found that the lower saturation velocity weakens the influence of the mobility. For $\upsilon_{sat} = 5.97 \times 10^7$cm/s, $I_{ds,lin}$ at $V_{ds} = 0.25$V and $V_{gs} = 0.6$V is increased from 63.2μA/μm to 81.3μA/μm when μ_{sc} changed from 160cm^2/Vs to 1600cm^2/Vs, almost 30% improvement. However, for $\upsilon_{sat} = 1.07 \times 10^7$cm/s, the improvement drops to 11%. The influence of mobility on the $I_{ds,sat}$ is hardly observed for the lower υ_{sat}. This suggests that the variation of the output characteristics in H-TFETs caused by the interface quality during the fabrication process can be mitigated more or less in the low saturation velocity or high temperature situation. However,

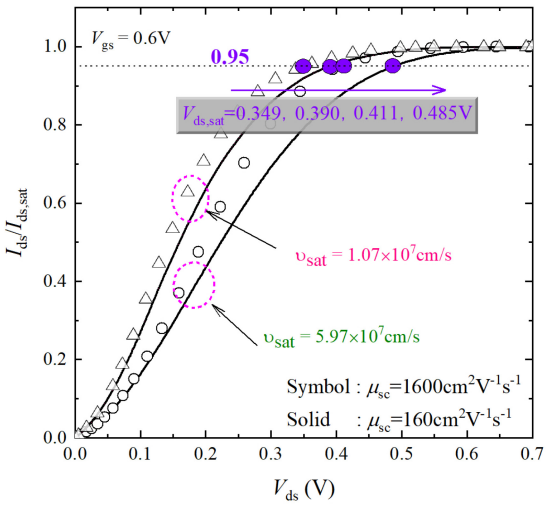

FIGURE 8. Dependence of the normalized $I_{ds} - V_{ds}$ curves at $V_{gs} = 0.6$V on mobility and saturation velocity.

this kind of mitigation is obtained at the cost of low current, considering that $I_{ds,sat}$ under $\upsilon_{sat} = 1.07 \times 10^7$cm/s is reduced down to 67μA/μm, about 1/2 of that under $\upsilon_{sat} = 5.97 \times 10^7$cm/s at $V_{gs} = 0.6$V, as shown in Fig. 6, which is not desirable.

The band-diagram under $\upsilon_{sat} = 1.07 \times 10^7$cm/s is shown in Fig. 7. Compared to the case in Fig. 5, the location in Fig. 7 where the difference between the e-QFPs starts to occur is farther away from the tunneling junction. It is well known that, in TFETs, the tunneling generation rate decays exponentially along the channel from the source side to the drain side. As a result, the influence of the mobility reduces when υ_{sat} lowers.

The normalized output characteristic from the data in Fig. 6 is shown in Fig. 8 to see if the channel transport has impact on the saturation drain voltage ($V_{ds,sat}$) or not.

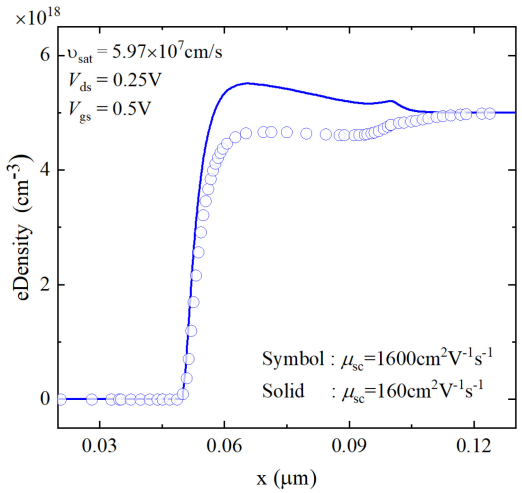

FIGURE 9. Density of electron profile along x axis under different mobilities.

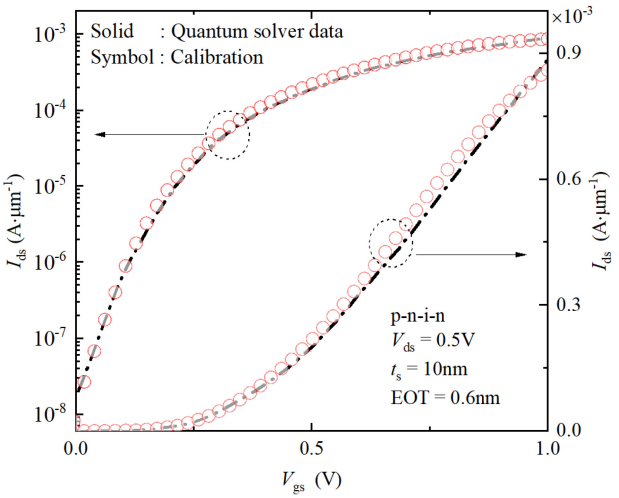

FIGURE 10. Calibration of simulation result for p-n-i-n H-TFET with t_s = 10nm and 2nm-thick of $In_{0.53}Ga_{0.47}As$ n+ pocket [27].

$V_{ds,sat}$ is defined as the drain voltage where the current is 0.95× of $I_{ds,sat}$. It can be found that $V_{ds,sat}$ is also dependent on the parameters characterizing the channel transport. The bigger μ_{sc} or smaller υ_{sat} is, the lower $V_{ds,sat}$ is. For example, $V_{ds,sat}$ reduces by 74mV when increasing μ_{sc} from 160 cm^2/Vs to 1600cm^2/Vs under $\upsilon_{sat} = 5.97 \times 10^7$cm/s. When the mobility is low, the inversion charge density in the channel is high (as shown in Fig. 9), and thus it needs more drain voltages to eliminate the inversion charge to reach to the saturation state. Since TFETs with coupled transport can be described as inserting a FET at the drain side of the ideal TFET [9], and the current is continuous in the devices, the saturation characteristic can also be analyzed from the perspective of FET part. As reported in [13], the saturation drain voltage is proportional to υ_{sat} for a nanoscale FET. Thus, $V_{ds,sat}$ is lower with smaller υ_{sat}, as shown in Fig. 8.

So far, the quantum confinement has been ignored. With the device scaling down to nanometer realm, the quantum confinement effect becomes important because it will lead to band splitting and band gap increasing, and thus reduce current. This effect is more serious for III-V materials due to their small effective mass [23]. Generally, the model with quantum effect is complex [24]. In order to take this effect into account easily, we adjust B_{btbt} to its quantum value ($B_{btbt,q}$) according to BGS scheme [25], as shown below

$$B_{btbt,q} = B_{btbt,bulk} \times \left(E_{g,q}/E_g\right)^2 \tag{3}$$

where $E_{g,q}$ is the band gap under confinement. As for A_{btbt}, it keeps its bulk value [25], since the modification of band gap rather than dimensionality is the main effect needed to be taken into account [26]. The calibrated result with quantum-mechanical solver [27] is shown in Fig. 10, with high mobility to capture the ballistic tunneling. The good agreement indicates that the simple BGS can be used to predict quantum effect with quantitative accuracy.

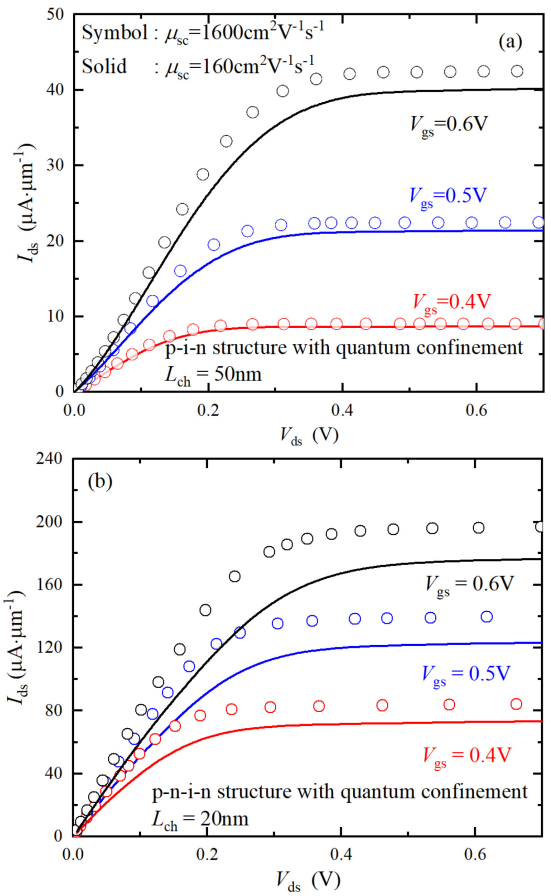

FIGURE 11. $I_{ds} - V_{gs}$ curves with quantum confinement effect in (a) p-i-n structure (same with Fig. 1) and (b) optimized p-n-i-n structure (same with that in [27]) under different mobilities.

Finally, using the calibrated parameters, we show the influence of channel transport on $I_{ds} - V_{ds}$ curves with quantum effects in Fig. 11. Fig. 11(a) and (b) are the cases in conventional p-i-n device and the optimized p-n-i-n structure

with 2nm-thick of $In_{0.53}Ga_{0.47}As$ n+ pocket, respectively. From Fig. 11(a), it can be found that the influence of channel transport becomes weaker when compared to the result in Fig. 3, which is caused from the decreased current. However, it indicates a lower limit of the variation in performance since no optimal design are adopted. After adopting some optimizations, such as adding n+ pocket in Fig. 11(b), channel transport still has significant influence on the performance of quantum confined device. At this time, when μ_{sc} increases from $160cm^2/Vs$ to $1600cm^2/Vs$, $I_{ds,sat}$ under 0.5V of V_{gs} varies about 13.9% at 20nm of L_{ch}, even larger than the 9.43% of variation in Fig. 3 with longer channel of 50nm. The result of the comparison between Figs. 3 and 11(b) with different L_{ch} further emphasizes the influence of structure optimization on the channel transport.

IV. CONCLUSION

The influences of channel transport on the output characteristic of sub-100nm H-TFET have been analyzed through the calibrated TCAD simulation. The results reveal that the impact of channel transport is on the profile of e-QFP, is more serious when the device is within linear region, and can be weakened by increasing μ_{sc}, reducing L_{ch} or lowing υ_{sat} to reduce the variability of the device. However, compared to lowing υ_{sat}, increasing μ_{sc} is more desirable since it can also simultaneously enhance the current and alleviated the delayed saturation. This indicates that the good III-V semiconductor-insulator interface quality in H-TFETs not only can ameliorate the subthreshold performance but also can improve the whole $I_{ds} - V_{ds}$ characteristic including channel transport-induced variability. Furthermore, for the small size device with strong quantum confinement, the impact of channel transport is still serious after adopting some optimizations. Thus, the channel transport should be taken into account in H-TFETs even with sub-100nm channel length, considering that high On-state current is one of goals of effort.

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