Received 3 July 2021; revised 28 July 2021; accepted 4 August 2021. Date of publication 17 August 2021; date of current version 13 December 2021.
The review of this paper was arranged by Editor C. Yang.

Digital Object Identifier 10.1109/JEDS.2021.3105375

ESD Design Verification Aided by Mixed-Mode Multiple-Stimuli ESD Simulation

MENGFU DI, ZIJIN PAN, CHENG LI, AND ALBERT WANG (Fellow, IEEE)

Department of Electrical and Computer Engineering, University of California at Riverside, Riverside, CA 92521, USA

CORRESPONDING AUTHOR: M. DI (e-mail: mdi002@ucr.edu)

This paper is an extended version of a report in IEEE EDTM2021 [6].

ABSTRACT Electrostatic discharge (ESD) protection is a grand design challenge for complex ICs in advanced technologies. ESD simulation is indispensable to guide ESD protection designs. However, no existing ESD simulation methods may accurately predict ESD protection designs in a universal manner due to various inherent limitations. TCAD-based ESD simulation is very useful for ESD protection designs. Transmission line pulse (TLP) and very fast TLP (VFTLP) are widely used to evaluate human body model (HBM) and charged device model (CDM) ESD protection designs, which provide rich details for calibrating TCAD ESD simulation for design prediction and validation. Using various ESD protection devices fabricated in 28nm CMOS and 45nm SOI CMOS technologies, a comprehensive experimental and simulation study finds that the ESD stimuli used in TCAD ESD design simulation have profound impacts on many subtle ESD protection behaviors, particularly in comparison with ESD testing. This study cautions against over-interpretation of TCAD ESD simulation results, obtained using any specific ESD stimulus, attempting to accurately predict practical ESD protection designs. A mixed-mode multiple-stimuli ESD simulation method is therefore developed to address the ESD stimulus induced ESD performance variation, hence offering a technique to achieve ESD protection design prediction.

INDEX TERMS CDM, ESD, HBM, stimuli, TCAD, TLP, VFTLP.

I. INTRODUCTION

On-chip electrostatic discharge (ESD) protection is required for ICs against ESD failures. On-chip ESD protection design becomes very challenging for high-performance and complex chips fabricated at advanced technology nodes [1]–[5]. Full-chip ESD protection design verification and prediction are the ultimate goal in practical ESD protection designs, which can only be achieved by careful ESD CAD simulation. These days, TCAD-based ESD simulation design method has been commonly used for ESD design optimization [4]. One critical decision to make in conducting TCAD ESD design simulation is to decide what input ESD stimulus to use to ensure accurate simulation of real-world ESD stressing events at chip level in order to avoid the possible "junk-in, junk-out" situation. Typically, a transient human body model (HBM) or charged device model (CDM) ESD waveform specified in selected ESD testing standards, or similarly, a fast square waveform produced by a transmission line pulse (TLP) or very fast TLP (VFTLP) ESD tester, is used as the input ESD zapping stimulus for TCAD ESD simulation [3]–[5]. However, several major unanswered problems exist in TCAD ESD simulation that can seriously affect the ESD simulation accuracy. First, the HBM and TLP ESD test set-ups are not identical to each other, and the same applies to CDM and VFTLP testers. While an HBM or CDM ESD event models the real-world ESD phenomenon, the corresponding TLP or VFTLP testing is merely an emulation of the real-world HBM or CDM ESD event, respectively. Accurate correlation between HBM ESD zapping and TLP ESD testing is still debatable today, which is even more true for the CDM and VFTLP measurement pair. Second, TLP or VFTLP testing utilizes a square waveform pulse train, not one simple square waveform similar to the corresponding single HBM or CDM waveform in real world. Hence, using a TLP or VFTLP square waveform pulse train inherently introduces errors in TCAD ESD simulation to model actual single-wave HBM or CDM ESD zapping test. On the other hand, using single-pulse TLP or VFTLP waveform in ESD

This work is licensed under a Creative Commons Attribution-NonCommercial-NoDerivatives 4.0 License. For more information, see https://creativecommons.org/licenses/by-nc-nd/4.0/

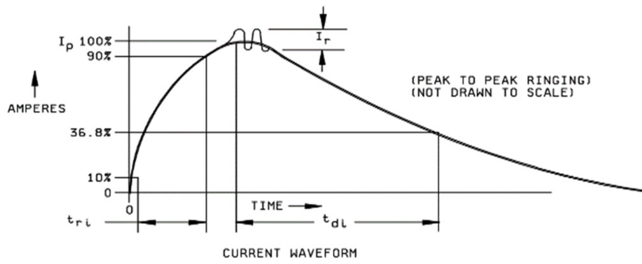

FIGURE 1. The classic HBM ESD waveform [7].

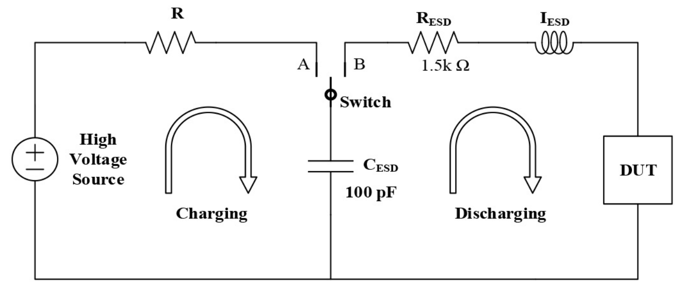

FIGURE 2. An equivalent circuit model for a standard HBM ESD tester including the charging and discharging procedures.

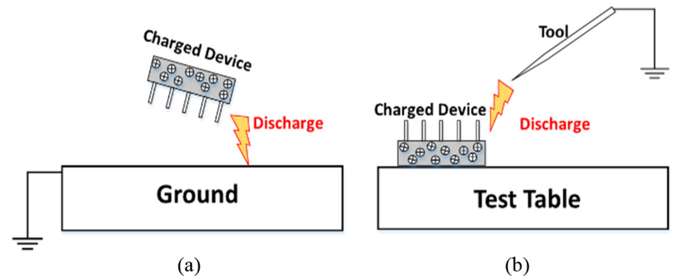

FIGURE 3. Different real-world CDM ESD charging and discharging scenarios: (a) Triboelectric-induced electrostatic charges accumulated inside a chip will be discharged when the IC is grounded, resulting in CDM ESD failures, and (b) a FICDM ESD testing model induces electrostatic charges into an IC and CDM discharging is initiated by contacting IC pin using a pogo pin [8].

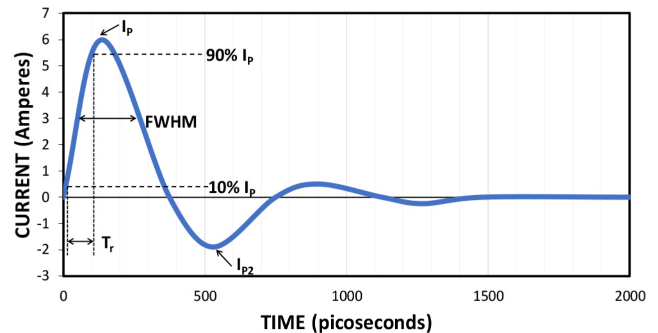

FIGURE 4. A typical CDM ESD discharging waveform [8].

simulation to model the TLP or VFTLP testing procedures also has fundamental uncertainty. Therefore, while HBM or CDM zapping is always required to evaluate ESD protection level and the corresponding TLP or VFTLP testing reveals rich transient ESD discharge details for HBM or CDM ESD protection designs, what would be the trustable TCAD ESD simulation procedure, particularly in terms of the ESD stimuli used, that can correlate HBM zapping with TLP stressing, or CDM with VFTLP ESD testing, respectively, hence accurately predicting ESD protection designs in Si? This paper, extended from a conference report [6], provides a thorough analysis of various TCAD ESD simulation scenarios using both real-world HBM and CDM ESD waveforms, and their corresponding TLP and VFTLP square waveforms, in both single-pulse and pulse train manners, as stimuli. It concludes that TCAD ESD simulation using either HBM (or CDM waveform), or the corresponding TLP (or VFTLP) pulse stimulus, alone, is insufficient in achieving ESD simulation accuracy. The paper introduces a new mixed-mode TCAD ESD simulation flow using combined HBM-TLP stimuli, or CDM-VFTLP stimuli, to enable ESD protection design prediction and verification.

II. HBM AND CDM ESD ZAPPING

The HBM ESD test model describes the human body induced ESD phenomena where electrostatic charges stored in a human body will discharge into an IC affected, resulting in HBM ESD failures. Fig. 1 depicts the original HBM ESD zapping waveform [7]. The key parameters for the standard HBM ESD waveform include the pulse rising time of $t_r \sim 10$ns and decay time (duration) of $t_d \sim 150$ns ($\pm$20ns).

Fig. 2 illustrates the equivalent circuit model for a standard HBM ESD tester where the capacitor C_{ESD} of 100 pF models a human body that is pre-charged. When touching a device under test (DUT), the electrostatic charges stored will be discharged into DUT through a human body resistor of $R_{ESD} \sim 1500\Omega$ and a parasitic inductor of L_{ESD}. The amplitude of the ESD pulse produced by an HBM ESD tester varies. For example, the peak transient current flowing into the DUT through the R_{ESD} of 1500Ω will be about 0.66A when C_{ESD} is pre-charged to 1KV. The HBM ESD discharge pulses can be considered as RC exponentially decaying waveforms.

CDM ESD phenomenon is completely different from HBM ESD events. HBM ESD is fundamentally a “from-external-to-internal” discharging event in nature, while CDM ESD describes a “from-internal-to-external” discharging phenomenon [9]. During a CDM ESD event, an IC is pre-charged, unavoidably and throughout its lifetime, and the electrostatic charges are distributed inside the chip. As such, when the IC is grounded (e.g., placed onto a PCB board), the charges stored inside the chip will be discharged into a ground, causing internal CDM ESD damages. Therefore, a CDM ESD failure is internal-oriented, while an HBM ESD damage is external-initiated. Fig. 3 illustrates different CDM ESD charging and discharging scenarios including triboelectric charging and field induction CDM event (FICDM) [8]. Compared to HBM ESD model, the

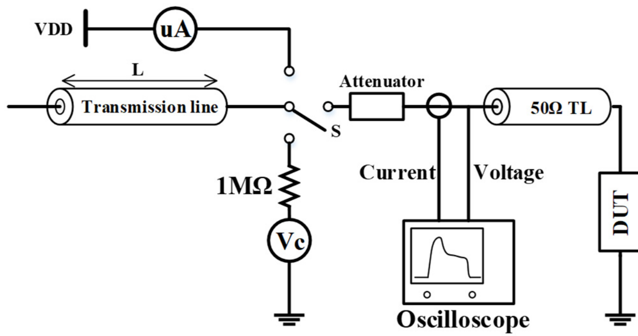

FIGURE 5. An equivalent circuit model for TLP tester.

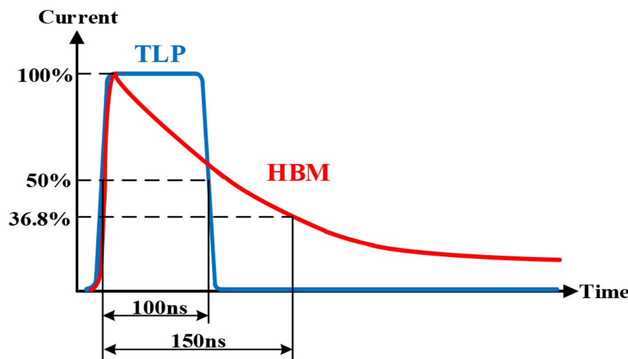

FIGURE 6. Correlating TLP and HBM waveforms in terms of the pulse rise time and the energy involved.

CDM ESD pulse is very short (full width at half maximum, or, FWHM = 250∼600ps) and rises extremely fast (t_r < 250ps), as depicted in Fig. 4 [8].

Before and after each HBM or CDM ESD zapping test, a DUT is characterized for its general functional Specs, commonly using DC testing for its leakage current (I_{leak}), and the Specs degradation is monitored as ESD failure criteria. For example, if I_{leak} increases by orders of magnitude after HBM or CDM ESD zapping, an IC is considered failed the ESD testing, typically giving a voltage level (V_{t2}) in KV or a thermal breakdown current level of I_{t2}. HBM or CDM ESD testing is destructive and does not provide useful transient ESD details; on the other hand, TLP or VFTLP testing is generally non-destructive and delivers instantaneous ESD discharging I-V-t characteristics that provide rich information for ESD CAD simulation calibration and design optimization.

III. TLP AND VFTLP ESD TESTING

TLP or VFTLP ESD testing is an alternative to the fail-or-pass HBM or CDM zapping method [10]. For industrial standard TLP testing shown in Fig. 5, a transmission line is pre-charged and then discharges into DUT. A TLP tester produces a well-defined, well-controlled square waveform pulse with t_r and t_d related to an HBM ESD waveform as in Fig. 6. To make the TLP pulses and HBM ESD waveforms equivalent in terms of the transient ESD behaviors and the energy involved, a TLP tester typically sets t_r = 10ns and t_d = 100ns. TLP testing is generally non-destructive because the pulse can be well-controlled. During TLP testing, a series of square waveforms (i.e., a pulse train) are produced to stress the DUT with the pulse height starting very low and increasing gradually at a selected voltage step. After each stressing TLP pulse, the current and voltage of the DUT will be obtained, and the I_{leak} of DUT will be monitored. When an TLP pulse reaches to certain high level, ESD failure will occur, which typically corresponds to an abrupt jump in the DUT leakage. Fig. 7 depicts conceptually the whole TLP stressing flow. After each TLP pulse stress, the oscilloscope captures the voltage and current of the DUT, hence producing an instantaneous ESD discharging I-V curve for the DUT under TLP ESD stressing, which provides details for TCAD ESD simulation calibration. The observed I and V waveforms for DUT during TLP stressing contain both incident and reflected waves that are superimposed after a time delay, hence resulting in varying shapes in the I and V waveforms monitored as depicted in Fig. 7. Since the actual waveform shapes (i.e., the top) of the current and voltage waves captured by the oscilloscope are not flat, a TLP tester is designed to take the average I and V values by integrating the observed I and V waves within a small pulse window (typically 70% - 90%) in time domain as indicated by the vertical dash-lined segment in Fig. 7b. The similar testing procedure applies to VFTLP ESD stressing measurement for CDM ESD characterization where the key difference is that a VFTLP pulse is ultrafast (t_r ∼ 0.1ns) and very short (t_d ∼ 1ns), which is illustrated in Fig. 8.

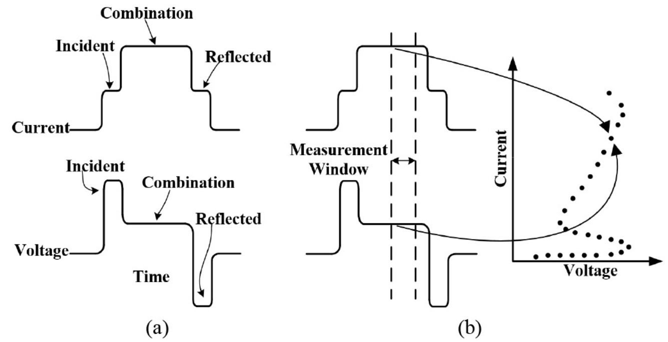

FIGURE 7. Illustration of standard TLP testing procedure shows incident and reflected I and V waveforms, as well as the combined I and V waves across DUT: (a) Incident and reflected pulses, and (b) superimposed I and V waves and the instantaneous ESD discharging I-V curve obtained.

In this work, the TLP tester used is Barth 4002 TLP model and the VFTLP tester used is Barth 4012 VFTLP+ model.

IV. MIXED-MODE MULTI-STIMULI TCAD ESD SIMULATION

A. HBM AND TLP ESD SIMULATION

Impacts of HBM and TLP ESD input stimuli on TCAD ESD simulation was studied using several ESD protection structures. Fig. 9 shows a shallow-trench-isolated (STI) ESD protection diode and a silicon-controlled rectifier (SCR) ESD protection device fabricated in 28nm bulk CMOS, and

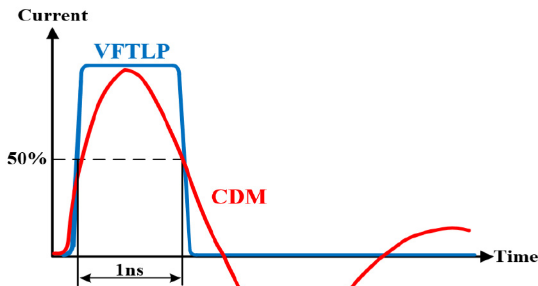

FIGURE 8. Correlating VFTLP and CDM waveforms.

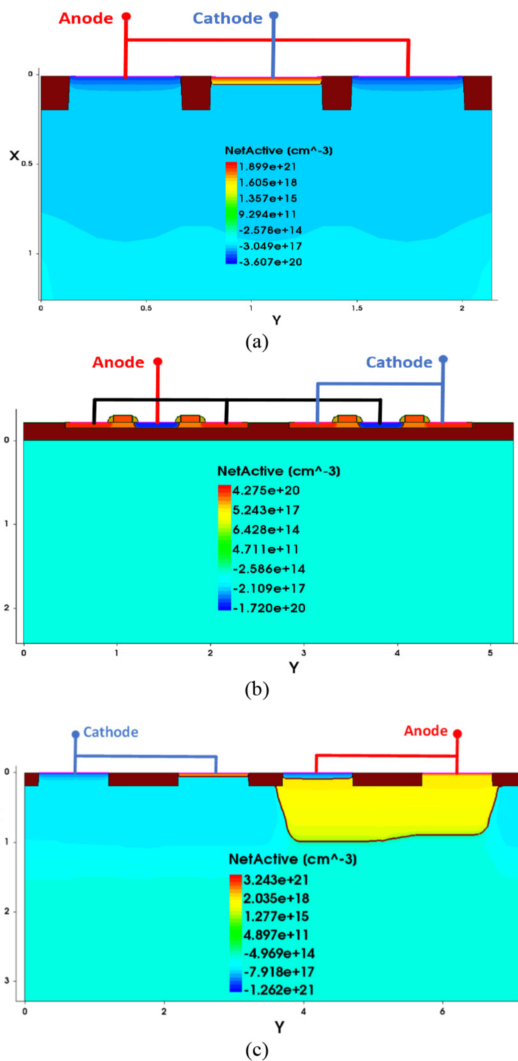

FIGURE 9. Cross-section views for the ESD protection structures in this work by TCAD: (a) A STI ESD protection diode, (b) a diode-string ESD protection structure, and (c) a SCR ESD protection structure.

a diode-string ESD protection structure fabricated in 45nm SOI CMOS. These ESD protection devices were designed using TCAD ESD simulation.

These fabricated ESD protection devices were characterized using a TLP tester, which was compared with TCAD ESD simulation using different ESD stimuli. For comprehensive and fair comparison, mixed-mode TCAD ESD simulation for these ESD protection devices were conducted using three different ESD input waveforms as depicted in Fig. 10: a single-pulse TLP square waveform, a single-pulse HBM waveform (real-world ESD pulse) and a square-waveform TLP pulse train (used in standard TLP testers). The single-pulse HBM ESD waveform corresponds to real-world HBM zapping event and the TLP pulse train models the industrial standard TLP tester. For typical HBM ESD zapping, a 1KV HBM ESD pulse delivers a peak ESD current of $I_{peak}\sim0.66A$ and a 2KV HBM waveform produces $I_{peak}\sim1.32A$ to stress the DUT. For equivalent ESD triggering speed and ESD-associated energy, the TLP pulses use $t_r\sim10ns$ and $t_d\sim100ns$, corresponding to HBM ESD waveform of $t_r\sim10ns$ and $t_d\sim150ns$. For TCAD ESD simulation, the ESD failure criterion is the thermal breakdown current (I_{t2}) caused by the maximum lattice temperature (T_{max}) reaching to 1688K in Si, causing Si melting inside an ESD protection device. TCAD ESD simulation provides rich insights on transient ESD discharging behaviors, which are carefully studied. First, Fig. 11 shows that single-waveform HBM ESD simulation predicts an ESD protection level of $I_{t2}\sim1.45A$ (~2.19KV) for the STI ESD protection diode, $I_{t2}\sim1.27A$ (~1.92KV) for the diode-string ESD protection structure and $I_{t2}\sim1.13A$ (~1.72KV) for the SCR ESD protection device under HBM ESD zapping, respectively. Unfortunately, since no HBM ESD zapping tester in our lab, there are no HBM ESD zapping test data to compare with. Second, using a square-waveform TLP pulse train, ESD simulation predicts that $I_{t2}\sim1.22A$ for the STI ESD protection diode, $I_{t2}\sim1.14A$ for the diode-string ESD protection structure and $I_{t2}\sim0.97A$ for the SCR ESD protection device, which match the ESD protection capability results obtained by actual TLP test very well. In fact, the transient ESD I-V curves for the STI ESD protection diode, diode-string ESD protection structure and SCR ESD protection device from both TLP pulse train simulation and

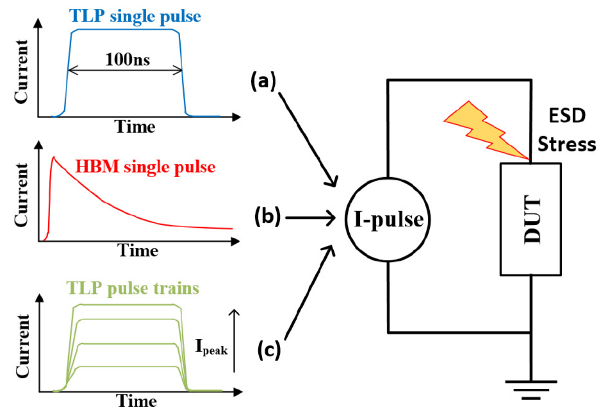

FIGURE 10. New mixed-mode multi-stimuli TCAD ESD simulation set-up uses (a) single-pulse TLP ESD stimulus, (b) single-waveform HBM ESD stimulus, and (c) a square-waveform TLP pulse train ESD stimulus.

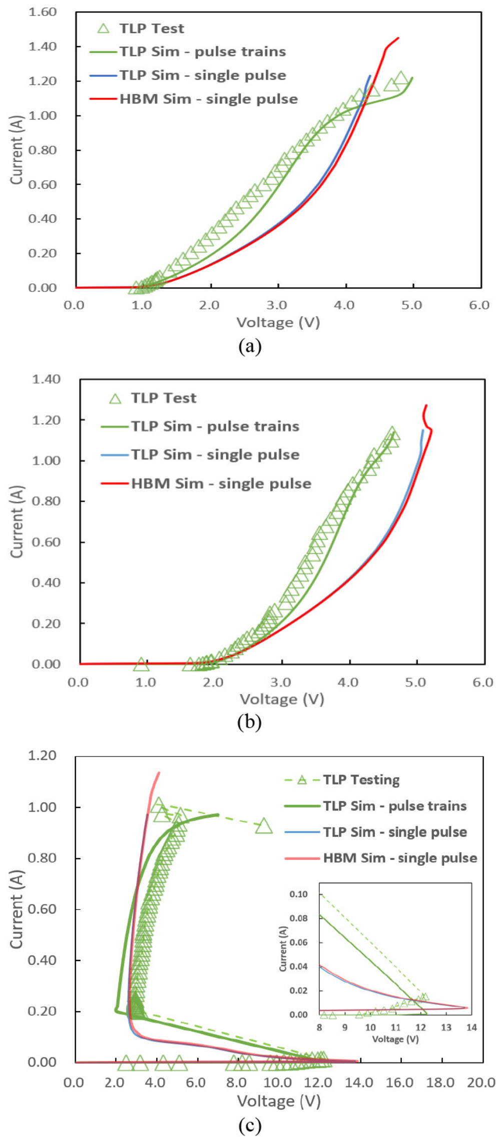

FIGURE 11. Instantaneous ESD discharging I-V curves obtained by TLP ESD testing, and TCAD ESD simulation using single-pulse TLP stimulus, square-waveform TLP pulse train stimulus, and single-waveform HBM ESD stimulus for (a) STI ESD protection diode, (b) diode-string ESD protection structure, and (c) SCR ESD protection device.

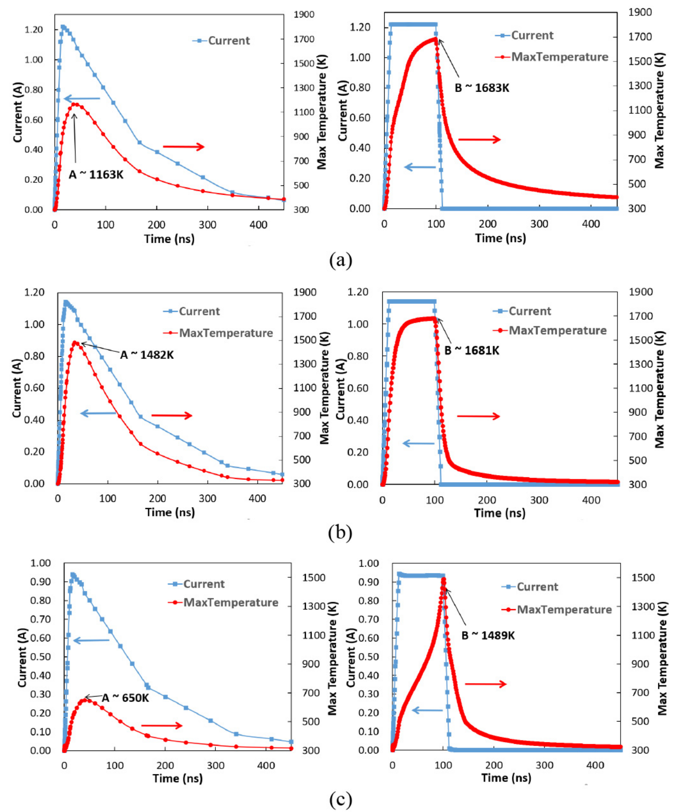

FIGURE 12. Comparison of transient I-t curve (blue) and T_{max}-t curve (red) obtained by single-wave HBM ESD simulation (L) and single-pulse TLP ESD simulation (R) for (a) an ESD protection diode, (b) a diode-string ESD protection structure, and (c) a SCR ESD protection device.

TLP testing agreed with each other very well for the whole ESD discharging I-V curves. In the SCR ESD protection device, the TLP pulse train ESD simulation accurately predicts the trigger voltage of $V_{t1}\sim 12.2V$ and turn-on resistance of $R_{on}\sim 3.3\Omega$ in TLP testing. This clearly states that well-calibrated TCAD ESD simulation using square-waveform TLP pulse trains as ESD stimuli can be used to evaluate TLP ESD testing results. However, it is critical to understand that TLP testing is different from real-world HBM zapping, which is always required for rating the ESD protection for IC products. Unfortunately, the ESD I_{t2} results from TLP pulse train ESD simulation is very different from that of single-pulse HBM ESD waveform simulation. On the other hand, the entire transient ESD discharging I-V characteristics obtained from single-pulse TLP simulation and single-waveform HBM ESD simulation match each other very well, except for the clear difference in I_{t2}. Meanwhile, the full ESD discharging I-V curve obtained by single-pulse TLP simulation is very different from that from both square-wave TLP pulse train simulation and TLP testing, even though the I_{t2} results agree with each well. Table 1 summarizes the ESD protection levels (I_{t2}) obtained from TLP ESD testing and TCAD ESD simulation, which clearly shows the difference. The comparison clearly suggests that one has to be cautious in using TCAD ESD simulation to predict actual ESD protection design performance. Third, to further understand the difference in single-wave HBM and single-pulse TLP ESD simulation, the time-domain dynamic ESD discharging behaviors are examined in details, including the transient T_{max}-t and I-t characteristics for the ESD protection devices as shown in Fig. 12. In ESD simulation, the resulting I_{peak} from both single TLP pulse and single HBM waveform simulation are almost same, i.e., $I_{peak}\sim 1.22A$ for STI ESD protection diode, $I_{peak}\sim 1.14A$ for the diode-string ESD protection structure and $I_{peak}\sim 0.97A$ for SCR ESD protection device. However, the T_{max} from single-pulse TLP simulation is much higher than that from single-waveform HBM ESD simulation for all ESD protection devices. It is

TABLE 1. HBM and TLP ESD I_{t2} comparison.

	SIM: single HBM pulse	SIM: single TLP pulse	SIM: TLP pulse train	TLP Test (pulse train)
STI Diode	1.45A	1.22A	1.22A	1.22A
Diode String	1.27A	1.14A	1.14A	1.14A
SCR	1.13A	0.97A	0.97A	0.97A

observed that, using single-wave HBM stimuli, T_{max} curve generally follows the transient ESD discharging I-curve in t-domain with a slight delay at the peak (labeled point-A). While for single-pulse TLP stimulus ESD simulation, T_{max} is not only much higher, it also stays high for a long period of ~100ns corresponding to the flat waveform top segment of the single TLP square pulse. This means that more significant heat generation and accumulation exist for the ESD protection devices under single-pulse TLP stressing compared to under single-wave HBM zapping. This further suggests that, while TLP testing provides useful ESD discharging behavioral information, one should be very cautious in using TLP results, both from testing and simulation, to predict the actual HBM zapping results. Fourth, Fig. 11 shows that the R_{ON} of the ESD protection devices under TLP pulse train simulation is different from that obtained by single-waveform HBM ESD simulation. Further, V_{t1} of the SCR ESD protection device by TLP pulse train simulation and testing is smaller than that from ESD simulation using single HBM waveform, which is likely attributed to the fact that in both TLP pulse train ESD simulation and TLP testing (also using pulse train), the instantaneous ESD discharging I-V curves for DUT are obtained by an integration within a later 70%-90% window of the whole square waveform duration, excluding any possible overshoot often observed in ESD discharging (Fig. 13); however, in single-wave HBM ESD simulation and real-world HBM zapping test, the whole HBM waveform, including all possible overshoot and the waveform tail, are included in the calculation for obtaining the instantaneous I and V values during HBM ESD stressing. This is a major difference that may cause discrepancy in ESD simulation and testing in practical ESD protection designs.

From the above analysis, it is clear that while TCAD ESD simulation is very useful, TCAD ESD simulation using an ESD stimulus of a single-wave HBM waveform, a single-pulse TLP waveform, or a square-waveform TLP pulse train alone, is rather insufficient in accurately correlating with TLP testing and predicting real-world HBM zapping results. A mixed-mode multi-stimuli TCAD ESD simulation method using combined HBM and TLP pulse train as ESD stimuli is critical to accurately predict ESD protection designs.

B. CDM AND VFTLP ESD SIMULATION

Similar to the HBM and TLP simulation discussed earlier, the same approach was applied to study the impacts of CDM and VFTLP input stimuli on TCAD ESD simulation using an ESD protection diode fabricated in a foundry 45nm SOI CMOS technology which is shown in Fig. 14. Mixed-mode

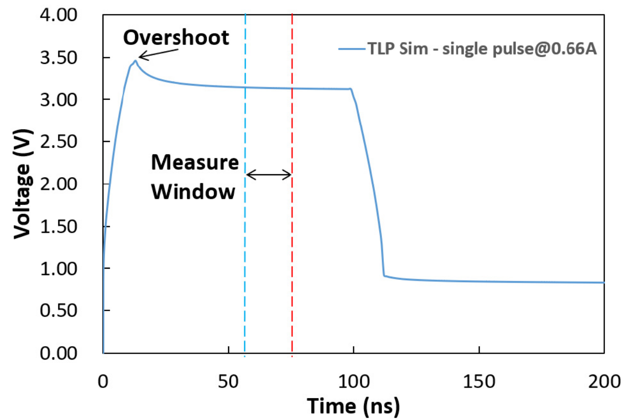

FIGURE 13. Single-pulse TLP simulation for an ESD protection diode shows an overshoot typically occurring, which is outside the 70%-90% integration window in obtaining the transient ESD discharging I-V curve during TLP testing. This contribute to errors in estimating the I and V values.

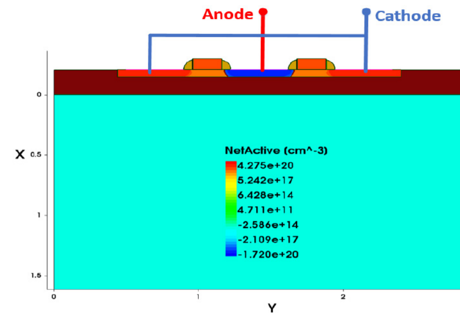

FIGURE 14. Cross-section for an ESD protection diode fabricated in 45nm SOI CMOS.

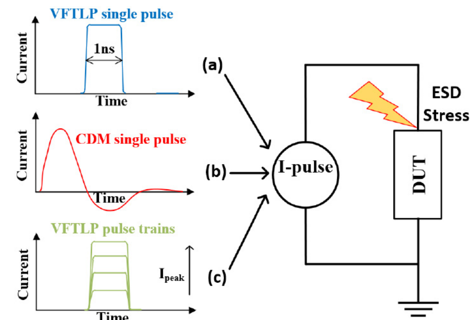

FIGURE 15. New mixed-mode multi-stimuli TCAD ESD simulation set-up uses single VFTLP pulse, single CDM ESD waveform and a VFTLP pulse train as the ESD input stimulating signal.

TCAD ESD simulation was conducted using three different ESD input waveforms as depicted in Fig. 15: single-pulse VFTLP square waveform, single-pulse CDM waveform and a square-waveform VFTLP pulse train. The fabricated ESD diode was characterized using a VFTLP tester.

The CDM ESD waveform used in this work follows the ESDA CDM ESD standard [8], where a 50V CDM pulse has I_{peak}~0.72A. Similar to TLP, for equivalent CDM ESD triggering speed and ESD energy, the VFTLP pulses use t_r~0.1ns and t_d~1ns. First, Fig. 16 shows that

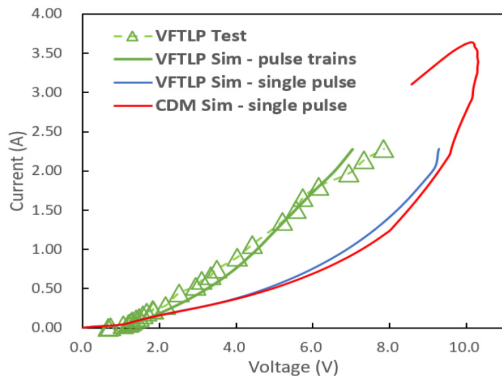

FIGURE 16. Instantaneous CDM ESD discharging I-V curves for an ESD protection diode made in 45nm SOI CMOS obtained from VFTLP testing (pulse train) and TCAD ESD simulation using single-pulse VFTLP stimulus, single-waveform CDM stimulus and a VFTLP pule train.

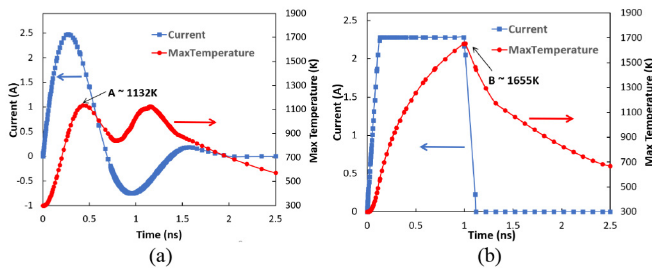

FIGURE 17. Comparison of transient I-t curve (blue) and T_{max}-t curve (red) obtained by (a) single-waveform CDM ESD simulation, and (b) single-pulse VFTLP ESD simulation, for an ESD protection diode made in a 45nm SOI CMOS.

CDM ESD simulation predicts an ESD protection level of I_{t2}~3.5A (~240V) for the ESD protection diode made in 45nm SOI CMOS. Unfortunately, since there is no CDM zapping tester in our Lab, CDM ESD simulation could not be compared with CDM zapping test. Second, square-waveform VFTLP pulse train ESD simulation predicts that I_{t2}~2.28A for the ESD protection diode, which match well with VFTLP testing. In fact, the transient ESD discharging I-V characteristics for both VFTLP pulse train simulation and VFTLP testing match each other very well for the whole CDM ESD discharging I-V curves. This again suggests that well-calibrated TCAD ESD simulation using VFTLP pulse trains as stimuli can be used to evaluate VFTLP testing results. However, it is noteworthy that VFTLP testing is actually different from CDM zapping and may not be used to predict real-world CDM ESD zapping results. It is further observed that the ESD discharging I-V curves by single-pulse VFTLP simulation and single-waveform CDM ESD simulation agree with each other nicely, except for difference in the I_{t2} results. On the other hand, the I_{t2} of single-pulse VFTLP simulation also matches that of VFTLP testing well, but their ESD discharging I-V characteristics are very different. Table 2 summarizes the ESD I_{t2} results extracted from VFTLP testing and TCAD ESD simulation

TABLE 2. CDM and VFTLP ESD I_{t2} comparison.

	SIM: single CDM pulse	SIM: single VFTLP pulse	SIM: VFTLP pulse train	VFTLP Test (pulse train)
Diode	3.5A	2.28A	2.28A	2.28A

using different ESD stimuli, which clearly shows the difference in between. Third, because the CDM and VFTLP ESD tests differ significantly, correlating the two results is much more difficult than doing so for HBM and TLP measurements [11]. To further understand the difference in CDM and VFTLP ESD simulation, time-domain ESD discharging behaviors are studied in details, including the transient T_{max}-t and I-t characteristics for the ESD diode as given in Fig. 17. In CDM ESD simulation, the resulting I_{peak} from both single-pulse VFTLP and single-waveform CDM stressing are almost same, with I_{peak} ~ 2.28A for the ESD protection diode in 45nm SOI. However, the T_{max} under single-pulse VFTLP stimulus is much higher than that obtained by using a CDM ESD stimulus. It is observed that, for single-waveform CDM ESD simulation, T_{max} curve generally follows the transient CDM ESD waveform in t-domain with a slight delay at the peak (labelled point-A). Also, there is a second peak of the T_{max} after the I-curve oscillates into the negative cycle. This is because as the real-world CDM waveform is oscillatory featuring strong first and substantial second peaks; however, the VFTLP waveforms are single-directional square waveforms. However, in single-pulse VFTLP simulation, T_{max} is not only much higher, but also stays high for the most period of ~1ns of the VFTLP square waveform. This translates into more heat generation and accumulation within the ESD protection devices under VFTLP pulse stressing compared to during CDM zapping. This again states that, while VFTLP ESD simulation and testing provides useful ESD discharging information, one should be very cautious in not over-interpreting the VFTLP results aiming to accurately predict actual CDM ESD protection performance. Fourth, similar to TLP case, commercial VFTLP testers take a data integration across the later 70%-90% window of the DUT voltage and current waveforms obtained during VFTLP ESD stressing to estimate the instantaneous I and V values to construct the dynamic ESD discharging curves. This VFTLP testing mechanism most likely misses the unavoidable overshoot during VFTLP characterization. On the other hand, using CDM ESD waveform can catch such overshoots. Therefore, the procedures of VFTLP stressing and CDM ESD zapping also contribute to the discrepancies in VFTLP and CDM ESD characterization in both simulation and testing.

V. CONCLUSION

No existing ESD simulation techniques may precisely predict practical ESD protection designs universally yet. This paper reports a comprehensive and comparison study of impacts of various ESD input stimuli on transient ESD discharging behaviors in TCAD ESD simulation in comparison with

ESD testing. Experiment and simulation of various ESD protection devices made in 28nm CMOS and 45nm SOI CMOS, using TLP and VFTLP ESD testing, and TCAD ESD simulation using single-waveform HBM/CDM ESD stimuli, single-pulse and pulse-train TLP/VFTLP ESD stimuli, clearly show that differences in ESD discharging characteristics exist in these ESD evaluation methods. Therefore, one must be cautious not over-interpreting TCAD ESD simulation details, obtained using any specific/individual ESD stimulus, to attempt to precisely predict practical ESD protection designs, as well as to correlate TLP/VFTLP stressing with HBM/CDM ESD zapping measurements. It concludes that it is important to use a mixed-mode multiple-stimuli ESD simulation method in meaningfully and accurately characterizing ESD protection designs, as well as for ESD design prediction and validation.

REFERENCES

[1] A. Wang, *On-Chip ESD Protection for Integrated Circuits*. Boston, MA, USA: Kluwer, 2002.

[2] A. Z. H. Wang *et al.*, "A review on RF ESD protection design," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1304–1311, Jul. 2005, doi: 10.1109/TED.2005.850652.

[3] H. Feng *et al.*, "A mixed-mode ESD protection circuit simulation-design methodology," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 995–1006, Jun. 2003, doi: 10.1109/JSSC.2003.811978.

[4] T. Cilento *et al.*, "Simulation of ESD protection devices in an advanced CMOS technology using a TCAD workbench based on an ESD calibration methodology," *Microelectron. Rel.*, vol. 50, pp. 1367–1372, Sep.–Nov. 2010.

[5] C. Wang *et al.*, "A comparison study of DTSCR by TCAD and VFTLP for CDM ESD protection," in *Proc. IEEE Int. Symp. Phys. Failure Anal. ICs (IPFA)*, Chengdu, China, 2017, pp. 1–4, doi: 10.1109/IPFA.2017.8060146C.

[6] M. Di, Z. Pan, C. Li, and A. Wang, "A new multi-stimuli-based simulation method for ESD design verification," in *Proc. IEEE Electron Devices Technol. Manuf. Conf. (EDTM)*, Chengdu, China, 2021, pp. 4–6, doi: 10.1109/EDTM50988.2021.9420890.

[7] *Electrostatic Discharge Sensitivity Classification, Method 3015.7*, Standard MIL-STD-883E, 1989.

[8] *ESDA and JEDEC ANSI/ESDA/JEDEC Standard for Electrostatic Discharge Sensitivity Testing, Charged Device Model (CDM)—Device Level*, Standard JS-002-2014, 2014.

[9] M. Di, C. Li, Z. Pan, and A. Wang, "Pad-based CDM ESD protection methods are faulty," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 1297–1304, 2020, doi: 10.1109/JEDS.2020.3022743.

[10] T. Maloney, "Transmission line pulsing techniques for circuit modelling of ESD phenomena," in *Proc. EOS/ESD Symp.*, 1985, pp. 49–54.

[11] Y. Xue, "Correlation of very fast transmission line pulse (VFTLP) and field-induced charged device model (CDM) testing," in *Proc. IEEE IPFA*, Singapore, 2012, pp. 1–3, doi: 10.1109/IPFA.2012.6306309.