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Effect of the Blocking Oxide Layer With Asymmetric Taper Angles in 3-D NAND Flash Memories

JUN GYU LEE[1], WOO JE JUNG[1], JAE HYEON PARK[1], KEON-HO YOO[2], AND TAE WHAN KIM[1]

1 Department of Electronics and Computer Engineering, Hanyang University, Seoul 04763, South Korea
2 Department of Physics, Research Institute for Basic Sciences, Kyung Hee University, Seoul 02447, South Korea

CORRESPONDING AUTHOR: T. W. KIM (e-mail: twk@hanyang.ac.kr)

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ABSTRACT The tapered channel effect is a major concern in three-dimensional (3-D) NAND technology because the effect causes differences in the electrical characteristics, including the threshold voltage (V_T), between the upper and the lower cells. We simulated the tapered channel effect by using Sentaurus technology, computer-aided design (TCAD) tools, and based on the results, we propose a novel method to lessen the non-uniformity of the threshold voltage shift (ΔV_T) between the cells. The difference in ΔV_T between the upper and the lower cells due to the tapered channel can be reduced by employing a tapered blocking oxide layer with a proper taper angle. These results will be helpful in designing reliable 3-D NAND flash memories.

INDEX TERMS 3-D NAND flash memories, threshold voltage shift, tapered channel.

I. INTRODUCTION

Two-dimensional (2-D) flash memory technologies have faced physical limitations due to the shrinking problem of NAND flash memories [1], [2]. To overcome these limitations, researchers have introduced various types of flash memory devices [3]. NAND technology currently uses a three-dimensional (3-D) structure and polysilicon as the channel material [4]. However, when implementing multi-level technology and high-rise stacking technology to enhance efficiency, several factors affect the variability of 3-D NAND flash memories, and these factors can be classified into three categories [5]: the effect of grain boundary traps [6]–[9], fluctuations in the control of the critical dimension [10], and the effect of the tapered channel [11]–[13]. Among these factors, the taper angle and the mold height are major reasons for the string performance differences between the top and the bottom cells as the number of cells is increased. Therefore, the differences in the electrical characteristics due to the tapered channel effect must be minimized. Even though much research has focused on the effects of the number of layers and the taper angle on the electrical characteristics [11], [12], few investigations have been performed to compensate for the shortcomings of tapered channels [13]. The tapered channel effect can be compensated by applying a different program voltage, but has the disadvantage of increasing peripheral circuit complexity.

This paper provides data on the electrical characteristics of 3-D NAND flash memories as simulated by using Sentaurus technology, computer-aided design (TCAD) tools. Simulations were performed by applying different taper angles only at the interface between the blocking oxide layer and the gate. We propose optimal etching profiles that can improve the uniformity of the electrical characteristics between cells were proposed, and we discuss the reasons for changes in the threshold voltage shift (ΔV_T) due to changes in the etching profile.

II. SIMULATION DETAILS

Figure 1 shows the simulated device based on the "gate-first," gate-all-around (GAA), vertical-channel method [14] with a macaroni channel structure. The device consists of 16 memory cells, a string select gate (SSG), and a ground select gate (GSG). The top channel's radius is fixed at 80 nm, and the taper angle is defined as the angle relative to the

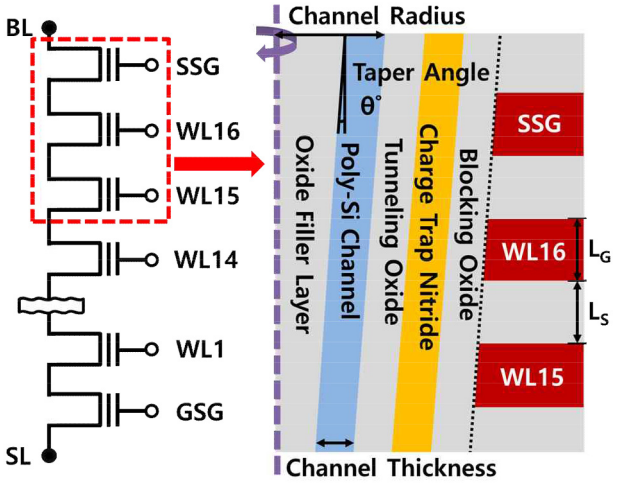

FIGURE 1. Cross-sectional diagram of the simulated 3-D NAND flash memory device.

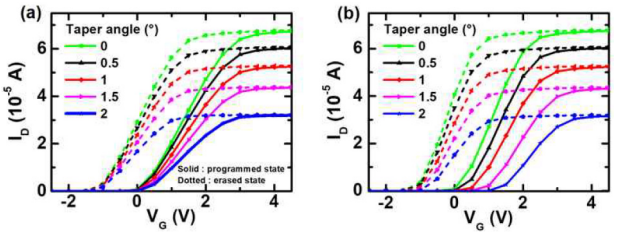

FIGURE 2. I_D-V_G characteristics in the programmed state (solid line) and the erased state (dotted line) of (a) the top cell and (b) the bottom cell at various taper angles.

vertical axis as shown in Figure 1. Taper angles are set at 0, 0.5, 1, 1.5 and 2° [3]. As the taper angle is increased, the channel radius of the bottom cells decreases. The thicknesses of channel layer, the tunneling oxide layer, the charge trap nitride layer, and the blocking oxide layer are 20, 5, 7, and 7 nm, respectively. Cells are regularly arranged with a spacer length (L_S) of 40 nm and a gate length (L_G) of 40 nm. The gate material is tungsten. We use poly-silicon channels without grain boundary traps to consider only the tapered channel effect. The source-line (SL) voltage, the bit-line (BL) voltage, the program voltage and the pass voltage of the cells are 0, 1, 15, and 8 V, respectively, and the control gate voltage (V_G) of the target cell is swept from −3 to 5 V. Electron and hole non-local tunneling models are applied both to the interface between the channel/tunneling oxide and the gate/blocking oxide during device operation; the Poole-Frenkel emission model is also considered.

III. RESULTS AND DISCUSSION

Figure 2 shows the drain current as a function of the gate voltage (I_D-V_G) in the programmed/erased state of (a) the top cell and (b) the bottom cell at various taper angles. The threshold voltage V_T is defined as the gate voltage V_G when I_D reaches 1×10^{-6} A. As the taper angle is increased, the value of I_D, which is greater in the lower cells than in the

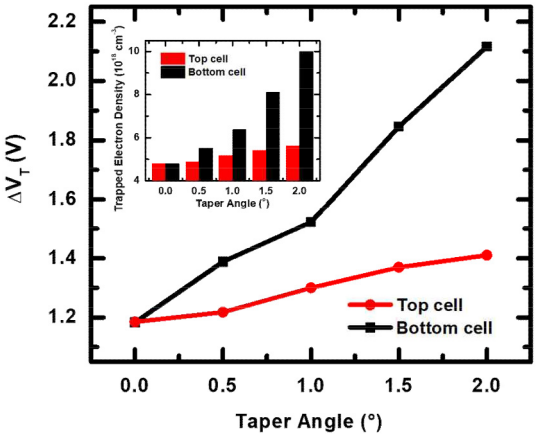

FIGURE 3. ΔV_T as a function of the taper angle according to the cell's position. The inset shows the density of electrons trapped in the nitride layer during the programming operation in the top cell and the bottom cell at various taper angles.

upper cells, tends to decrease, resulting in a large V_T. Our previous study showed that I_D decreased due to an increase in the resistance as the channel's radius was decreased [11]. However, the change in resistance induced by the change in the channel's radius does not fully account for the large V_T difference, which depends on the cell's position.

The threshold voltage shift ΔV_T is defined by V_T in the programmed state minus V_T in the erased state. Figure 3 shows ΔV_T as a function of the taper angle according to the cell's position. ΔV_T increases with increasing taper angle more rapidly in bottom cells than in top cells. This is because the smaller the channel radius, the stronger the programming electric field, resulting in more trapped charges in the nitride layer. As can be seen in the inset of Fig. 2, increasing the taper angle increases the difference in the density of electrons trapped in the nitride layer during the programming operation between the top cell and the bottom cells. The change in ΔV_T is mostly due to the change in the value of V_T in the programmed state.

Figure 4 shows a cross-sectional diagram for the tapered blocking oxide layer introduced to compensate for ΔV_T differing with cell position. We define the taper angle applied to all interfaces except the interface between the blocking oxide layer and the gate as the 'taper angle θ'. The other taper angle applied to the interface between the blocking oxide layer and the gate is expressed as the 'outer taper angle θ_1'. The thickness of the blocking oxide adjacent to the SL at the bottom is fixed at 7 nm and decreases toward the upper cell. In the simulation, θ_1 is decreased from θ in 0.02° steps for each taper angle θ, and the optimal angle θ_1 is sought by changing θ_1 until $(\theta - \theta_1)$ is equal to 0.14.

The difference in ΔV_T between the top and the bottom cells ($\Delta V_{T\_top\ cell} - \Delta V_{T\_bottom\ cell}$) is denoted by $\sigma(\Delta V_T)$. Figure 5 shows $\sigma(\Delta V_T)$ as a function of $(\theta - \theta_1)$ at various taper angles. For a taper angle of 2°, $|\sigma(\Delta V_T)|$ has a minimum at a specific angle $(\theta - \theta_1)$. For other taper angles,

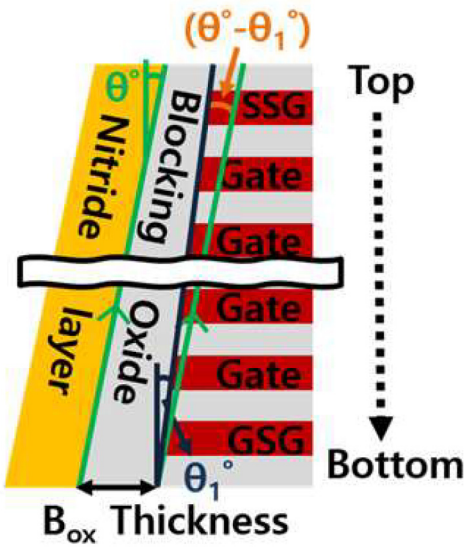

FIGURE 4. Cross-sectional diagram for the tapered blocking oxide layer introduced to compensate for the variation in ΔV_T with cell position.

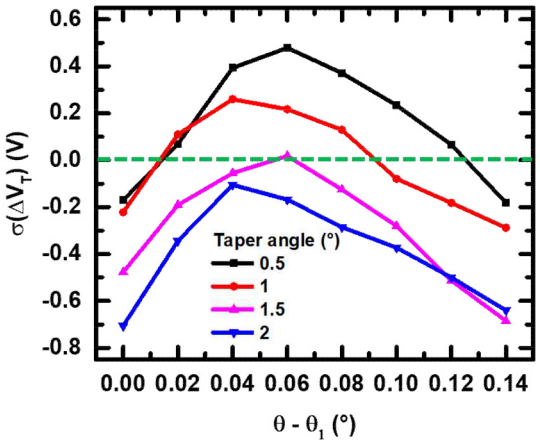

FIGURE 5. $\sigma(\Delta V_T)$ as a function of $(\theta - \theta_1)$ at various taper angles.

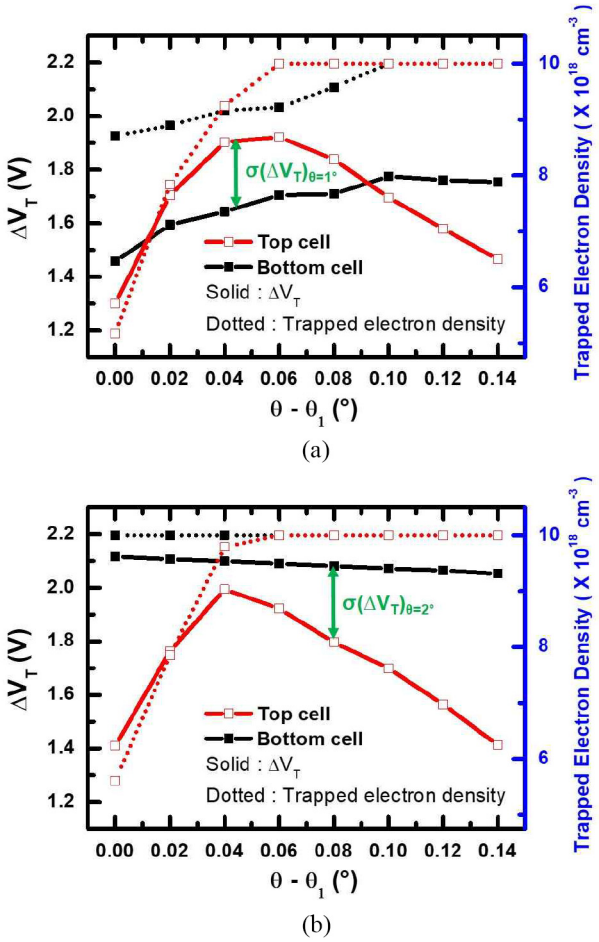

FIGURE 6. (a). ΔV_T (left Y-axis) and trapped electron density (right Y-axis) as a function of $(\theta - \theta_1)$ for a taper angle of 1°. (b). ΔV_T (left Y-axis) and trapped electron density (right Y-axis) as a function of $(\theta - \theta_1)$ for a taper angle of 2°.

$|\sigma(\Delta V_T)|$ has two minimum values; i.e., the $\sigma(\Delta V_T)$ curve crosses the $\sigma(\Delta V_T) = 0$ line twice. In order to understand these different behaviors, we looked into the various ΔV_T's contributing to $\sigma(\Delta V_T)$ for taper angles of 1° and 2°.

Figure 6(a) shows ΔV_T (left Y-axis) and trapped electron density (right Y-axis) as functions of $(\theta - \theta_1)$ for a taper angle of 1°. For small $(\theta - \theta_1)$, the trapped electron density is a major factor in determining ΔV_T. As $(\theta - \theta_1)$ increases, the density of electrons trapped in the nitride increases and ΔV_T increases. However, when $(\theta - \theta_1)$ is larger than a certain value, the density of electrons trapped in the nitride layer converges to 1×10^{19} cm^{-3}, but ΔV_T tends to decrease. This phenomenon can be explained in terms of fringing fields [15]. The fringing field induced by the pass voltage forms an inversion layer providing a "read" function. The read voltage is applied large enough to form an inversion layer even in the programmed state, so V_T in the erased state is almost unchanged. As $(\theta - \theta_1)$ increases, the corresponding thinner blocking oxide layer yields a higher fringing field between the gates. As a result, V_T in the programmed state is lower and ΔV_T decreases accordingly. The decrease in ΔV_T of the bottom cell is slightly smaller than that of the top cell, because the blocking oxide layer is relatively thicker in the bottom cell than the top cell and the fringing field is weaker. Figure 6(b) is for a taper angle of 2°. ΔV_T of the top cell at the taper angle of 2° shows a trend similar to that of the taper angle of 1°. However, for the bottom cell the taper angle of 2°, ΔV_T tends to decrease as $(\theta - \theta_1)$ increases because the cell's nitride layer is fully trapped even when $(\theta - \theta_1)$ is 0°.

IV. CONCLUSION

We investigated the electrical characteristics of 3-D NAND flash memory devices with a tapered channel. The tapered channel effect can be understood as a change in the density of trapped electrons with changing channel radius. To minimize $|\sigma(\Delta V_T)|$, the difference in ΔV_T between the upper cells and the lower cells due to the tapered channel, we propose the use of a tapered blocking oxide layer with a different taper

angle. For each taper angle of the channel, the uniformity of ΔV_T is greatly improved at the optimum taper angle for the blocking oxide layer. These results indicate that the introduction of a designed blocking oxide can improve the uniformity of the electrical characteristics between cells.

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