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Simultaneous Analysis of Multi-Variables Effect on the Performance of Multi-Domain MFIS Negative Capacitance Field-Effect Transistors

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ABSTRACT With the simulation calibration for negative capacitor considering Landau model and multi-domain (MD) effect, MD MFIS negative capacitance field-effect transistor (NCFET) was thoroughly established for performing the simultaneous analysis of multi-variables (ferroelectric layer thickness (T_{FE}), oxide layer thickness (T_{OX}) and gate length (L_g)) effect on the device performance. In this study, subthreshold swing (*SS*) and hysteresis properties of MD-MFIS-NCFET were demonstrated by employing TCAD simulation tool. Compared with the previous reported study on single variable effect based on single-domain (SD) NCFET, the simultaneous analysis of multi-variables effect on MD-NCFET enabled to obtain better device performance and generate more comprehensive results. Convincing models were established based on the experimental data by calibration. Demonstration on the basic simulated results including the lowering *SS* mechanism and the multi-variables effect on MD-NCFET performance was completely presented based on the capacitance matching theory and short channel effect. With the optimal T_{FE} and T_{OX}, a trade-off mechanism between the *SS* and L_g was shown with the consideration of L_g scaling. Noticeable in-depth study in association with the simultaneous analysis of the multi-variables effect was carried out, indicating that the hysteresis-free *SS* obtained by simultaneous analysis of multi-variables was lower than that obtained by single-variable analysis. Final validation results demonstrate that the optimization proposed in this work by considering the multi-variable effect shows high compatibility with other NCFET devices, providing an instructive strategy for the high-performance NCFET optimization.

INDEX TERMS NCFET, capacitance matching, multi-domain, TCAD.

I. INTRODUCTION

As the subthreshold swing (*SS*) of the traditional MOSFETs faces difficulty to fall below 60 mV/dec at room temperature due to the physical limitation of the Boltzmann tyranny [1], Moore's law is increasingly being challenged. Therefore, alternative electronic devices have been explored for achieving sub-60 mV/dec in ultralow voltage operation. There is clear evidence that negative capacitance field-effect transistor (NCFET) enables the *SS* below 60 mV/dec through internal voltage amplification [2]–[4]. Up to now, numerous studies have explored different approaches to achieve NCFETs with lower *SS* and free hysteresis, such as doping in ferroelectric materials [5], negative capacitance ring structure [6] and using oxide charge trapping layer [7]. It is noticeable that many studies concentrate on capacitance matching and have achieved better NCFET performance [8]–[10]. Recently, capacitance matching is considered in terms of the structural parameters, including ferroelectric layer thickness (T_{FE}) and oxide layer thickness (T_{OX}), in order to obtain better electrical properties of NCFET [11]–[13]. However, most reported studies only discussed single-variable effect on the NCFET devices that based on single-domain (SD) model with the uniform distribution of polarization in ferroelectric layer. Recently, the study on the ferroelectric materials with multi-domain (MD) state

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has also been reported by considering that the polarization intensity direction of each position in the ferroelectric layer is not in consistence, which is more reasonable with the actual ferroelectric material properties [14]. Nevertheless, the simulation of MD-NCFET devices is still rarely reported. In this work, considering the simultaneous change in multi-variables, such as T_{FE}, T_{OX} and gate length (L_g), the MD model was employed to investigate the NC effect and MD-MFIS-NCFET characteristics, which could provide a further comprehensive guidance for the future design procedure.

In the present study, ferroelectric parameters were firstly extracted from the experimental data of the capacitor with negative capacitance effect (NCCAP) by transient NC characteristics fitting. With the ferroelectric parameters, MD model for the ferroelectric capacitor was developed. Based on the calibration for the NCCAP and the non-ferroelectric field-effect transistor (non-FeFET), a MD-MFIS-NCFET was developed with Sentaurus TCAD simulation tool. The simulation that focused on the variation of the *SS* and hysteresis with the change of the structural or electrical parameters including V_g, T_{FE} and T_{OX} was demonstrated by capacitance matching theory from several aspects. Subsequently, the effect of the L_g on the MD-NCFET with optimal capacitance matching was discussed, implying that short channel effect exerted negative impact on the *SS* performance of the MD-NCFET while the *SS* performance could be further enhanced by the scaling of the L_g under capacitance matching. Finally, the simultaneous analysis of multi-variables (T_{OX}, T_{FE} and L_g) on device optimization was presented, obtaining lower hysteresis-free *SS* than that obtained by performing single-variable analysis. Finally, the model validation was presented, which revealed the fact that there was a considered optimization solution in MD-NCFET design. The above results give a thoughtful design guideline for fabricating high-performance NCFETs.

II. MODELING

Regarding the modeling, the ferroelectric parameters of Landau–Khalatnikov (LK) model were extracted from the experimental data for the transient NC effect, and the MD model was adopted to establish the verified soft domain MD-LK NC model. For further investigation of the MD-NC effect, the NC model was combined with the well-calibrated non-FeFET to develop MD-MFIS-NCFET. To acquire accurate parameters of NC model, NCCAP model and its RC_{FE} circuit were developed for transient NC effect calibration based on LK theory [15]–[17]. As shown in the inset of Fig. 1(a), the experimental NCCAP with 10 nm HfZrO (HZO) [18] and its RC_{FE} circuit was adopted for ferroelectric parameters extraction and simulation. The transient model of NCCAP is deduced as:

$$\rho \frac{\partial P}{\partial t} = -\frac{\partial U}{\partial P} \tag{1}$$

where ρ is the viscosity coefficient, P is the ferroelectric polarization and U is Gibb's free energy. Considering the total anisotropic energy and the energy obtained by the external electric field, Gibb's free energy is denoted by:

$$U = \alpha P^2 + \beta P^4 + \gamma P^6 - E_{FE} P \tag{2}$$

where α, β and γ are the expansion coefficients and E_{FE} is the electric field across the ferroelectric layer. According to (1) and (2), E_{FE} is expressed by:

$$E_{FE} = \frac{V_{FE}}{T_{FE}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 + \rho \frac{\partial P}{\partial t} \tag{3}$$

where V_{FE} is the interface voltage of the NCCAP. Based on the electrostatics, P can be written as:

$$P = Q - \epsilon_0 E_{FE} \tag{4}$$

where Q is the free charge density. According to the diagram of the RC_{FE} circuit, the equation based on Kirchhoff's law can be written as:

$$\frac{\partial Q}{\partial t} = \frac{V_{IN} - V_{FE}}{RA} \tag{5}$$

where R is the series resistor in circuit, A is the capacitor area and V_{IN} is the input voltage. According to (3), (4) and (5), the equation for the free charge dynamic can be expressed as:

$$RA \frac{\partial Q}{\partial t} = V_{IN} - \frac{T_{FE}(Q - P)}{\epsilon_0} \tag{6}$$

On this basis, a complete set of transient NC fitting model can be obtained. Fig. 1(a) displays the voltage and charge response for the RC_{FE} circuit. The region circled presents a trend that free charge increases while V_{FE} decreases, which indicates that the NC effect happens in this region. The emergence of NC effect can be further explained in Fig. 1(b), in which the trend of V_{FE} and free charge density in the circuit is shown. Although $\partial Q/\partial t$ is always positive, NC effect occurs when $\partial V_{FE}/\partial t < 0$. Gibb's energy versus the polarization of the NCCAP is illustrated in Fig. 1(c). A two-well energy landscape for the NCCAP is observed, which indicates that the thermodynamic free energy in the ferroelectric layer creates an energy barrier [14]. We performed the experiment-based calibration for the NCCAP with the TCAD tool by fitting transient model with experiment data [18] to extract the ferroelectric parameters. The result of the NCCAP calibration is shown in Fig. 1(d). The simulated *P-V* characteristic curve based on the LK equation presents a reasonable match with the experimental data. Reliable key parameters are listed in Table 1, in which α, β and γ are used to establish the MFIS-NCFET for further study. V_{IN} and R are transient simulation parameters, which are not related to subsequent MFIS-NCFET studies [15].

The extracted ferroelectric parameters above were then used to build MD-MFIS NC model. The MD-MFIS model developed here was adopted to calibrate the soft domain state with typical gradient coefficient (k), which provided feasible and accurate NC model to establish MD-MFIS-NCFET for further study. Considering the MD model, k was adopted to

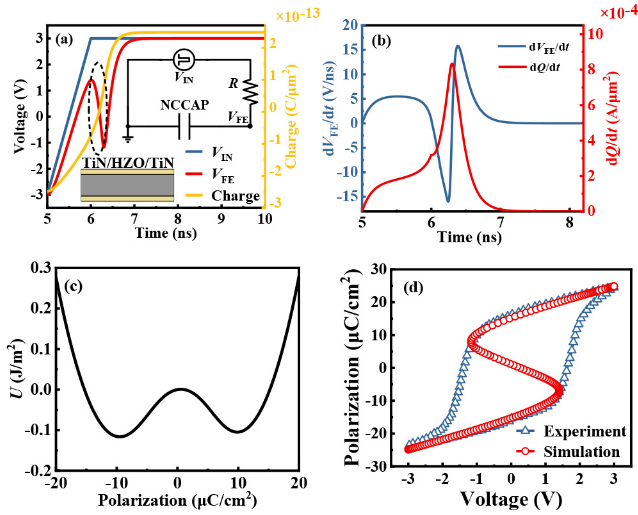

FIGURE 1. (a) The transient response of the NCCAP with the structure and the transient RC_{FE} circuit in the inset, (b) the variation of V_{FE} and Q per unit time as a function of time, (c) thermodynamic free energy profile as a function of polarization and (d) *P-V* calibration for the experimental NCCAP [18].

TABLE 1. Simulation parameters for the NCCAP.

Symbol	Quantity	Value
V_{IN}	Input pulse voltage amplitude	±3 (V)
R	External series resistance	5 (KΩ)
α		-8.2×10^{10} (m/F)
β	Static parameters of LK model	4.2×10^{12} (m^5/C^{2}F)
γ		5×10^{29} (m^9/C^{4}F)

determine the polarization intensity distribution of MD ferroelectric materials in the NC model. The LK model including MD effect is expressed as [14]:

$$E_{FE} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 + \rho \frac{\partial P}{\partial t} - 2k \frac{\partial^2 P}{\partial x^2} \quad (7)$$

The hardness of the NC domain wall of MD exerts great influence on the NC effect. The hard domain will bring undesirable hysteresis effect due to the instability of free energy when polarization intensity is relatively zero, while the soft domain enables to avoid this issue. Smaller k causes the domain walls to stiffen, while the larger k keeps the ferroelectric layer in soft domain state. At present, the determination of k for HZO still remains unclear. Here, the MD-MFIS stack negative capacitor is selected with $T_{FE} = 10$ nm and $T_{OX} = 3$ nm, as shown in Fig. 2(a). The reasonable typical value of $k = 2 \times 10^{-4}$ cm^3/F for HZO is used to establish MD model [19], and the polarization intensity distribution of MFIS structure under the typical value is verified using ferroelectric parameters extracted above to guarantee the status in soft domain, as shown in Fig. 2(b). The occurrence of MD effect with soft domain can be observed, suggesting that the MD-MFIS NC model established in this work can be used to develop MD-MFIS NCFET for further simulation.

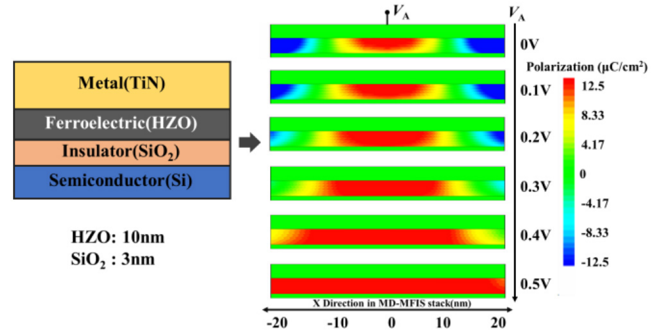

FIGURE 2. (a) Schematic structure and (b) polarization intensity distribution of MFIS stack negative capacitor.

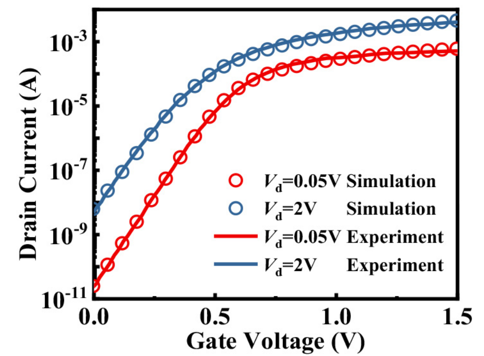

FIGURE 3. Simulation calibration for the baseline device (non-FeFET) with reported experimental data [20].

Fig. 3 shows the simulation calibration for the baseline non-FeFET device with the reported experimental data (Silicon-based NMOS with $L_g = 40$ nm, $T_{OX} = 3$ nm, substrate impurity concentration is 1×10^{18} cm^{-3} and junction depth is 10 nm) [20]. The simulation results for the transfer characteristics were in good agreement with the experimental data at both high and low V_d, providing the accuracy and feasibility of our simulation. Base on the calibration of our simulation for the NCCAP and non-FeFET, the optimization of the MD-NCFET with the MFIS stack was investigated subsequently.

III. RESULTS AND DISCUSSION

Fig. 4(a) shows the schematic structure of the MD-MFIS-NCFET for simulation based the reported experimental data of the NCCAP and non-FeFET [18], [20]. The Si-based MD-MFIS-NCFET built in this work was set with the initial parameters containing L_g (40 nm), junction depth (10 nm), HZO ferroelectric layer (10 nm) and SiO_2 insulator layer (3 nm). The related equivalent capacitance circuit of the MD-MFIS-NCFET is given in Fig. 4(b). V_{int} is the voltage at the oxide layer, which is equivalent to the gate voltage of traditional MOSFET. Obviously, the capacitance circuit can be equivalent to the series of MOS capacitor (C_{MOS}) and ferroelectric capacitor (C_{FE}).

To investigate the effect of T_{FE} on the performance of the MD-NCFET, various T_{FE} was selected. Fig. 5(a) depicts

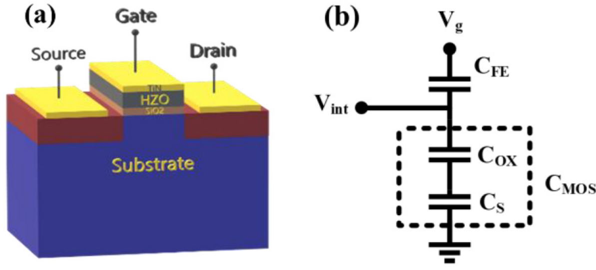

FIGURE 4. (a) Schematic structure of the MD-MFIS-NCFET for simulation and (b) its equivalent capacitance circuit.

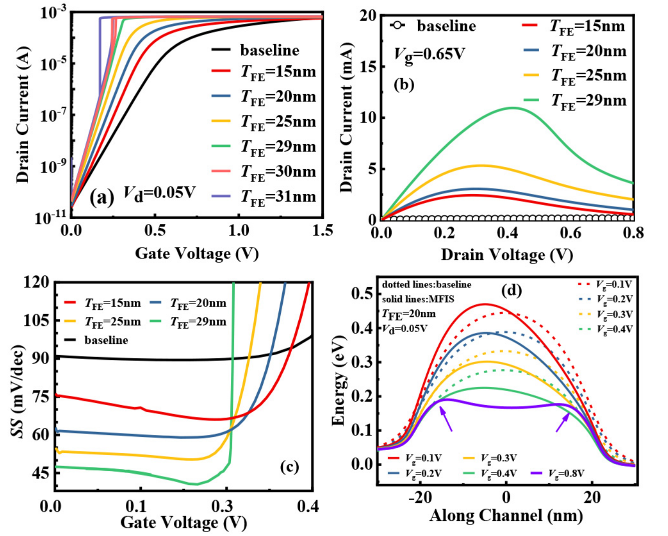

FIGURE 5. (a) Transfer I_d-V_g curves, (b) output I_d-V_d curves, (c) SS-V_g plot of the MD-NCFETs with different T_{FE} and (d) E_c profiles for the baseline non-FeFET and the MD-NCFET with the $T_{FE} = 20$ nm at different V_g.

the transfer $I_d - V_g$ curves at $V_d = 0.05$ V with different T_{FE}. The greater tilt with thicker ferroelectric layer can be observed. It is noticeable that hysteresis-free *SS* reaches lowest value at 40.6 mV/dec when $T_{FE} = 29$ nm. The hysteresis appears when T_{FE} is larger than 29 nm. In the meanwhile, the hysteresis effect becomes more significant as the T_{FE} continues to increase. Additionally, it can be also seen that the hysteresis exhibits abrupt switching, which is commonly found in TCAD simulation [7], [8]. It is worth pointing out that the HZO thickness of 29 nm with hysteresis-free property is not within the range of T_{FE} obtained by most reported experiments. The reason refers to that the T_{OX} of 3 nm here for simulation is the same as that of the baseline device, which is much thicker than that of most experimental devices. In terms of the thinner T_{FE}, the related results will be discussed later. The output I_d-V_d curves in Fig. 5(b) show the negative differential resistance (NDR) effect. The output current presents the decreasing trend before saturation due to the NDR [21]–[23]. As the V_g is constant while V_d sweeps, internal voltage (V_{int}) of the MD-NCFET shows different characteristics from the traditional MOSFET due to the voltage amplification of ferroelectric material. As the V_d increases from 0, NC region is caused due to the ferroelectric layer, leading to the phenomenon that gate charge decreases while V_{FE} increases. Consequently, V_{int} reduces and the carriers near the channel decreases, causing the decrease of I_d. Fig. 5(c) depicts *SS*-V_g plot with different T_{FE}. It can be found that the *SS* exhibits smaller value with thicker T_{FE} at any certain V_g, indicating that the increase of T_{FE} can enhance the NC effect. Besides, the improved *SS* can also be explained by the profile of the conduction band energy along the channel. Fig. 5(d) shows the distribution of conduction band energy (E_c) along the channel in the MD-NCFET in comparison with that of the baseline non-FeFET device, which explains the mechanism of the *SS* improvement. With increasing V_g, the reduction of the conduction band barrier in MD-NCFET is more significant than that of the baseline non-FeFET device, which can be attributed to the voltage amplification of ferroelectric layer. Therefore, higher current is obtained for the MD-NCFET, resulting in the decrease of *SS*. In addition, due to the existence of NC effect, the halo-like bulges appear at the edges of the source and drain in the conduction band energy distribution when V_g becomes larger [24], as shown in Fig. 5(d).

The *SS* and hysteresis effect caused by different T_{FE} mentioned above can be explained by capacitance matching theory [8]–[10]. From Fig. 4(b), the voltage amplification (A_{FE}) can be obtained as:

$$A_{FE} = \frac{V_{int}}{V_g} = \frac{C_{FE}}{C_{MOS} + C_{FE}} = \frac{|C_{FE}|}{|C_{FE}| - C_{MOS}} \tag{8}$$

The NCFET with the NC effect ($C_{FE} < 0$) can produce larger internal voltage without large input gate voltage and achieve lower *SS* than the traditional MOSFET. To obtain A_{FE} larger than 1, the C_{FE} should be satisfied as:

$$|C_{FE}| > C_{MOS} \tag{9}$$

With properly tuning the T_{FE}, C_{FE} can be made to match C_{MOS} closely, resulting in the hysteresis-free operation with sub-60 mV/dec *SS*. However, if $|C_{FE}|$ is lower than C_{MOS}, the hysteresis occurs. It indicates the better the capacitance matching between $|C_{FE}|$ and C_{MOS} is achieved, the lower the *SS* is. Fig. 6(a) shows the *SS* and hysteresis as a function of T_{FE}. With the increase of the T_{FE}, the *SS* decreases before T_{FE} goes beyond 29 nm and no hysteresis is found. With the T_{FE} further increasing from 29 nm, the *SS* continues to decrease while the hysteresis occurs. To make the explanation of it, the charge as a function of capacitance at various T_{FE} is evaluated as shown in Fig. 6(b). It can be found that (9) is satisfied before T_{FE} goes beyond 29 nm. The $|C_{FE}|$ at $T_{FE} = 29$ nm is matched much closely to the C_{MOS}, resulting in the lowest *SS* with no hysteresis. When T_{FE} is larger than 29 nm, the C_{MOS} exceeds the $|C_{FE}|$ between two *Q* points, as shown in Fig. 6(b).

The effect of T_{OX} on the performance of the MD-NCFET is also investigated based on NC theory. Fig. 7(a) shows the

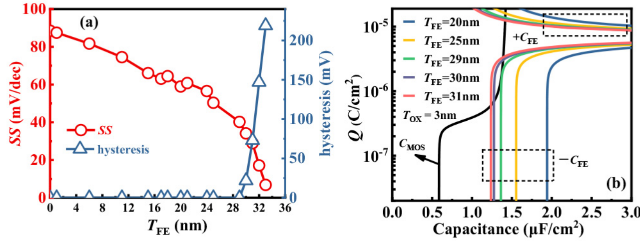

FIGURE 6. **(a)** ***SS*** **and hysteresis as a function of** T_{FE} **and (b) Charge as a function of** C_{FE} **and** C_{MOS} **at various** T_{FE} **with** $T_{OX} = 3$ **nm for MD-NCFETs.**

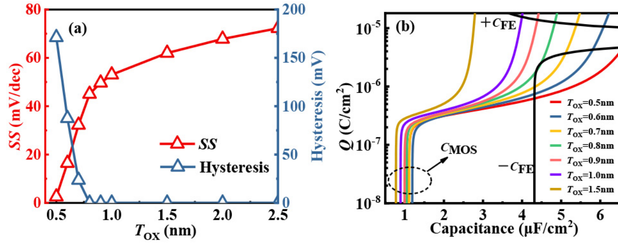

FIGURE 7. **(a)** ***SS*** **and hysteresis as a function of** T_{OX} **and (b) Charge as a function of** C_{FE} **and** C_{MOS} **at various** T_{OX} **with** $T_{FE} = 10$ **nm for MD-NCFETs.**

SS and hysteresis as a function of T_{OX} at the fixed T_{FE} of 10 nm. To achieve the capacitance match, T_{OX} should be tuned to satisfy (9). Fig. 7(b) depicts the charge as a function of C_{FE} and C_{MOS} at various T_{OX}. With T_{OX} decreasing to 0.8 nm, *SS* decreases with no hysteresis. However, with T_{OX} continues to decrease below 0.8 nm, the hysteresis occurs. It can be clearly seen that the C_{MOS} is matched much closely to the $|C_{FE}|$ when $T_{OX} = 0.8$ nm. Therefore, by appropriately selecting T_{OX} with fixed T_{FE}, the performance of the MD-NCFET will be optimized.

With the device size being scaled down, the L_g effect on the device performance of the MD-NCFET is also of great importance. Based on the optimal T_{FE}, T_{OX} obtained by the capacitance matching theory mentioned above, the L_g effect is further investigated for *SS* improvement. Fig. 8(a) shows the *SS* versus L_g for traditional MOSFET and MD-NCFET with the $T_{FE} = 29$ nm and $T_{OX} = 3$ nm by capacitance matching. The *SS* remains almost stable in long channel but exhibits a slight drop as the L_g becomes shorter to nearly hundreds nanometers. However, when L_g is even shorter, the *SS* presents the dramatical increase. To explain this phenomen, the factors of the *SS* should be considered. For the *SS*, it can be expressed as [24]:

$$SS = \frac{\partial V_g}{\partial log_{10} I_d} = \frac{\partial \psi_c}{\partial log_{10} I_d} \frac{m}{A_{FE}} \tag{10}$$

where ψ_c is the minimum potential along the channel center, and $m = \partial V_{int}/\partial \psi_c$ is the body factor. The A_{FE} represents the amplification ability of the ferroelectric layer to the input gate voltage. From (10), the first term remains constant (~60 mV/dec) due to the Boltzmann limit. Therefore, the second term m/A_{FE} plays an important role in *SS*.

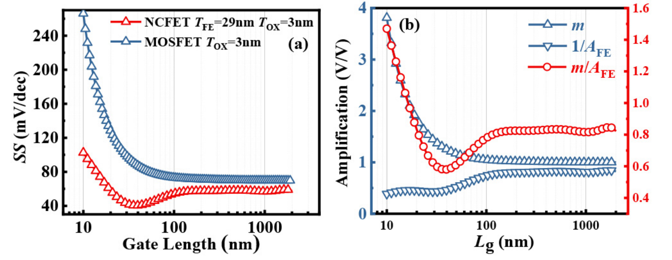

FIGURE 8. **(a)** ***SS*** **versus** L_g **for traditional MOSFET and MD-NCFET with the** $T_{FE} = 29$ **nm and** $T_{OX} = 3$ **nm by capacitance matching and (b) impact factors including** m**,** A_{FE} **and** m/A_{FE} **as a function of** L_g**.**

Fig. 8(b) illustrates the impact factors including m, A_{FE} and m/A_{FE} as a function of L_g, demonstrating the trend of the *SS* with the L_g variation. With the L_g decreasing, the ferroelectric polarization is strengthened due to the enhancement of the fringing field coupling [25]. Equivalently, it induces the accumulation of negative charge in the interface of gate terminal with the L_g scaling, causing that the C_{MOS} increases but the C_{FE} remains almost constant [26]. Therefore, A_{FE} increases with the L_g scaling according to (8), generating the decrease of the *SS*. However, due to the existence of short channel effect [24], the reduction of the *SS* experiences a limitation when the L_g further decreases. As the L_g becomes shorter, the short channel effect becomes an increasingly indispensable factor, resulting that the factor m related to the short channel effect will increase rapidly and dominate over $1/A_{FE}$. With the increase of the m/A_{FE}, the *SS* accordingly increases. In addition, similar phenomon can be found in the MD-MFIS-NCFETs with other optimal T_{FE} and T_{OX} by capacitance matching (not shown here).

It is worth mentioning that there exists a trade-off between the *SS* and L_g in the NCFET design. The discussion mentioned above only concentrates on the effect of single-variable (T_{FE}, T_{OX} or L_g) on the *SS* and hysteresis properties of MD-NCFET. On this basis, more correlation studies are performed. In order to find further optimization solution for NCFET design, the simultaneous analysis of multi-variables (T_{FE}, T_{OX} and L_g) effect on the performance of MD-NCFET is presented. Fig. 9 shows the effect of the T_{FE} and T_{OX} on the *SS* and hysteresis properties with different L_g. It can be seen the white area is the hysteresis area while the colored area is the hysteresis-free area with the *SS* distribution at different T_{FE}, T_{OX}. For short L_g (20 or 40nm), *SS* values exhibits obvious change, while for long L_g (60, 100 nm or more), *SS* values remain relatively stable in the hysetersis-free region. Moreover, it is worth noting that in the hysteresis-free region with the fixed T_{OX}, the phenomenon that the *SS* decreases as the T_{FE} increases can also be found. At the same time, with the same T_{FE}, the effect of increasing T_{OX} gives a rise in the *SS*. Besides, the more severe *SS* degradation with wider distribution due to the short channel effect can be observed in the MD-NCFET with shorter L_g, which is in good agreement with the L_g effect mentioned above. In addition, in the

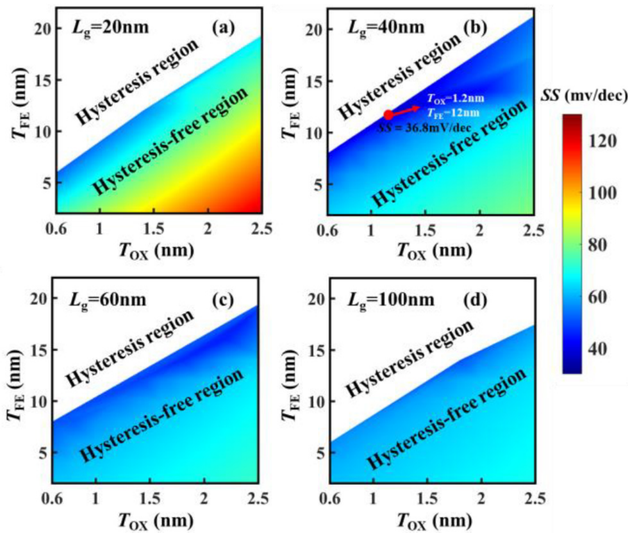

FIGURE 9. Hysteresis and hysteresis-free region with the *SS* distribution at different T_{FE}, T_{OX} with the L_g of (a) 20 nm, (b) 40 nm, (c) 60 nm and (d) 100 nm.

process of continuously shrinking the L_g, it is challenging to avoid the degraded *SS* caused by short channel effect. Through the observation, the lowest *SS* of 36.8 mV/dec with hysetersis-free property is found in the MD-NCFET with $L_g = 40$ nm, $T_{OX} = 1.2$ nm and $T_{FE} = 12$ nm, which can be found in the red dot in Fig. 9(b). The optimization strategy of the simultaneous multi-variables analysis here obtains lower *SS* than that of single-variable analysis discussed above (*SS* = 40.6 mV/dec in Fig. 5(a) when $L_g = 40$ nm, $T_{OX} = 3$ nm and $T_{FE} = 29$ nm), indicating that simultaneous analysis of multi-variables enables to search optimal MD-NCFET structural parameters when designing high-performance NCFET.

IV. VALIDATION

The TCAD model used in this work has been validated for the reported experimental NCFET on fully depleted silicon-on-insulator (FDSOI) with $T_{OX} = 3$ nm, $T_{FE} = 5$ nm and $L_g = 90$ nm [27]. Fig. 10 shows the experimental and simulated transfer I_d-V_g curves at $V_d = 0.05$ V. Obviously, the simulation result is in good agreement with the experimental data. Based on this calibration, the optimized simulation results were obtained from the optimization with single-variable and multi-variable analysis based on MD-NC model, respectively. The experimental *SS* was 69.7 mV/dec. Considering the optimization by changing single variable (L_g, T_{FE} or T_{OX}) with unchanged other variables, the optimized hysteresis-free *SS* was 64.7, 64.6 and 63.9 mV/dec for L_g, T_{FE} or T_{OX} at 150, 17 and 0.4 nm, respectively, indicating that the optimization results were not satisfied enough. When using the optimization by simultaneous multi-variables analysis discussed above, the hysteresis-free *SS* was 48.4 mV/dec, and the device structural parameters were determined as $T_{OX} = 3$ nm, $T_{FE} = 34$ nm, and $L_g = 45$ nm. According to the optimization results, the hysteresis-free *SS*

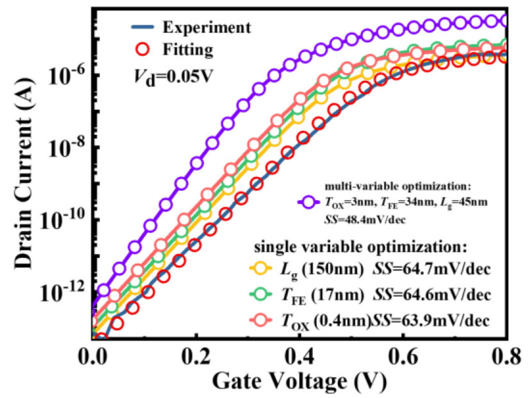

FIGURE 10. Experimental and simulated transfer I_d-V_g curves at $V_d = 0.05$ V.

obtained by simultaneous multi-variable analysis is much smaller than that obtained by single-variable analysis and 30.6% smaller than the experimental *SS*.

V. CONCLUSION

In this paper, with the simulated calibration for the MD-NCCAP, the MD-MFIS-NCFET is established based on the ferroelectric parameters extracted from the experimental results and the verified baseline non-FeFET model. Electrical characteristics of the MD-NCFETs are illustrated to investigate the *SS* properties and capacitance matching mechanism. Further study concentrates on demonstrating the variation of the *SS* or hysteresis influenced by the structural multi-variables including T_{FE}, T_{OX} and L_g. By simultaneously selecting the appropriate T_{FE}, T_{OX} and L_g, the optimal *SS* with no hysteresis can be obtained. The final TCAD verification and optimization for the reported experimental data demonstrates that the proposed optimization by considering the multi-variable effect is feasible, which could provide a solution for practical high-performance NCFET design.

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