

Received 12 March 2021; revised 13 May 2021; accepted 24 July 2021. Date of publication 28 July 2021; date of current version 12 August 2021.
The review of this article was arranged by Editor S. Chakrabarti.

Digital Object Identifier 10.1109/JEDS.2021.3100760

Effect of *In-Situ* Silicon Carbon Nitride (SiCN) Cap Layer on Performances of AlGa_N/Ga_N MISHFETs

JAE-HOON LEE¹ (Senior Member, IEEE), KI-SIK IM² (Member, IEEE),
AND JUNG-HEE LEE³ (Senior Member, IEEE)

¹ Yield Enhancement Team, Foundry, Samsung Electronics Company Ltd., Pyeongtack 177786, South Korea

² Advanced Material Research Center, Kumoh National Institute of Technology, Gumi 39177, South Korea

³ School of Electronics Engineering, Kyungpook National University, Daegu 41566, South Korea

CORRESPONDING AUTHOR: J.-H. LEE (e-mail: jaehoon03.lee@samsung.com)

This work was supported by Civil-Military Technology Cooperation Program under Grant 19-CM-BD-05.

ABSTRACT AlGa_N/Ga_N metal insulator semiconductor heterostructure field effect transistors (MISHFETs) with different thickness of *in-situ* silicon carbon nitride (SiCN) cap layer were investigated. It was found that *in-situ* SiCN layer not only increases the two dimensional electron gas (2DEG) density, but also effectively passivates the surface of the AlGa_N/Ga_N MISHFET. The fabricated device with 2 nm-thick SiCN cap layer exhibits superior device performances, such as larger maximum transconductance (g_m) and higher on/off drain-current ratio (I_{ON}/I_{OFF}) compared to those of the device without SiCN cap layer.

INDEX TERMS AlGa_N/Ga_N, metal insulator semiconductor heterostructure field effect transistors (MISHFETs), *in-situ* silicon carbon nitride (SiCN), cap layer, 2DEG density, surface leakage current.

I. INTRODUCTION

AlGa_N/Ga_N-based heterostructure field effect transistors (HFETs) are very promising power electronic and high frequency device applications [1], [2]. Even though the epitaxial growth and device fabrication of AlGa_N/Ga_N HFETs have been matured, it is still necessary to reduce the surface traps, which leads to degrade the device performances and deteriorate the device reliability. The origin of the surface traps in AlGa_N/Ga_N heterostructures is believed to be mainly due to the formation of unstable native GaO_x on the surface of AlGa_N barrier [3]. It leads to large leakage current and occasionally severe current collapse when the HFET operates under high power and high frequency conditions. The epitaxial Ga_N cap layer was usually grown on AlGa_N layer to protect the AlGa_N surface, but the removal of GaO_x has been turned out to be difficult [4]. The *ex-situ* deposition of dielectrics like SiN_x, SiO₂, and Al₂O₃ has been applied to passivate the surface [5]–[7], but the results are not satisfactory to completely eliminate the formation of the GaO_x

at the AlGa_N surface due to the finite surface exposure to ambience or undesirable chemical reaction at the surface.

The *in-situ* growth of SiN_x layer has been investigated not only to prevent the AlGa_N surface from being exposed to air ambient, but also to provide an effective surface passivation for the AlGa_N/Ga_N HFETs [8]–[11]. Recently, we also proposed a similar method for passivating the surface of an AlGa_N/Ga_N Schottky barrier diode (SBD), which utilizes very thin *in-situ* silicon carbon nitride (SiCN) cap layer with thickness of a few nm [12]. The thickness of the SiCN cap layer is comparable to the thickness of the Ga_N cap layer. Therefore, the thin *in-situ* SiCN cap layer on the AlGa_N layer would replace the Ga_N cap layer, without significantly changing the threshold voltage of the device, because it is not necessary to be etched away for the fabrication of the AlGa_N/Ga_N HFET. Instead, the existence of the thin *in-situ* SiCN cap layer effectively passivates the AlGa_N surface to reduce the leakage current of the device even without depositing an additional thicker surface passivation layer.

Furthermore, the thin *in-situ* SiCN cap layer would increase the 2DEG sheet carrier concentration and electron mobility to improve the on-current of the device.

In this work, the AlGaIn/GaN metal-insulator-semiconductor heterostructure field effect transistors (MISHFETs) with the different *in-situ* SiCN thickness were fabricated and the thickness of the *in-situ* SiCN cap layer was optimized with analyzing the device performances along with Hall effect and atomic force microscopy (AFM) measurement.

II. EXPERIMENTS

AlGaIn/GaN heterostructure deposited the *in-situ* SiCN cap layer was grown on 4-inch (0001) c-plane sapphire substrates utilizing metal-organic chemical vapor deposition (MOCVD) [10], [13]. Trimethylgallium (TMGa), trimethylaluminum (TMAI), carbontetrabromide (CBr₄), ditertiarybutylsilane (DTBSi), and ammonia (NH₃) were used for the precursors for Ga, Al, C, Si, and N, respectively. The detailed layer structure proposed in this work consists of 30 nm-thick GaN initial nucleation layer grown at low temperature, 3 μm-thick highly-resistive GaN buffer layer, and 25 nm-thick AlGaIn barrier layer. Finally, the SiCN cap layer was grown at 1100 °C with varying its thickness from 2 to 10 nm. The AlGaIn/GaN heterostructure without the SiCN cap layer was also grown as a reference sample. The Al content in the AlGaIn barrier is 27%, which is determined by high-resolution X-ray diffraction (XRD).

For the device fabrication, the active region of the device was defined by inductively coupled plasma reactive ion etching (ICP-RIE) using a BCl₃/Cl₂ gas mixture. The SiCN cap layer in source and drain region was removed using same ICP-RIE machine. Ohmic metal layer with Ti/Al/Ni/Au was then deposited and followed by rapid thermal annealing at 850 °C for 30 sec in N₂ ambient. Finally, Ni/Au gate metal was deposited on the SiCN cap layer. The gate length, the gate width, and the gate-to-drain distance of devices were 3, 50, and 10 μm, respectively. A schematic cross-sectional view of the fabricated MISHFETs is shown in Fig. 1. The SiCN cap layer with thickness of 2 nm is shown from the transmission electron microscope (TEM) image in the inset of the figure.

III. RESULTS AND DISCUSSION

Fig. 2 shows the Hall measurement of samples with different SiCN cap-layer thickness from 0 to 10 nm according to growth time. The sample grown without SiCN cap layer exhibited sheet resistance (R_{sh}) of 488 Ω/□, 2DEG sheet carrier density of $7.5 \times 10^{12} \text{ cm}^{-2}$, and mobility of 1650 cm²/V.s. All samples with SiCN cap layers exhibited decreased R_{sh} from 420 to 384 Ω/□, increased sheet carrier density from 8.4 to $10.4 \times 10^{12} \text{ cm}^{-2}$, and decreased mobility from 1530 to 1250 cm²/V.s compared to that of sample without SiCN cap layer. Especially, the product of (mobility) × (sheet carrier density) is highest when thickness of SiCN is 2 nm. The values of the sheet carrier density for

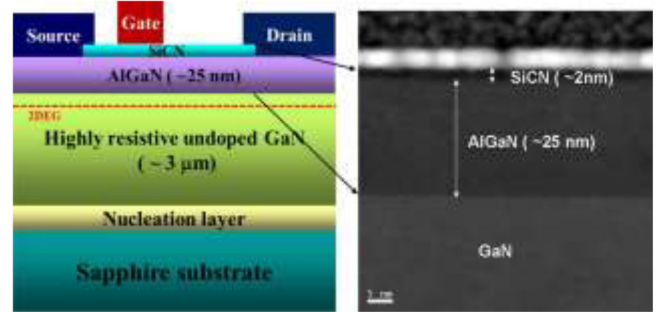


FIGURE 1. Schematic cross-sectional view of the fabricated MISHFETs. Inset shows the TEM image for the AlGaIn/GaN heterostructure with 2 nm-thick SiCN-cap layer.

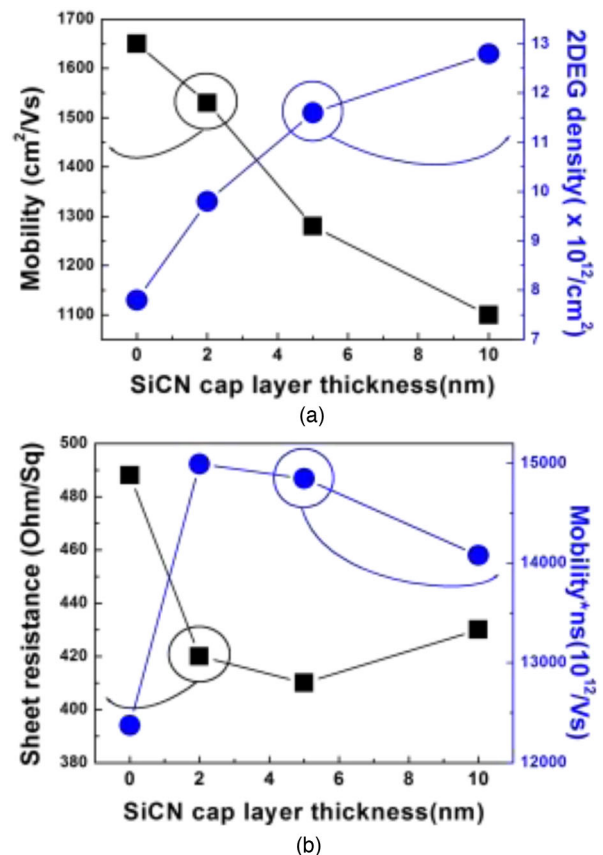


FIGURE 2. Hall measurement data for samples with different SiCN-cap layer thickness: (a) mobility and concentration, (b) sheet resistance and the product of mobility × sheet carrier density (n_s).

the samples with SiCN cap layer were higher than that of the reference sample without cap layer, which can be expected because the existence of Si⁺ ions in the *in-situ* SiCN film induces more electrons in the 2DEG channel. Onojima *et al.* [14] reported that the Si atoms located at the SiN/AlGaIn interface act as positively ionized donor, which can partially neutralize the negative polarization charge of the AlGaIn surface and hence increase the 2DEG density. The degradation in mobility for the samples with cap layer

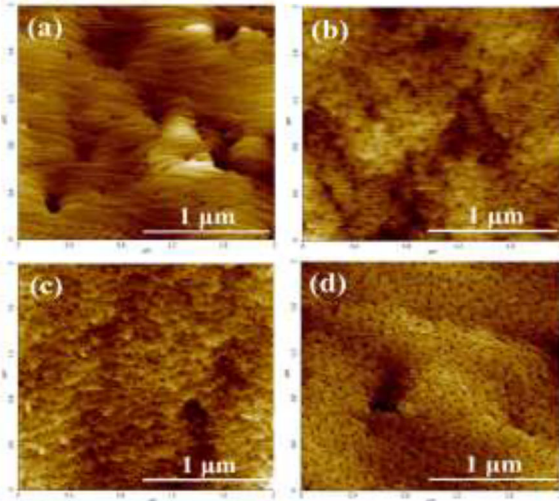


FIGURE 3. AFM images (2 μm × 2 μm) of surface morphology according to the SiCN cap-layer thickness with (a) 0 nm, (b) 2 nm, (c) 5 nm, and (d) 10 nm.

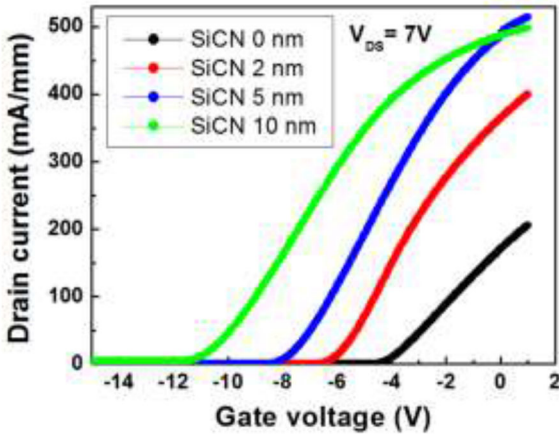


FIGURE 4. I-V characteristics of the AlGaIn/GaN MISHFETs according to the SiCN cap layer thickness.

is probably due to the increased strain-induced interface roughness scattering at the AlGaIn/GaN interface [15]–[17].

Fig. 3 shows atomic force microscopy (AFM) surface images for the as-grown AlGaIn/GaN heterostructures with and without SiCN cap layer. The root-mean-square (rms) roughness of the structure without SiCN cap-layer is 0.8 nm. The surface morphology of the structure with 2 and 5 nm-thick SiCN cap layer becomes improved with corresponding rms roughness of 0.3 and 0.5 nm, respectively. This is because the rough AlGaIn surface becomes smooth during the slow growth of the SiCN cap layer with growth rate (5 nm/hour). However, the surface morphology of the structure with 10 nm-thick SiCN cap layer becomes poor with rms roughness of 1.0 nm, which is believed to be due to the etching process of the AlGaIn surface under DTBSi/NH₃/CBR₄ gas conditions for longer growth time at high temperatures of 1100 °C [18]–[23]. The etching of the AlGaIn surface

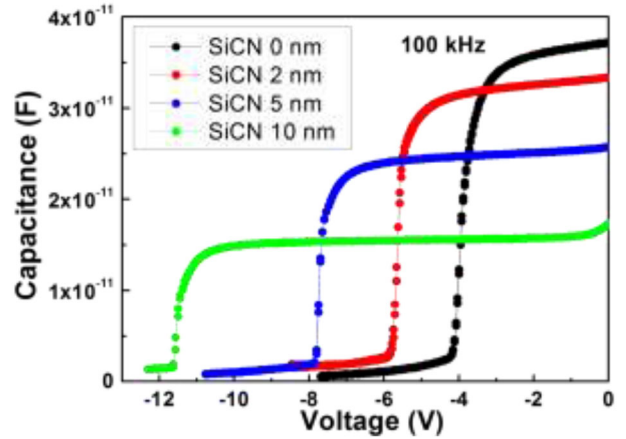


FIGURE 5. C-V characteristics of the SiCN/AlGaIn MIS capacitors measured at 100 kHz according to SiCN thickness.

and its effect on the device performance will be further discussed later.

Fig. 4 shows the static current-voltage (I-V) characteristics of the AlGaIn/GaN MISHFETs with different SiCN cap-layer thickness of 0 to 10 nm. The threshold voltages of the devices were shifted from −4.5 to −12 V as the thickness of the SiCN cap layer increased. The threshold voltage shift of the MISHFET, as compared to the control HFET, is given as [24]

$$V_{TH}^{MIS} - V_{TH}^{HFET} = \phi_b^{MIS} - \phi_b^{HFET} - \frac{1}{e} \Delta E_{C_SiCN/AlGaIn} - V_{SiCN} \quad (1)$$

where ϕ_b^{MIS} and ϕ_b^{HFET} represent the Schottky potential barrier of Ni/SiCN/AlGaIn and Ni/AlGaIn, respectively [10]. $\Delta E_{C_SiCN/AlGaIn}$ is the SiCN/AlGaIn conduction band offset. V_{SiCN} is the electric potential drops in the SiCN layer. By solving Gauss formula at each interface, the expression of V_{SiCN} can be derived [25]

$$V_{SiCN} = \frac{e(\sigma_{if} - \sigma_D - \sigma_{AlGaIn})}{C_{SiCN}} \quad (2)$$

where σ_{if} is the effective fixed charge density at SiCN/AlGaIn interface, σ_D is background electron concentration in GaN buffer, σ_{AlGaIn} is polarization charges of AlGaIn. Note that the capacitance of the SiCN dielectric (C_{SiCN}) is determined through capacitance-voltage (C-V) characterization of the Ni/SiCN/AlGaIn/GaN MIS diodes as shown in Fig. 5. The capacitance at accumulation, measured at 100 kHz, was 4.73×10^{-7} , 3.27×10^{-7} , 2.57×10^{-7} , and 2.20×10^{-7} F/cm² for the sample with SiCN cap layer thickness of 0, 2, 5, and 10 nm, respectively. When assuming SiCN/AlGaIn conduction band offset is ~2.29 eV [26]–[28] from the Equations (1) and (2), the effective fixed charge density at SiCN/AlGaIn interface is roughly determined to be 1.7×10^{13} , 1.9×10^{13} , and 2.3×10^{13} /cm² for SiCN cap-layer thickness of 2, 5, and 10 nm, respectively.

It is noticed from Fig. 6(a) that the MISHFET with 2 nm-thick SiCN cap layer exhibits the highest maximum

transconductance (g_m), almost two times higher than that of the HFET without SiCN cap layer. The reason for the g_m enhancement of the MISHFET with 2 nm-thick SiCN cap layer is due to the decrease in series resistance caused by higher 2DEG density, as shown in Fig. 2(b) [29], [30]. As the thickness of the SiCN cap layer increases, however, the g_m for the MISHFET gradually decreases due to the increased gate leakage current as shown in Fig. 6(c), which will be discussed below.

Fig. 6(b) and 6(c) show the logarithmic $I_D - V_G$ curves and the gate leakage currents, respectively. The MISHFET with 2 nm-thick SiCN cap layer exhibits better subthreshold characteristics with subthreshold swing (SS) of 90 mV/dec, higher on/off drain-current ratio (I_{ON}/I_{OFF}), and much lower gate leakage current compared to the MISHFET without SiCN cap layer. This indicates that 2 nm-thick SiCN cap layer gate leakage current compared to the MISHFET without SiCN cap layer. This indicates that 2 nm-thick SiCN cap layer effectively passivates the AlGaIn surface. However, the MISHFET with 5 nm-thick SiCN cap layer shows slightly degraded SS and increased gate leakage current. However, the performances of the MISHFET with 10 nm-thick SiCN layer become severely degraded. This unexpected result can be explained by considering the AFM images in Fig. 3. Prior to the SiCN growth, many V-shaped pits were evolved on the AlGaIn surface as shown in Fig. 3 (a), which is believed to be due to the threading dislocation [31]. After the growth of the SiCN layer with thickness up to 5 nm, the surface becomes smooth and most V-shaped pits were covered with deposition of the SiCN layer. Conversely, few V-shaped pits becomes enlarged and deeper as shown in Fig. 3(d), after growing 10 nm-thick SiCN layer. This is because the etching process of the AlGaIn layer near relatively large-sized V-shaped pits can be favorable than the growth of SiCN layer under the growth ambient (DTBSi/NH₃/CB₄) at high temperature (1100 °C) for long time. The schematic etching process is illustrated in Fig. 7. The measured depth of the pit was increased to from 3.98 nm for the sample without cap layer to 6.18 nm after growing 10 nm-thick SiCN layer.

The V-shaped pits on the AlGaIn surface severely increase the trap-assisted tunneling leakage current through the Schottky contact. However, the leakage current can be effectively reduced with growing a 2 nm-thick SiCN cap layer on the AlGaIn layer. This thin SiCN cap layer not only passivates the AlGaIn surface, but also covers the V-shaped pits to block the leakage path (Fig. 7 (b)), which greatly reduces the gate leakage current as shown in Fig. 6 (c). As the thickness increases to 5 nm, however, the leakage current slightly increases. This is because the size of the V-shaped pits becomes large due to the incidental etching process described above [18]–[23], even though the evidence is not shown in AFM image in Fig. 3. When the growth time is very long, the etching of AlGaIn layer is rather favorable than the growth of the SiCN layer to make the V-shaped pits deeper and would expose the AlGaIn layer to ambient. Therefore, in the case of the device with 10 nm-thick SiCN cap layer

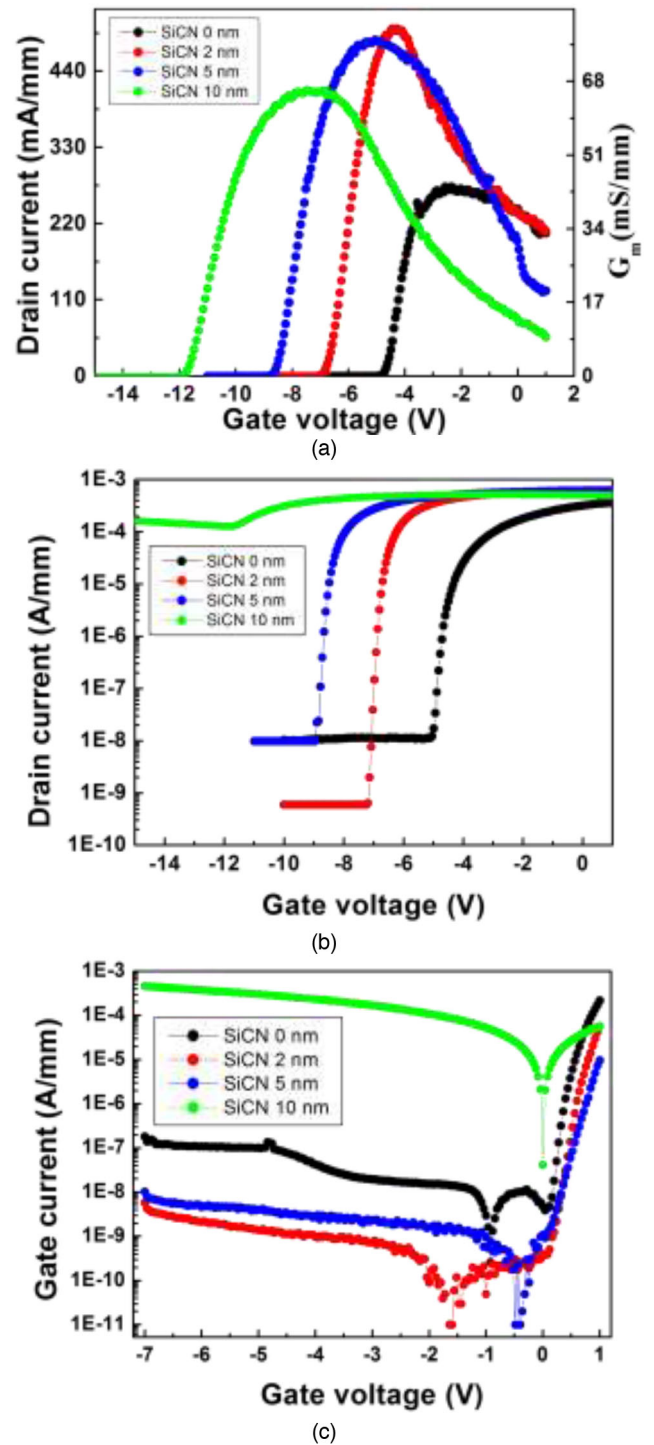


FIGURE 6. I-V characteristics of the AlGaIn/GaN MISHFETs according to the SiCN cap layer thickness; (a) G_m characteristics, (b) log-scale drain currents and (c) gate leakage current.

(Fig. 7 (c)), the gate metal deposits not only on the SiCN cap layer, but also directly on the exposed AlGaIn layer near V-shaped pits, which results in huge gate leakage current due to tunneling process through the thinned AlGaIn barrier to the GaN channel layer [32]. In addition, the a surface etching process is also likely to introduce large amount of the

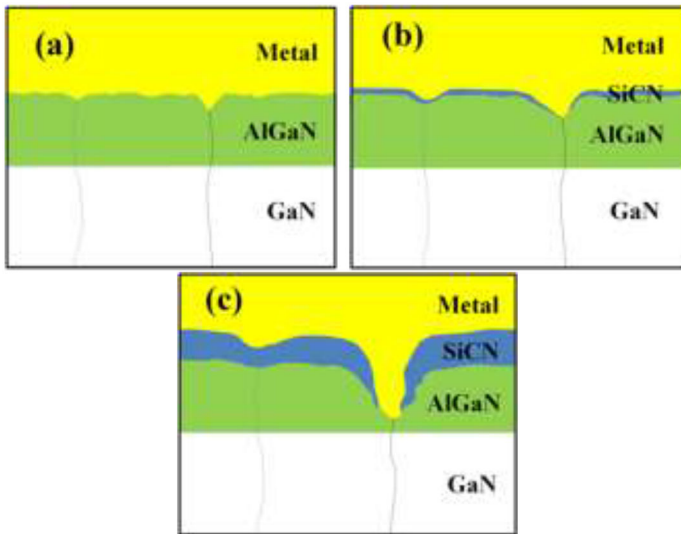


FIGURE 7. Schematic views of V-shaped pits enlarged by DTBSi/NH₃/CBr₄ etching effect at high temperature during the long growth time with (a) no SiCN layer, (b) 2 nm-SiCN layer, and (c) 10 nm-SiCN layer.

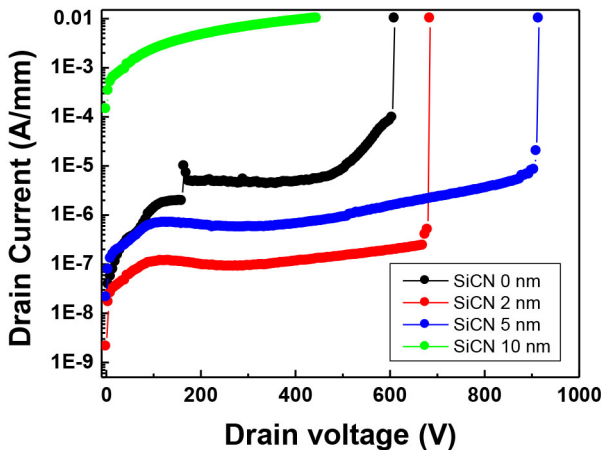
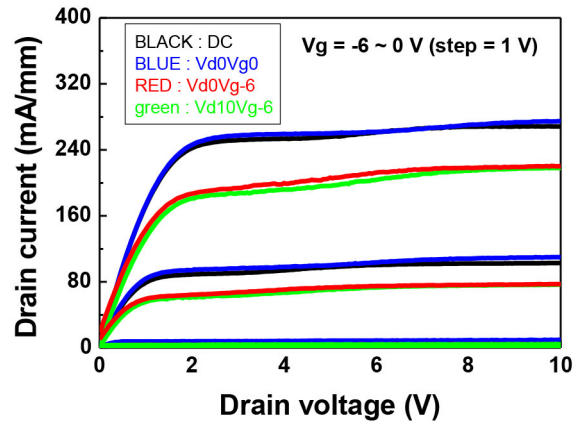


FIGURE 8. Off-state breakdown characteristics of the AlGaN/GaN MISHFETs according to the SiCN cap layer thickness ($L_{GD} = 10 \mu\text{m}$).

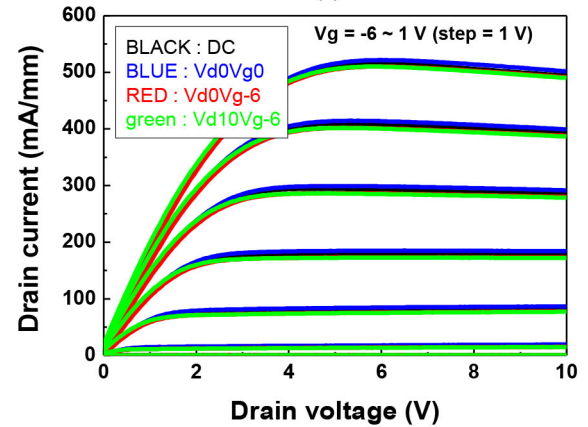
nitrogen vacancies on the exposed surface of AlGaN layer to further increase the tunneling leakage current [33]. Further investigation is still required to more clearly understand the etching effect in *in-situ* growth of the SiCN layer.

Fig. 8 shows the off-state breakdown characteristics of the AlGaN/GaN MISHFETs with different SiCN layer thickness. Due to effective surface passivation of SiCN cap layer, the breakdown voltage of the MISHFET with 2 and 5 nm-thick SiCN cap layer were increased to 686 and 915 V, respectively, compared to the value of ~ 590 V for the MISHFET without SiCN cap layer. However, the device with 10 nm-thick SiCN cap layer, the breakdown voltage was extremely low due to large leakage current caused by issues described above.

Fig. 9 shows the pulsed I-V characteristics of AlGaN/GaN MISHFETs with and without 2 nm-thick SiCN cap layer to



(a)



(b)

FIGURE 9. Pulsed I-V characteristics of MISHFETs without (a) and with (b) 2nm-thick SiCN cap layer.

evaluate the current dispersion related to the trapping effects. The bias voltages for measuring the gate- and the drain-lag were set at $V_{DS} = 0$ V, $V_{GS} = -6$ V and $V_{DS} = 10$ V, $V_{GS} = -6$ V, respectively [34]. The pulse width of 0.5 ms and the pulse period of 0.5 ms were set. The device with SiCN cap layer exhibited almost negligible current dispersion, while the device without SiCN cap layer poor current dispersion with increased on-resistance and large current collapse. This result suggests that the thin SiCN cap layer effectively passivates the surface of the device and suppresses the current dispersion in AlGaN/GaN HFETs [35].

IV. CONCLUSION

Improved electrical characteristics of the AlGaN/GaN MISHFET with the *in-situ* SiCN cap-layer grown at high temperature have been demonstrated. The fabricated device with 2 nm-thick SiCN cap layer exhibits maximum transconductance of almost two times higher and on/off drain-current ratio of two orders higher than those of the device without SiCN cap layer. The enhanced device performances for the device with 2 nm-thick SiCN cap layer are because the *in-situ* SiCN cap layer not only increases the 2DEG density, but also effectively passivates the surface of the device.

REFERENCES

- [1] Y.-F. Wu, D. Kapolnek, J. P. Ibbetson, P. Parikh, B. P. Keller, and U. K. Mishra, "Very-high power density AlGaIn/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 586–590, Mar. 2001, doi: [10.1109/16.906455](https://doi.org/10.1109/16.906455).
- [2] Y. Uemoto *et al.*, "Gate injection transistor (GIT)—A normally-off AlGaIn/GaN power transistor using conductivity modulation," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3393–3399, Dec. 2007, doi: [10.1109/LED.2007.908601](https://doi.org/10.1109/LED.2007.908601).
- [3] S. Yang *et al.*, "High-quality interface in Al₂O₃/GaN/AlGaIn/GaN MIS structures with in situ pre-gate plasma nitridation," *IEEE Electron Device Lett.*, vol. 34, no. 12, pp. 1497–1499, Dec. 2013, doi: [10.1109/LED.2013.2286090](https://doi.org/10.1109/LED.2013.2286090).
- [4] S. Arulkumaran, T. Egawa, and H. Ishikawa, "Studies on the influences of *i*-GaN, *n*-GaN, *p*-GaN and InGaN cap layers in AlGaIn/GaN high-electron-mobility transistors," *Jpn. J. Appl. Phys.*, vol. 44, no. 5R, pp. 2953–2960, May 2005, doi: [10.1143/JJAP.44.2953](https://doi.org/10.1143/JJAP.44.2953).
- [5] N. Onojima, M. Higashiwaki, J. Suda, T. Kimoto, T. Mimura, and T. Matsui, "Reduction in potential barrier height of AlGaIn/GaN heterostructures by SiN passivation," *J. Appl. Phys.*, vol. 101, no. 4, pp. 1–6, Feb. 2007, doi: [10.1063/1.2472255](https://doi.org/10.1063/1.2472255).
- [6] C. Wang *et al.*, "Mechanism of superior suppression effect on gate current leakage in ultrathin Al₂O₃/Si₃N₄ bilayer-based AlGaIn/GaN insulated gate heterostructure field-effect transistors," *Jpn. J. Appl. Phys.*, vol. 45, no. 1R, pp. 40–42, Jan. 2006, doi: [10.1143/JJAP.45.40](https://doi.org/10.1143/JJAP.45.40).
- [7] S. Arulkumaran, T. Egawa, and H. Ishikawa, "Studies on the influences of *i*-GaN, *n*-GaN, *p*-GaN and InGaN cap layers in AlGaIn/GaN high-electron-mobility transistors," *Jpn. J. Appl. Phys.*, vol. 44, no. 5R, pp. 2953–2960, May 2005, doi: [10.1143/JJAP.44.2953](https://doi.org/10.1143/JJAP.44.2953).
- [8] J. Derluyn *et al.*, "Improvement of AlGaIn/GaN high electron mobility transistor structures by in situ deposition of a Si₃N₄ surface layer," *J. Appl. Phys.*, vol. 98, no. 5, pp. 1–5, Sep. 2005, doi: [10.1063/1.2008388](https://doi.org/10.1063/1.2008388).
- [9] H. Jiang, C. Liu, Y. Chen, X. Lu, C. W. Tang, and K. M. Lau, "Investigation of in situ SiN as gate dielectric and surface passivation for GaN MISHEMTs," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 832–839, Mar. 2017, doi: [10.1109/LED.2016.2638855](https://doi.org/10.1109/LED.2016.2638855).
- [10] L. Cheng *et al.*, "Gate-first process compatible, high-quality in situ SiNx for surface passivation and gate dielectrics in AlGaIn/GaN MISHEMTs," *J. Phys. D, Appl. Phys.*, vol. 52, May 2019, Art. no. 305105, doi: [10.1088/1361-6463/ab1dc3](https://doi.org/10.1088/1361-6463/ab1dc3).
- [11] H. Jiang, C. Liu, Y. Chen, X. Lu, C. W. Tang, and K. M. Lau, "Investigation of in situ SiN as gate dielectric and surface passivation for GaN MISHEMTs," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 832–839, Mar. 2017, doi: [10.1109/LED.2016.2638855](https://doi.org/10.1109/LED.2016.2638855).
- [12] J.-H. Lee, J.-H. Jeong, and J.-H. Lee, "Enhanced electrical characteristics of AlGaIn-based SBD with in situ deposited silicon carbon nitride cap layer," *IEEE Electron Device Lett.*, vol. 33, no. 4, pp. 492–493, Apr. 2012, doi: [10.1109/LED.2012.2182671](https://doi.org/10.1109/LED.2012.2182671).
- [13] J.-H. Lee, J.-H. Jeong, and J.-H. Lee, "Normally off GaN power MOSFET grown on sapphire substrate with highly resistive undoped buffer layer," *IEEE Electron Device Lett.*, vol. 33, no. 10, pp. 1429–1431, Oct. 2012, doi: [10.1109/LED.2012.2207366](https://doi.org/10.1109/LED.2012.2207366).
- [14] N. Onojima, N. Hirose, T. Mimura, and T. Matsui, "Effects of Si deposition on AlGaIn barrier surfaces in GaN heterostructure field-effect transistors," *Appl. Phys. Exp.*, vol. 1, no. 7, pp. 1–3, Jun. 2008, doi: [10.1143/APEX.1.071101](https://doi.org/10.1143/APEX.1.071101).
- [15] F. Sacconi, M. Povolotskiy, and A. D. Carlo, "Strain effects in SiN-passivated GaN-based HEMT devices," *J. Comput. Electron.* vol. 5, pp. 115–118, Jul. 2006, doi: [10.1007/s10825-006-8829-y](https://doi.org/10.1007/s10825-006-8829-y).
- [16] N. Maeda *et al.*, "Systematic study of insulator deposition effect (Si₃N₄, SiO₂, AlN, and Al₂O₃) on electrical properties in AlGaIn/GaN heterostructures," *Jpn. J. Appl. Phys.*, vol. 46, no. 2R, pp. 547–554, Feb. 2007, doi: [10.1143/JJAP.46.547](https://doi.org/10.1143/JJAP.46.547).
- [17] J. R. Shealy, T. R. Prunty, E. M. Chumbes, and B. K. Ridley, "Growth and passivation of AlGaIn/GaN heterostructures," *J. Cryst. Growth*, vol. 250, pp. 7–13, Mar. 2003, doi: [10.1016/S0022-0248\(02\)02187-5](https://doi.org/10.1016/S0022-0248(02)02187-5).
- [18] J. Ma, X. Lu, H. Jiang, C. Liu, and K. M. Lau, "In situ growth of SiNx as gate dielectric and surface passivation for AlN/GaN heterostructures by metalorganic chemical vapor deposition," *Appl. Phys. Exp.*, vol. 7, no. 9, pp. 1–4, Aug. 2014, doi: [10.7567/APEX.7.091002](https://doi.org/10.7567/APEX.7.091002).
- [19] A. Siddique, R. Ahmed, J. Anderson, and E. L. Piner, "Effect of reactant gas stoichiometry of in-situ SiNx passivation on structural properties of MOCVD AlGaIn/GaN HEMTs," *J. Cryst. Growth*, vol. 517, pp. 28–34, Jul. 2019, doi: [10.1016/j.jcrysgro.2019.03.020](https://doi.org/10.1016/j.jcrysgro.2019.03.020).
- [20] K. Pakula, R. Bozek, J. M. Baranowski, J. Jasinski, and Z. Liliental-Weber, "Reduction of dislocation density in heteroepitaxial GaN: Role of SiH₄ treatment," *J. Cryst. Growth*, vol. 267, nos. 1–2, pp. 1–7, Jun. 2004, doi: [10.1016/j.jcrysgro.2004.03.020](https://doi.org/10.1016/j.jcrysgro.2004.03.020).
- [21] R. A. Oliver, M. J. Kappers, J. Sumner, R. Datta, and C. J. Humphreys, "Highlighting threading dislocations in MOVPE-grown GaN using an in situ treatment with SiH₄ and NH₃," *J. Cryst. Growth*, vol. 289, no. 2, pp. 506–514, 2006, doi: [10.1016/j.jcrysgro.2005.12.075](https://doi.org/10.1016/j.jcrysgro.2005.12.075).
- [22] N. Ketteniss, A. Oliver, C. McAleese, M. Kappers, Y. Zhang, and C. Humphreys, "The role of strain in controlling the surface morphology of Al_xGa_{1-x}N following in situ treatment with SiH₄ and NH₃," *Appl. Surface Sci.*, vol. 254, no. 7, pp. 2124–2130, 2008, doi: [10.1016/j.apsusc.2007.08.075](https://doi.org/10.1016/j.apsusc.2007.08.075).
- [23] S. Arakawa, M. Itoh, and A. Kasukawa, "In-Situ etching of semiconductor with CBr₄ in metalorganic chemical vapor deposition (MOCVD) reactor," *Jpn. J. Appl. Phys.*, vol. 41, p. 1076, 2002, doi: [10.1143/JJAP.41.1076](https://doi.org/10.1143/JJAP.41.1076).
- [24] Z. Liu *et al.*, "Investigation of the interface between LPCVD-SiNx gate dielectric and III-nitride for AlGaIn/GaN MIS-HEMTs," *J. Vac. Sci. Technol. B*, vol. 34, no. 4, pp. 1–6, Mar. 2016, doi: [10.1116/1.4944662](https://doi.org/10.1116/1.4944662).
- [25] N. Onojima, M. Higashiwaki, J. Suda, T. Kimoto, T. Mimura, and T. Matsui, "Reduction in potential barrier height of AlGaIn/GaN heterostructures by SiN passivation," *J. Appl. Phys.*, vol. 101, no. 4, pp. 1–6, Feb. 2007, doi: [10.1063/1.2472255](https://doi.org/10.1063/1.2472255).
- [26] M. Kumar, B. Roul, T. N. Bhat, M. K. Rajpalke, A. T. Kalghatgi, and S. B. Krupanidhi, "Valence band offset at GaN/ β -Si₃N₄ and β -Si₃N₄/Si(111) heterojunctions formed by plasma-assisted molecular beam epitaxy," *Thin Solid Films*, vol. 520, no. 15, pp. 4911–4915, May 2012, doi: [10.1016/j.tsf.2011.10.051](https://doi.org/10.1016/j.tsf.2011.10.051).
- [27] J. Robertson and B. Falabretti, "Band offsets of high-*K* gate oxides on III-V semiconductors," *J. Appl. Phys.*, vol. 100, no. 1, pp. 1–8, Jul. 2006, doi: [10.1063/1.2213170](https://doi.org/10.1063/1.2213170).
- [28] T. E. Cook, Jr., C. C. Fulton, W. J. Mccouch, R. F. Davis, G. Lucovsky, and R. J. Nemanich, "Band offset measurements of the Si₃N₄/GaN (0001) interface," *J. Appl. Phys.*, vol. 94, no. 6, pp. 3949–3954, Aug. 2003, doi: [10.1063/1.1601314](https://doi.org/10.1063/1.1601314).
- [29] P. Kordos, D. Gregusova, R. Stoklas, K. Cico, and J. Novak, "Improved transport properties of Al₂O₃/AlGaIn/GaN metal-oxide-semiconductor heterostructure field-effect transistor," *Appl. Phys. Lett.*, vol. 90, no. 12, pp. 1–3, Feb. 2007, doi: [10.1063/1.2716846](https://doi.org/10.1063/1.2716846).
- [30] M. Higashiwaki, T. Matsui, and T. Mimura, "AlGaIn/GaN MIS-HFETs with Γ_T of 163 GHz using cat-CVD SiN gate-insulating and passivation layers," *IEEE Electron Device Lett.*, vol. 27, no. 1, pp. 16–18, Jan. 2006, doi: [10.1109/LED.2005.860884](https://doi.org/10.1109/LED.2005.860884).
- [31] J.-H. Lee, K.-S. Im, J. K. Kim, and J.-H. Lee, "Performance of recessed anode AlGaIn/GaN Schottky barrier diode passivated with high-temperature atomic layer-deposited Al₂O₃ layer," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 324–329, Jan. 2019, doi: [10.1109/LED.2018.2875356](https://doi.org/10.1109/LED.2018.2875356).
- [32] E. Zanoni, M. Meneghini, S. A. Chini, D. Marcon, and G. Meneghesso, "AlGaIn/GaN-based HEMTs failure physics and reliability: Mechanisms affecting gate edge and Schottky junction," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3119–3131, Oct. 2013, doi: [10.1109/LED.2013.2271954](https://doi.org/10.1109/LED.2013.2271954).
- [33] H. Hasegawa, T. Inagaki, S. Ootomo, and T. Hashizume, "Mechanisms of current collapse and gate leakage currents in AlGaIn/GaN heterostructure field effect transistors," *J. Vac. Sci. Technol. B, Microelectron. Nanometer Struct. Process. Meas. Phenom.*, vol. 21, no. 4, pp. 1844–1855, Jul./Aug. 2003, doi: [10.1116/1.1589520](https://doi.org/10.1116/1.1589520).
- [34] S. C. Binari *et al.*, "Trapping effects and microwave power performance in AlGaIn/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 465–471, Mar. 2001, doi: [10.1109/16.906437](https://doi.org/10.1109/16.906437).
- [35] R. Vetry, N. Q. Zhang, S. Keller, and U. K. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaIn/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 560–566, Mar. 2001, doi: [10.1109/16.906451](https://doi.org/10.1109/16.906451).



JAE-HOON LEE (Senior Member, IEEE) received the Ph.D. degree in electronic engineering from Kyungpook National University, Daegu, South Korea, in 2003. He is currently a Principal Engineer with Yield Enhancement Team, Foundry, Samsung Electronics Company, Pyeongtack, South Korea. He has authored or coauthored over 88 articles in peer-reviewed journals, seven book chapters, and holds 48 U.S., 17 foreign, and 52 Korean granted patents in his fields of expertise. His current research interests include GaN-based electron

and optoelectronic devices, IGBT power electronics, and Si CMOS logic devices.



JUNG-HEE LEE (Senior Member, IEEE) received the Ph.D. degree in electrical and computer engineering from North Carolina State University, Raleigh, in 1990. He has been a Professor with the School of Electrical Engineering and Computer Science, Kyungpook National University, Daegu, South Korea, since 1993. He has authored or coauthored over 200 publications on semiconductor materials and devices. His current research interests include the growth of nitride-based materials and the fabrication and characterization of

gallium-nitride-based electronics and optoelectronic devices.



KI-SIK IM (Member, IEEE) received the M.S. and Ph.D. degrees in electronic engineering from Kyungpook National University, Daegu, South Korea, in 2005 and 2012, respectively. He is currently a Research Professor with the Advanced Material Research Center, Kumoh National Institute of Technology, Gumi, South Korea. He has authored or coauthored over 35 articles in peer-reviewed journals. His current research interests include GaN-based electronic nanodevices and physics of III-nitride compounds.