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Variability Study of Ferroelectric Field-Effect Transistors Towards 7nm Technology Node

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ABSTRACT The random variation sources have a significant influence on the performance of ferroelectric field-effect transistor (FeFET). In this work, comparative analysis on the process variation induced variability of FeFET towards a 7 nm technology node has been conducted, including different device structures from bulk to FDSOI and FinFET. The random ferroelectric/dielectric phase variation (PV), the metal work function variation (WFV) and the line-edge roughness (LER) effects are incorporated in TCAD simulations to quantitatively investigate their impacts on the threshold voltage variation. Especially, the Voronoi diagram is employed to realistically model the ferroelectric grain distributions and to accurately simulate the impact of PV on FeFET characteristics.

INDEX TERMS Ferroelectrics, process variations, polycrystalline phases, nonvolatile memory.

I. INTRODUCTION

Ferroelectric materials have been studied for next-generation nonvolatile memory devices because they possess electrically controllable spontaneous polarization states [1], [2]. Among the ferroelectric devices, ferroelectric field-effect transistor (FeFET) has two notable advantages compared to the other ferroelectric devices such as ferroelectric random-access memory (FeRAM), and ferroelectric tunneling junction (FTJ). The first one is that the FeFET could perform the nondestructive read, and the second one is the read-out current of FeFET could be in desirable range for fast $<$10 ns read out. Nevertheless, FeFET needs to improve the cycling endurance and further lower the write voltage by interfacial layer engineering [3].

Previously, ferroelectric materials having perovskite structure such as lead zirconium titanate (PZT), barium titanate (BTO) or strontium bismuth tantalite (SBT) have been used for FeFET [4]. However, those materials need to be thick (at least 100 nm) to exhibit ferroelectric properties, which becomes the limitation to scale down the FeFET to advanced technology node. In the past decade, the Hafnia based ferroelectric materials have received a lot of attentions since only few-nm could achieve the ferroelectric properties. Moreover, they are compatible to the silicon CMOS fabrication processes using atomic-layer deposition (ALD) [4].

State-of-the-art industrial FeFET prototypes have been demonstrated at 28nm [5] and 22nm [6] platforms, the scalability towards more advanced technology node remains to be explored. One of the major challenges for scaling is the process variations similarly as the logic transistors face [7]. In [7], the impact of work function variation (WFV), random dopant fluctuation (RDF), and interface trap (IFT) has been discussed. It shows the WFV has larger influence on the threshold voltage variation than the RDF or IFT. Besides the common variations sources as mentioned above, there is other unique variation source introduced by the multi-grain nature of the ferroelectric materials. When the ferroelectric layer is deposited as thin film, it is generally comprised of many grains. In the case of the Hafnia based ferroelectric material, the ferroelectric grains on the gate stack show two different phases. One is the ferroelectric phase (FE) owing to the orthorhombic structure and the other is the dielectric phase (DE) by the other structures such as monoclinic structure and cubic structure [8]. Those FE/DE phases caused by the atomic structure difference are randomly distributed on the ferroelectric layer, whereby affect the non-uniform formation of the channel inside FeFET. The random phase variation (PV) disperses the threshold voltage (V_{th}) and on/off current of the FeFET. In a previous study [8],

the square diagram was used to model the grains for the variability of the FeFET caused by the PV. However, the actual grains do not have same size as a square but actually have different sizes and shapes as experimentally measured by scanning electron microscopy with a Bruker Optimus TKD detector [9]. To realistically model the actual shape and size of the grains, the Voronoi diagram [10] is more desired on the FeFET simulation. Even though the domain formation inside the grains is naturally random as well, which becomes an additional variation source, we assumed each grain has the same remnant/saturation polarization and coercive field, and considered FE/DE phase variation as the primary source for the ferroelectric material.

In this paper, the variability of the FeFETs towards a 7 nm technology node has been studied using Sentaurus TCAD [11]. Here, we proposed a method to generate the grains modeled with Voronoi diagram and compared the influence of PV using both Voronoi and square diagrams on the threshold voltage variation on the 28 nm node. Next, the impacts of PV, WFV, and LER on the threshold voltage have been compared depending on the different technology nodes (bulk at 28 nm, FDSOI at 22 nm, FinFET at 14 nm and 7 nm). This article is an extension of our conference paper [12], where only 28 nm analysis was reported.

II. SIMULATION METHOD

The 3D FeFET structures used in this simulation are depicted in Fig. 1. For the 28 nm node and 22 nm node, bulk FeFET and fully-depleted silicon-on-insulator (FDSOI) FeFET have been used, respectively [see Fig. 1(a) and (b)]. For the 14 nm node and 7 nm node, FinFET structure has been applied for both technology nodes [see Fig. 1(c)]. Fig. 1(d) shows the conceptual image of WFV, LER and PV included in this simulation. Specifically, since the gate LER does not affect the device performance significantly for the bulk FeFET compared to the WFV and PV [12], it is not included for bulk FeFET simulation. On the other hand, the fin LER has been adopted as well as the WFV and PV for the FeFETs with the FinFET structure (Fe-FinFETs). In addition, FinFET is lightly doped or undoped, RDF is not considered. The structural parameters are summarized in Table 1. The remnant polarization (P_r) and saturation polarization (P_s) of the ferroelectric layer are 15 μC/cm^2 and 25 μC/cm^2, respectively. The coercive field is 1 MV/cm assuming $Hf_{0.5}Zr_{0.5}$ O_2 as a ferroelectric gate stack in this work. We extracted those ferroelectric parameters from the experiments of our group's previous research [10]. The plasma enhanced ALD was used for depositing the $Hf_{0.5}Zr_{0.5}O_2$ layer in [13]. Fig. 2(a) shows the Voronoi-grain and the square-grain for modeling the grain on the ferroelectric layer. Each grain has FE phase (green) or DE phase (blue) depending on its atomic structure. The Voronoi grain generation method is below: 1) the 100×100 nm^2 of Voronoi pattern is created using MATLAB. The different grain sizes are generated following a Gaussian distribution, whose average is an input grain size. 2) capture the pattern as much as the gate area, and

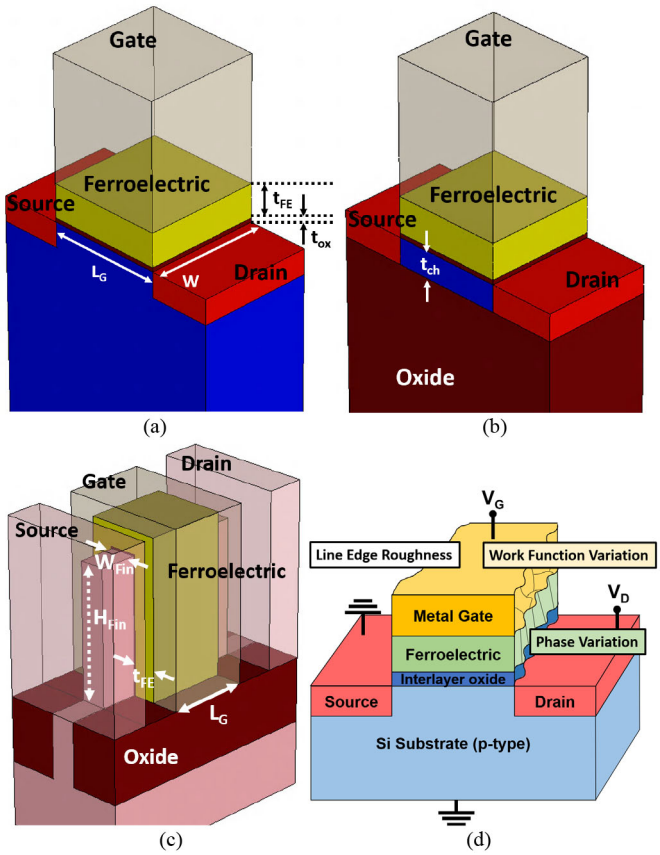

FIGURE 1. (a) Bulk FeFET structure for 28 nm node and (b) FDSOI FeFET for 22 nm node. (c) Fe-FinFET structure for 14 nm and 7 nm node. (d) Three variation sources of FeFETs, which are included in this simulation.

3) extrude the pattern plane with the ferroelectric thickness (t_{FE}). 4) designated the spatial FE/DE phase for grains [see Fig. 2(b)]. Fig. 2(b) shows that the various size of grains is randomly distributed well throughout the whole ferroelectric layer. We used one Voronoi pattern of grain map for a certain technology node since it could statistically represent different FE/DE area ratio and grain sizes together by randomly distributing the FE/DE phase. Fig. 3 shows the I_D-V_G of 28 nm bulk FeFET with and without PV (from 100 samples) using the above method. For the WFV, we employed the built-in function in Sentaurus TCAD. Since we chose the TiN as a metal electrode, 4.6 eV and 4.4 eV were assumed for work function of metal grain (probabilities are 60% and 40%, respectively) [see Fig. 4(a)] [14]. Fin LER was generated by following the 1-D Gaussian autocorrelation function [15], using the LER parameters from the International Roadmap for Devices and System (IRDS) [16]. The correlation length and root-mean-square for 14 nm node (7 nm node) are 20 nm (20 nm) and 1 nm (0.6 nm), respectively [see Fig. 4(b)].

The physical models used in this work include the doping dependent model, thin-layer model, modified local-density approximation model and high-field saturation model for mobility. The Shockley-Read-Hall model and Auger recombination model are employed as recombination models. To

TABLE 1. Simulation parameters.

Name	28 nm node	22 nm node	14 nm node	7 nm node
Gate Length (L_G)	28 nm	25 nm	26 nm	18 nm
Width (W)	28 nm	25 nm	N/A	N/A
Channel Thickness (t_{ch})	N/A	6 nm	N/A	N/A
Oxide Thickness (t_{ox})	1 nm	1 nm	1 nm	1 nm
FE Thickness (t_{FE})	8 nm	8 nm	8 nm	8 nm
Fin Height (H_{fin})	N/A	N/A	42 nm	52 nm
Fin Width (W_{fin})	N/A	N/A	8 nm	6 nm
N-type Doping Concentration	$1\times10^{20}/cm^3$	$1\times10^{20}/cm^3$	$2\times10^{20}/cm^3$	$2\times10^{20}/cm^3$
P-type Doping Concentration	$1\times10^{17}/cm^3$	$1\times10^{17}/cm^3$	$1\times10^{15}/cm^3$	$1\times10^{15}/cm^3$

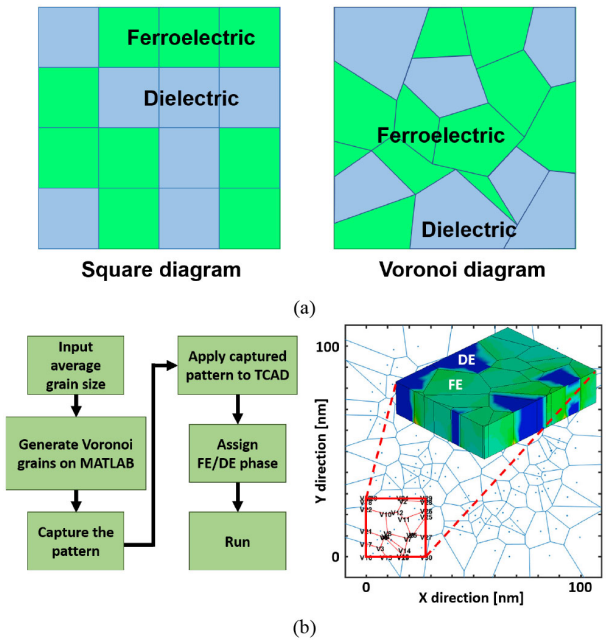

FIGURE 2. (a) Square diagram vs. Voronoi diagram to model the ferroelectric/dielectric phase variation. (b) Voronoi grain generation flow and extracted Voronoi FE/DE grain distribution on the TCAD.

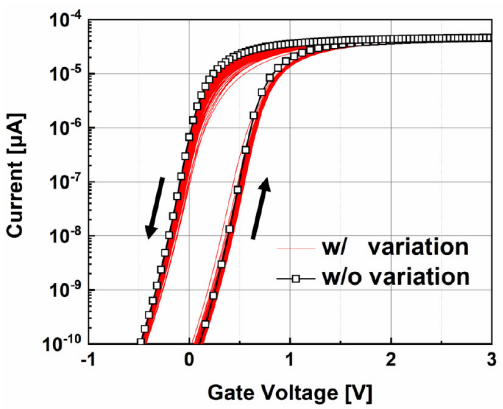

FIGURE 3. I_D–V_G of 28 nm FeFETs with and without PV (average grain size: 6 nm, FE/DE probability: 50%/50%).

efficiently simulate the ferroelectric multi-domain polarization switching, we used Preisach model that is compatible with in the TCAD software. It is recognized that phase

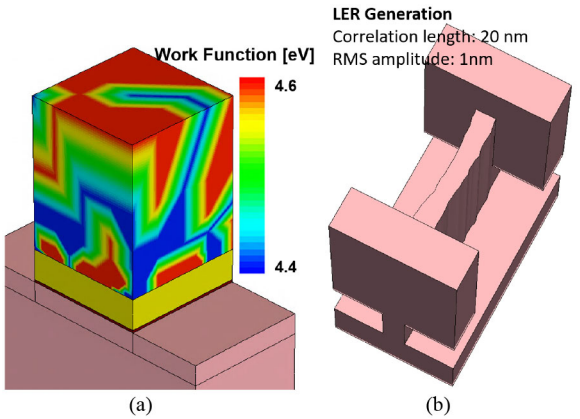

FIGURE 4. TCAD structures considering (a) WFV and (b) Fin LER.

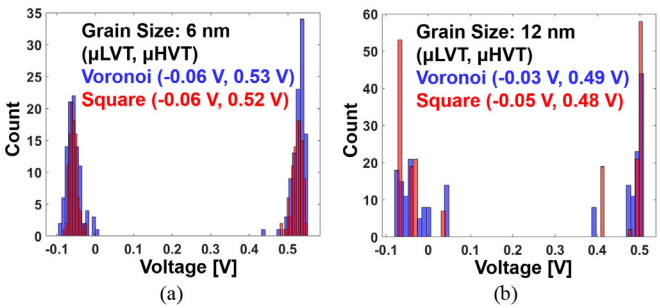

FIGURE 5. HVT and LVT distribution with (a) 6 nm and (b) 12 nm of grain size for Voronoi and square diagrams (FE/DE probability: 50%/50%).

filed modeling of multi-domain polarization switching will give further insights on FeFET design [17], though it is computationally more expensive.

III. RESULTS

As an initial estimation, Fig. 5 shows the high V_{th} (HVT) and low V_{th} (LVT) distribution of a generic bulk FeFET depending on the grain size with 100 samples. The ferroelectric thickness is 6 nm and the interfacial oxide thickness is 0.5 nm. The 24 nm of gate length and width are assumed. The FE/DE phase probability is assumed to 50%/50%. Here the probability ratio is referred to the number of grains. When the average grain size is small, the square diagram has similar V_{th} distribution to the Voronoi diagram. However,

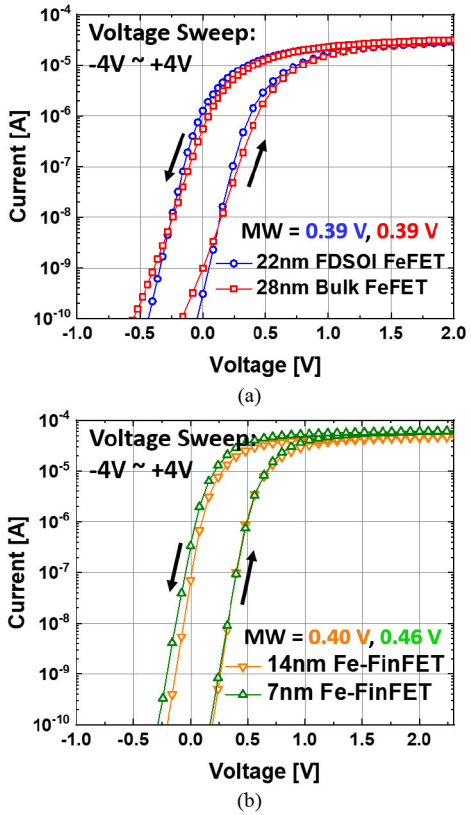

FIGURE 6. I_D-V_G of (a) 28 nm Bulk and 22 nm FDSOI of FeFETs, and (b) 14 nm and 7nm Fe-FinFETs.

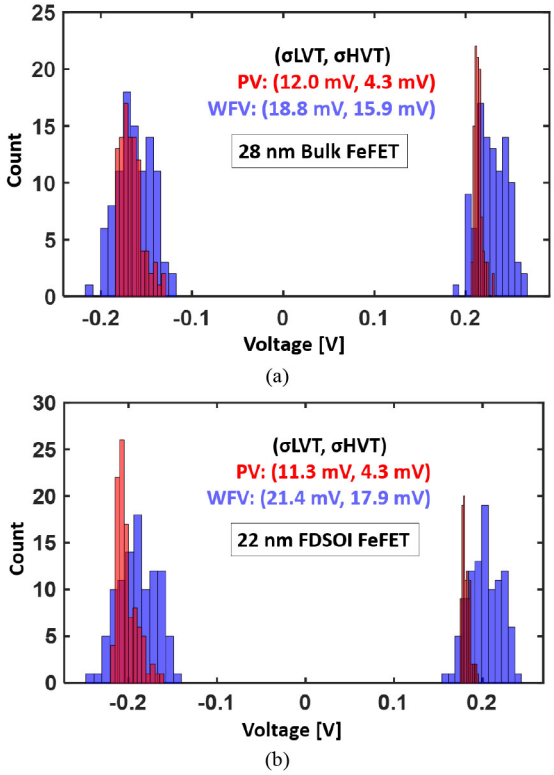

FIGURE 7. HVT and LVT variation of (a) 28 nm bulk FeFET and (b) 22 nm FDSOI FeFET (average grain size: 8 nm, FE/DE probability: 70%/30%).

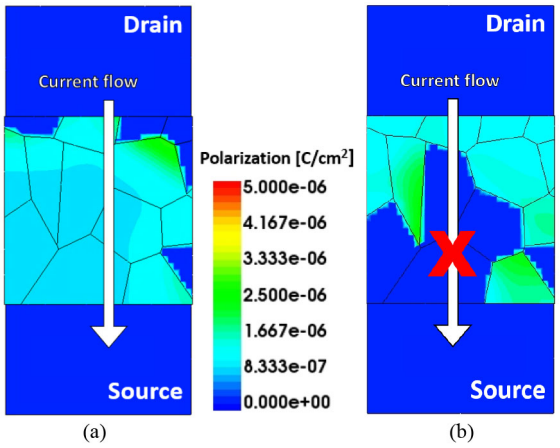

FIGURE 8. Polarization map which has (a) smallest LVT and (b) largest LVT after the program operation (at $V_G = 0$ V). The probability of FE/DE phase is 70%/30% for both cases.

as the average grain size is getting larger (i.e., 12 nm), the threshold voltage distribution of square diagram is much dispersive and discrete than that of Voronoi diagram. Hence, the Voronoi diagram which resembles the shape of actual ferroelectric layer's grains as in the experimental data is exploited in this work. The HVT/LVT standard deviations of 6 nm of grain size were 16 mV/19 mV, and those of 12 nm of grain size were 30 mV/40 mV under Voronoi diagram. The grain size should be minimized for less V_{th} distribution.

Next, a more systematic investigation is conducted. The threshold voltage distributions by the work function variation, phase variation, and line-edge roughness have been investigated depending on the technology node. The FE/DE phase probability is set to be 70%/30% [18]. Since the grain size is similar to the thickness of the ferroelectric layer [19], it is assumed as 8 nm. Fig. 6 shows the I_D-V_G of baseline FeFETs without any variation sources under the four technology nodes. The voltage sweep range is from 4 V to −4 V for all the cases. It is seen that the sub-threshold slope and the memory window is improved with scaling.

After the variation sources are included in the FeFETs in different nodes, the threshold voltages are distributed. The number of samples are all 100 for each case as a balance between the statistics and the 3D TCAD simulation time. Fig. 7 shows the influences of WFV and PV on the 28 nm and 22 nm FeFETs. The gate LER is not considered because the deviation by the LER is smaller than the others [12]. The V_{th} has been extracted using the constant current method at 1 μA/μm. The deviations of HVT and LVT by the WFV are correlated than those by the PV owing to the fact that the WFV shifts the HVT and LVT together in the same direction, whereas the HVT and LVT by the PV moves more independently. Especially, Fig. 8 shows the polarization map of smallest LVT and largest LVT with the same FE/DE ratio in

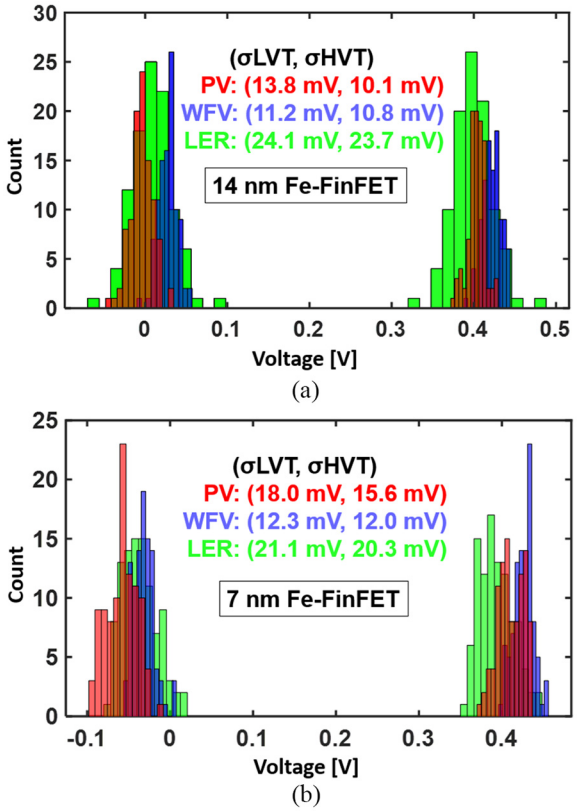

FIGURE 9. Threshold voltage variation of (a) 14 nm node and (b) 7 nm node of Fe-FinFETs by the phase variation, work function variation and line-edge roughness (average grain size: 8 nm, FE/DE probability: 70%/30%).

terms of numbers of grains. Blue color represents the dielectric phase and other colors represent ferroelectric phase with different polarization values. Due to the local variation, the current could not flow in the sample of Fig. 8(b) at the threshold voltage of the sample of Fig. 8(a). The impact of WFV on the threshold voltage is greater than that of PV for both technology nodes. In the case of 28 nm node, the phase variation accounts for 21% (HVT) and 39% (LVT), and the work function variation accounts for 78% (HVT) and 61% (LVT). The WFV-induced V_{th} variation could be mitigated by using thicker gate oxide as well as with higher relative permittivity. In addition, the phase variation can be suppressed by reducing the grain size and increasing the ferroelectric phase grain probability by further device fabrication recipe optimization [18].

Fig. 9 shows the threshold voltage variation of the 7 nm node and 14 nm node of Fe-FinFETs by WFV, PV as well as fin LER. In the case of planar FeFETs, the impact of LER was comparably small, thereby it was not taken into account. However, the impact of fin LER on the Fe-FinFETs is becoming a dominant factor. The σ LVT/σ HVT induced by the LER account for 45%/53% under 14 nm Fe-FinFET design rule, and for 41%/42% under 7 nm Fe-FinFET among three variation sources. Hence, it must be included into the variability analysis as one of primary variation sources. The

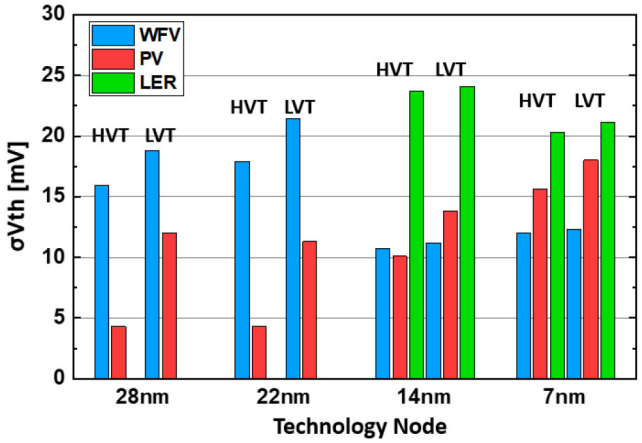

FIGURE 10. Summary of the overall standard deviation of threshold voltage distribution by its individual variation sources.

LER-induced V_{th} variation on the 14 nm node is larger than the 7 nm node. This is because we assumed the 7 nm technology node uses the extreme ultraviolet (EUV) lithography, whereby the input LER parameters for 7 nm node are smaller than those for 14 nm node [16]. The phase variation and work function variation have increased as the technology node changes from 14 nm node to 7 nm node. These two variation sources have a relationship with the effective gate area. For example, as shown in Fig. 5, when the grain size is getting larger, but the gate area is same, the threshold voltage variation (σHVT/σLVT) increases from 16 mV/19 mV to 30 mV/40 mV. The effective gate area of 14 nm Fe-FinFET is 2,392 nm^2, and that of 7 nm Fe-FinFET is 1,980 nm^2, even though the effective width has been increased from 14 nm node to 7 nm node. Hence, the fin should be even taller in order to alleviate the influence of the PV. In Fig. 10, the threshold voltage variation from the 28 nm node to 7 nm node has been summarized to compare the impact of each variation source individually. Since the gate area of 22 nm node is smaller than that of 28 nm node, the overall standard deviation has been degraded. Despite the FinFET structure of FeFET has larger gate area than the planar FeFETs, the fin LER makes the threshold voltage variation worse. Even though the impact of PV is relatively smaller than that of WFV under planar devices, the high threshold voltage deviation by PV is more than a half of HVT deviation by WFV. Furthermore, under the FinFET structure, the PV accounts for 28% $\sim$ 35%, which is the second place among these three variation sources. Hence, the PV is still one of the important variation sources. To sum up, WFV and PV should be incorporated for the planar FeFETs. Fe-FinFETs need to include the WFV, PV as well as the fin LER together for accurately quantifying the process variations.

IV. CONCLUSION

A comparative study considering the impacts of different random variation sources of FeFET on the threshold voltage has been theoretically explored towards 7 nm technology

node. We employed Voronoi diagram for modeling the grains of HZO ferroelectric layer. Among the considered variation sources, the threshold voltage variation is mostly affected by the work function variation on planar devices and by the fin line-edge roughness on FinFET structures, while dielectric/ferroelectric phase variation plays an important role as well. These variations are expected to be mitigated with further optimization of gate stack and structural parameters. In addition, improved HZO atomic-layer-deposition recipes is necessary to achieve better random phase variation by increasing the probability of ferroelectric phase grain and/or reducing the average grain size. Besides these device-to-device variations, the temporal effects such as read noise and cycle-to-cycle variation also need to be quantified for the practical FeFET application in the future. Impact of antiferroelectric phases needs to be explored as well.

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