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A Modified NMOS Inverter With Rail-To-Rail Output Swing and Its Application in the Gate Driver Integrated by Metal Oxide TFTs

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ABSTRACT A modified NMOS inverter employing output feedback theme has been proposed in this paper. The feedback structure can guarantee high voltage output at a wider range of low voltage input. The proposed inverter and the conventional pseudo-CMOS inverter are both fabricated by top gate coplanar In-Zn-O thin film transistors (IZO TFTs) for comparing. The experimental results show that the proposed inverter possesses better static performance exhibiting noise margin NM_L/NM_H, output swing V_{OL}-V_{OH}, switching threshold V_M of 3.95/5.82 V, 0.05-9.97 V, 4.05 V, respectively. In addition, the proposed inverter is also applied in the gate driver integrated by IZO TFTs to further verify its function. Benefited from good static characteristic of the proposed inverter, the output module is well controlled to produce a good output waveform. It is measured that the output waveform of the 120th-stage has almost no distortion compared with that of the 1st-stage at 25 kHz.

INDEX TERMS Modified NMOS inverter, IZO TFTs, gate driver.

I. INTRODUCTION

The inverter is one of the most basic unit in the modern digital circuits [1]–[3]. The well-known CMOS inverter has distinct advantages in static and dynamic characteristic. With the development of thin film transistors (TFTs) technology, the researchers also attempt to design integrated circuits by TFTs for their application in flexible electronic systems or wearable devices. Generally, it is difficult to directly employ a-Si:H TFTs or metal oxide TFTs to CMOS circuits due to the lack of reliable p-type device. However, several design schemes for inverter circuit have been tried to overcome the problem.

The ratioed logic inverter consisting of pull-up and pull-down network are simple enough in structure [4]–[7]. However, the defects like narrow output swing severely impede its practical application. Compared with ratioed logic inverter, the pseudo-CMOS inverter [8]–[11] has the obvious advantages in output swing, delay time, power consumption, etc. There are still some disadvantages such as low noise margin and asymmetric voltage-transfer characteristic (VTC). In addition, the differential logic inverter has good stability due to effectively avoiding the influence of the noise [12] The inverter composed of dual-gate TFTs [13]–[15] could adjust the turn-on voltage (Von) of the driving transistor by applying bias to the second gate electrode to get symmetric VTC similar with CMOS inverter. But there are also some different limitations in terms of design and technology for these other methods.

This paper presents a new inverter schematic integrated by IZO TFTs with top gate structure. The proposed inverter

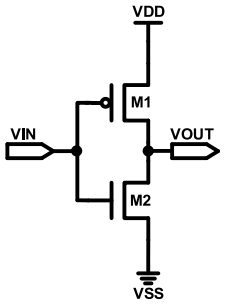

FIGURE 1. Inverter A: Complementary inverter.

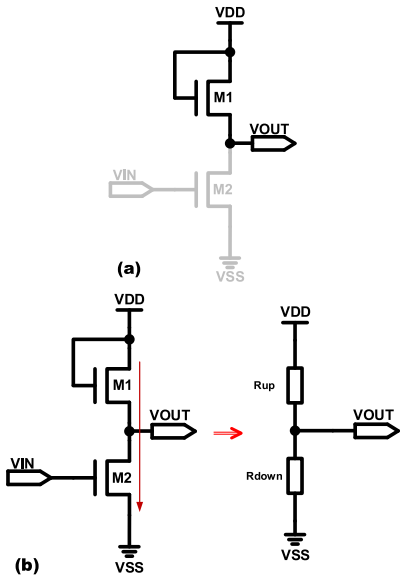

FIGURE 2. Inverter B: Diode-connected inverter (a) Input low voltage (b) Input high voltage.

has good static characteristics including large output swing, large noise margin and symmetric VTC curve. Furthermore, the proposed inverter is also applied into the gate driver integrated by metal oxide TFTs.

II. THE INVERTER STRATEGY AND THE PROPOSED INVERTER

The complementary inverter (inverter A) employing complementary structure is widely used in CMOS or LTPS TFT [16]–[19] circuit, as shown in Fig. 1. The diode-connected inverter (inverter B) depicted in Fig. 2 uses one diode-connected TFT (M1) as enhancement-type load, thus its process requirement will be lower than that of inverter A. Nonetheless, the output swing of inverter B is narrower than that of inverter A. As shown in the Fig. 2(a), the gate-source voltage of M1 decreases from VDD to the threshold voltage of M1 (V_{th1}) when the output voltage of inverter is charged to high from low. As shown in Fig. 2 (b), M2 prevents the output voltage from approaching VSS as the input voltage is high. The bootstrap inverter [7] (inverter C) shown in Fig. 3 effectively improves the charging speed

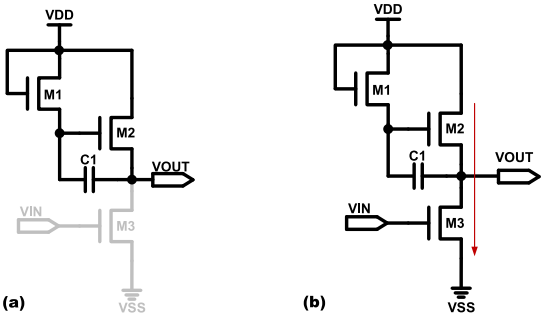

FIGURE 3. Inverter C: Bootstrap inverter (a) Input low voltage (b) Input high voltage.

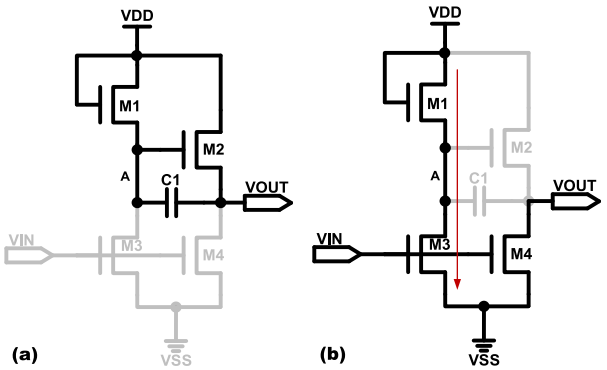

FIGURE 4. Inverter D: Pseudo-CMOS inverter (a) Input low voltage (b) Input high voltage.

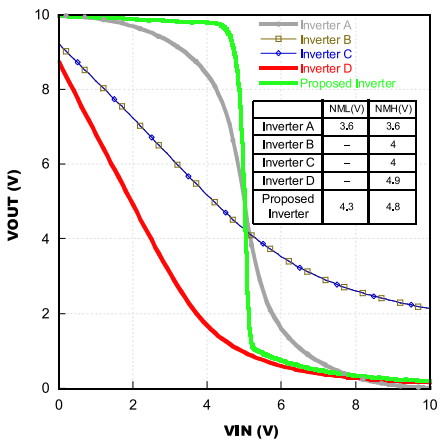

FIGURE 5. The voltage-transfer characteristic of different inverters.

of pull-up TFT(M2) by employing bootstrapped theme during the period of the output voltage charged to high from low. However, it is hard to attain rail-to-rail output by only changing TFT channel size since its low output voltage is always greater than VSS. The Pseudo-CMOS inverter [8] (inverter D) depicted in Fig. 4 adds an additional pull-down TFT (M3) compared with the inverter C. As shown from Fig. 4(a), inverter D works like the inverter C during the period of the output voltage charged to high from low. As shown in Fig. 4(b), M3 releases the voltage charged in node A to turn off M2 when input voltage is high to gain low output voltage.

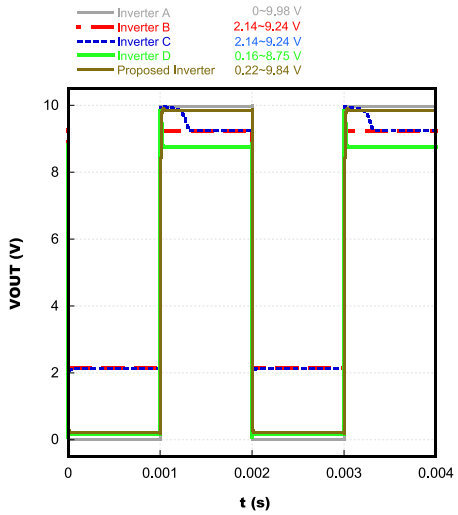

FIGURE 6. The dynamic characteristic of different inverters.

TABLE 1. The design parameters of inverters.

	A	B	C	D	Proposed inverter
M1(μm /μm)	30/5	20/5	10/5	10/5	10/5
M2(μm /μm)	30/5	30/5	20/5	20/5	20/5
M3(μm /μm)	--	--	30/5	15/5	15/5
M4(μm /μm)	--	--	--	30/5	60/5
M5(μm /μm)	--	--	--	--	60/5
M6(μm /μm)	--	--	--	--	30/5
C1 (pF)	--	--	0.5	0.5	0.5

Fig. 5 shows the voltage-transfer characteristic for the different inverters above, and TABLE 1 shows the specific parameters for simulation. In addition, the VDD/VSS used in all the simulation processes are 10V/0V respectively. The inverter A have the best noise margin and output swing, but it can't be realized by unipolar TFTs. The inverter B and C have the same behavior on the voltage-transfer characteristic, and they both lack a low enough output voltage. Notice that, inverter B and C have the same VCT characteristics since the input voltage changes slowly during scanning, and the capacitor has enough time to response. The inverter D has satisfied low output voltage, but its low-level noise margin (NM_L) still cannot be calculated since the critical voltage point for low voltage is null. On the whole, the inverter D is more desirable for unipolar TFTs compared to the inverters of A, B and C.

Figure 6 shows the dynamic characteristic of the different inverters. The inverter A has the optimal dynamic characteristic, but it's hard for the application of metal oxide TFTs. The output swing of inverter B is much narrower compared with other inverters due to the diode connection of pull-up TFT. For the inverter C, the bootstrapping capacitor (C1) boots the gate of M2 above VDD when the output voltage arises from VOL to VOH, so that M2 can turn fully on to drive VOUT to VDD. Similar thing happens to the inverter D to improve the VOH and the rising time of output voltage [20]. But both of the inverter C and D can't keep the VOH close to VDD due to the leakage current of pull-down TFTs.

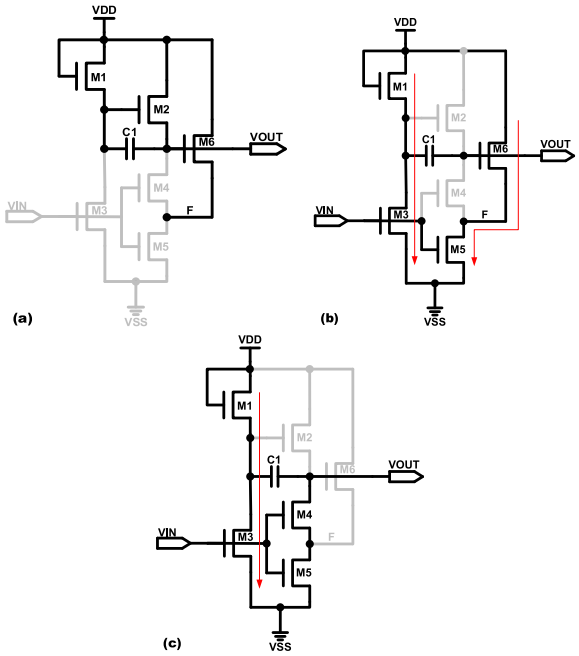

FIGURE 7. The proposed inverter (a) Input low voltage; (b) Input higher voltage but $V_{GS4} < V_{TH4}$; (c) Input high voltage.

This paper proposed a new inverter, which employs the output signal as feedback to improve the NM_L of the inverter D (the pseudo-CMOS inverter). As shown in Fig. 7, the proposed inverter adds two transistors M5 and M6 compared with inverter D. M5 is in series with M4, and M6 is controlled by output signal VOUT, which can be seen as serial-connected two transistors (STT) structure [21], [22]. As shown in Fig. 7(a), the output signal VOUT is high and M6 is turn on when the input signal VIN is low. As shown in Fig. 7(b), M3 and M5 is turn on when VIN starts to go up. And then M4 remains closed for some time unless the gate-source voltage of M4 (V_{GS4}=VIN-V_F) is higher than its threshold voltage (V_{TH4}), as shown in Fig. 7(c). In other words, the output signal VOUT holds high within a certain range of low-level input signal and NM_L should be improved. As a result, the value of NM_L is mainly determined by the V_F, rather than the threshold voltage of M4 in the pull-down network. Furthermore, the VOUT would drop sharply when V_{GS4} is higher than V_{TH4} since M5 has been fully opened to form the current path. Consequently, the voltage-transfer characteristic of proposed inverter may approximate to that of inverter A as shown in Fig. 5.

III. EXPERIMENTAL RESULTS OF THE PROPOSED INVERTER

To verify the feasibility of the proposed inverter, the proposed inverter and the pseudo-CMOS inverter are fabricated on the same glass by unipolar metal oxide TFTs process. Fig. 8 shows the IZO TFTs with top gate coplanar structure, which can effectively reduce the parasitic capacitance [23]. The fabrication process is described as follows: The IZO thin film is deposited on the glass substrate using the

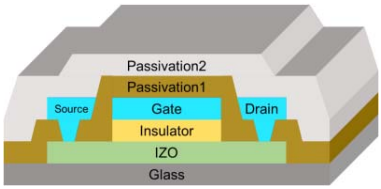

FIGURE 8. Structure of IZO TFT.

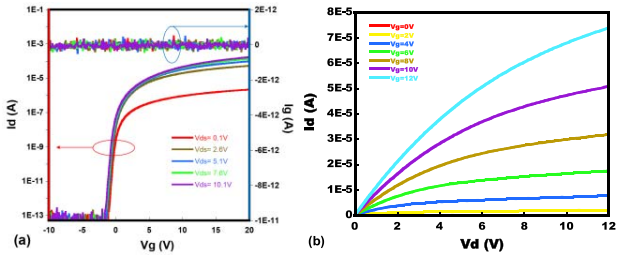

FIGURE 9. The characteristic curve of TFT (W/L=30um/5um) (a) transfer characteristic curve; (b) output characteristic curve.

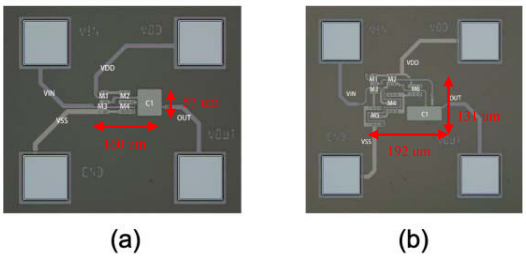

FIGURE 10. The micrograph of (a) inverter D; (b) proposed inverter.

RF magnetron co-sputtering system. Then a gate insulator (SiO_2, 300 nm) is deposited by plasma-enhanced chemical vapor deposition (PECVD) and a gate metal (Mo, 200 nm) is deposited subsequently by DC sputtering. After that, a 230 nm SiO_2 is grown by PECVD as the isolation layer to prevent the direct contact between Gate electrode and Source/Drain electrodes. Next, Mo source (S)/drain (D) electrodes (Mo, 230 nm) are formed by DC sputtering and patterned by wet etching. After that, a 2 um organic as passivation is grown by PECVD. Fig. 9 shows the transfer and output characteristics of TFT (W/L=30um/5um). It is found that the threshold voltage, subthreshold swing, I_{on}/I_{off} is 0.54 V, 0.29 V/dec, 10^9 at the condition of Vds=10.1 V, respectively. And the structure of M4 cascade with M5 in proposed inverter is equivalent to M4 in inverter D. TABLE 1 depicts the detail parameters of inverters, Fig. 10 shows the micrograph of inverter D and the proposed inverter.

Table 2 indicates the experimental results of the inverter D and the proposed inverter by the same metal oxide TFTs process, as well as other results presented in the previous works. However, it is difficult to perform comparison between our results and the previous published works since there exists many differences at the performances of TFTs, the design parameters of devices and conditions of test. Fig. 11 depicts

TABLE 2. The comparison of different inverters.

	Inverter A[18]	Inverter B[1]	Inverter D[8]	Inverter D	Proposed inverter
VDD(V)	3	10	40	10	10
Output swing (V)	--	0.85~9.33	--	0.05~8.58	0.05~9.97
NM_H (V)	1.17	--	16.9	5.03	5.82
NM_L (V)	1.79	--	0.96	--	3.95
V_M (V)	--	--	20.05	2.7	4.05
t_r (us)	--	1.26	--	7.29	31.5
t_f (us)	--	0.11	--	4.09	10.0
Power(uW)	0.24	261.0	--	49.7	50.8
Area(um^2)	--	30800	16464	9120	25152

the measured voltage-transfer characteristic of the inverter D and the proposed inverter. The measured conditions for the inverter D and the proposed inverter are identical for objective comparison. VDD and VSS are set to be 10V and 0V, respectively. And the input signal VIN scans from 0V to 10V. For the inverter D, the output swing, the NM_L/NM_H, the V_M are 0.05V~8.58V, null/5.03V, 2.7V, respectively. However, for the proposed inverter, the output swing, the NM_L/NM_H, the V_M are 0.05V~9.97V, 3.95V/5.82V, 4.05V, respectively. The proposed inverter has two more transistors than the inverter D, and causes the area increased from $9120um^2$ to $25152um^2$. At the cost of this, we receive some better merits in the proposed inverter as below. The output swing arrives at 0.05~9.97V and achieves rail-to-rail output swing improved by 16% compared with inverter D. Furthermore, the noise margin is widened by 3.75V compared with inverter D. What is the most important, the NM_L of the proposed inverter is determined by VF, unlike inverter A/B/C/D whose NM_L is determined by the threshold of TFTs. Since the proposed inverter is relatively insensitive to threshold voltage.

Fig. 12 shows the transient waveforms of the inverter D and the proposed inverter, which is consistent with the simulation results shown in Fig. 6. The blue line denotes the pulse signal VIN with the frequency of 500Hz both for the inverter D and the proposed inverter. And the red and yellow lines denote the VOUT of the inverter D and the proposed inverter, respectively. As shown in Fig. 12, the VOUT of inverter D is initially jumped to 9.9V due to the bootstrapped effect of capacitor C1 at input signal VIN=0V, and then it is reduced and kept at 8.82V due to the leakage path of M4. Whereas, the output signal VOUT of the proposed inverter is charged to 9.40V and kept at this value without voltage overshoot. The transient results of these two inverters basically conform to the output swings extracted from the voltage-transfer characteristic. But on the other hand, the rise time/fall time (t_r/t_f,) of the proposed inverter increases to 31.5us/10.0us due to the existence of M6. As shown in Fig. 7(b), since the additional current path from VDD to ground occurs for an instantaneous moment when the level flips, the power consumption of the proposed inverter is only slightly larger than that of the invert D. However, the area of the proposed inverter is obviously larger than that of inverter D due to larger number of TFTs. Overall consideration, the performance of the

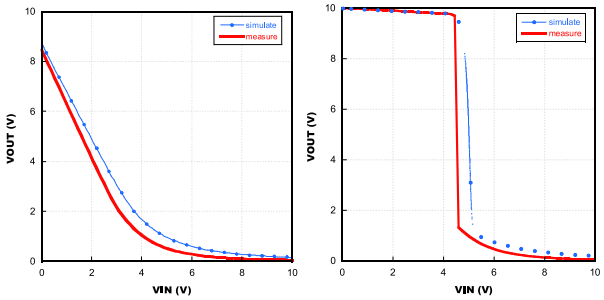

FIGURE 11. The voltage-transfer characteristic of (a) inverter D; (b) proposed inverter.

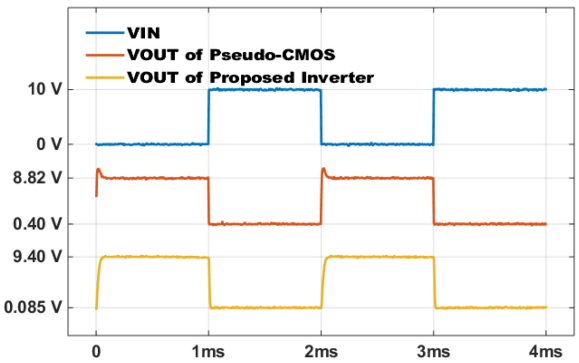

FIGURE 12. The measured transient waveforms.

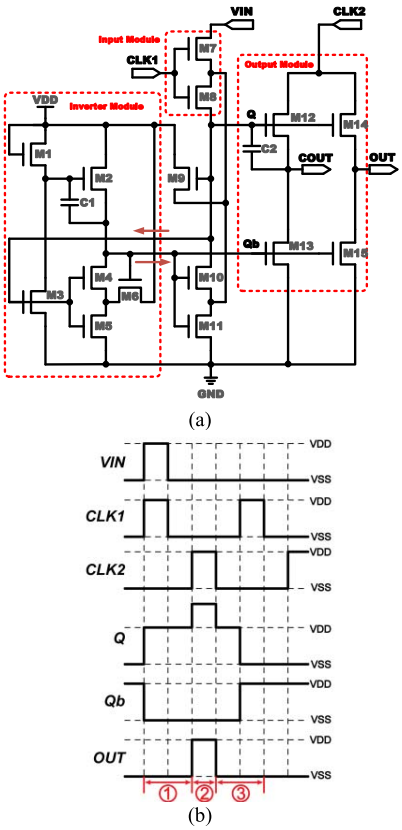

FIGURE 13. (a) The schematic of proposed gate driver; (b) The operated waveforms of proposed gate driver.

proposed inverter is improved in some aspect by employing feedback theme compared with the inverter D.

IV. THE NEW GATE DRIVER WITH THE PROPOSED INVERTER

The gate driver integrated TFTs is critical for achieving narrow bezel and saving process cost in flat display panel. The inverter is the necessary module for achieving the level reversal in the gate driver [24]–[26]. It is thought that the proposed inverter may be applied in the gate driver due to its good static characteristic, as shown in Fig. 13(a). Thereinto, M1∼M6 and capacitor C1 compose the proposed inverter module, M7∼M8 compose the input module, M12∼M15 and capacitor C2 compose the output module. The proposed inverter is hard to be affected by the voltage fluctuation at Q due to the coupling effect of parasitic capacitors in M12. Fig. 13(b) shows the operation of gate driver, which can be divided into three periods.

In period ①, VIN and CLK1 turn to high at the same time, thus node Q is charged to high through the input module. After that, VIN and CLK1 switch to low to shut down the input module. It should be noticed that Qb has been overturn to low by the proposed inverter module.

In period ②, CLK2 turns to high and output nodes (COUT, OUT) are charged to high through the output module. The charging time can be reduced due to the coupling effect of C2.

In period ③, CLK2 changes to low and output voltage are discharged to low through the output module. Thereafter, CLK1 goes back to high for the purpose of resetting the potential of each node.

TABLE 3. The design parameters of gate driver.

Device	Parameter
M9(μm /μm)	14/7
M1, M3, M6(μm /μm)	21/7
M2, M10, M11(μm /μm)	28/7
M5(μm /μm)	35/7
M4, M13(μm /μm)	105/7
M7, M8(μm /μm)	203/7
M12, M15(μm /μm)	420/7
M14(μm /μm)	840/7
C1 (pF)	0.5
C2 (pF)	3
VDD(V)	10
VSS(V)	-6
f_{CLK}(kHz)	25

The proposed gate driver with 120 stages has been successfully fabricated by metal oxide TFTs with the top gate process on the glass substrate, the process of which has been described at Section III. Table 3 indicates the design specifications of the circuit with the critical length of 7μm for all TFTs. VDD and VSS for circuit driving are 10V and −6V respectively. Fig. 14 shows the micrograph of the proposed gate driver, and the area of one stage including signal wires is 750μm*285μm.

Fig. 15 depicts the output waveforms of 1st stage and 120th stage with resistive load R_L=1kΩ and capacitive load

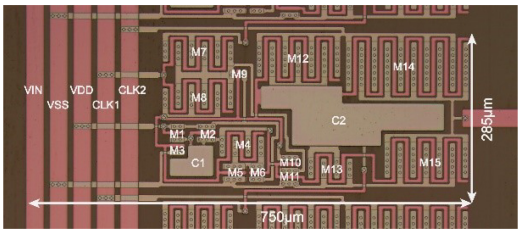

FIGURE 14. **The micrograph of the proposed gate driver.**

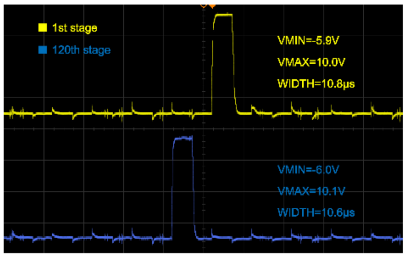

FIGURE 15. **Output waveforms at 1st stage and 120th stage.**

C_L=30pF. And the clock frequency is 25 kHz with the pulse width of 10μs. The output waveform of 1st-stage is denoted by yellow line with the voltage swing of −5.9V∼10V, while that of 120th-stage is denoted by blue line with the voltage swing of −6.0V∼10.1V. Therefore, the gate driver with 120 stages can output full-swing waveforms based on the proposed inverter module.

V. CONCLUSION

In this paper, a modified NMOS inverter with output feedback structure has been proposed, which is verified by the IZO TFTs process. Compared with pseudo-CMOS, the proposed inverter has better static characteristic, which has larger noise margin NM_L/NM_H of 3.95/5.82 V, wider output swing V_{OL}-V_{OH} of 0.05-9.97 V, better switching threshold V_M of 4.05 V. For the NM_L, the proposed inverter is relatively insensitive to threshold voltage. Furthermore, the proposed inverter is successfully applied in a new gate driver circuit with 120-stages by the same TFTs process. The 120th-stages output waveform nearly has no distortion compared with 1st-stage output waveform, which proves the validity of the proposed inverter for its application in the gate driver.

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